AOK033V120X2Q

1200 V αSiC Silicon Carbide Power MOSFET

Features

- Proprietary αSiC MOSFET technology
- Low loss, with low $R_{DS,\ ON}$
- Fast switching with low R_G and low capacitance
- Optimized gate drive voltage ($V_{GS} = 15\,V$)
- Low reverse recovery diode (Qrr)
- AEC-Q101 Automotive Qualified

Product Summary

V_{DS} @ $T_{J,\ max}$	1200 V
I_{DM}	120 A
$R_{DS(ON),\ typ}$	33 mΩ
Q_{rr}	226 nC
E_{OSS} @ 800 V	63 µJ
100% UIS Tested	

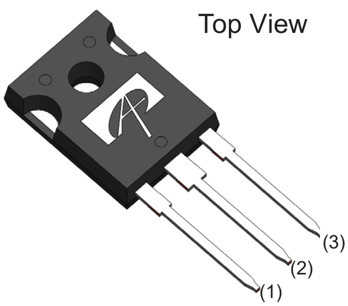
RoHS Compliant

Applications

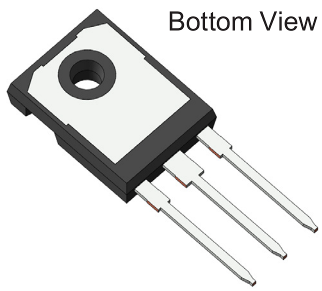
- xEV Charger
- Electric Vehicle Supply Equipment (EVSE)
- Motor Drives
- Automotive Inverters

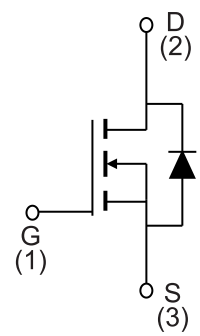
Pin Configuration

Top View



Bottom View





Ordering Part Number	Package Type	Form	Shipping Quantity
AOK033V120X2Q	TO-247-3L	Tube	30/Tube

Absolute Maximum Ratings

(T_A = 25°C, unless otherwise noted)

Symbol	Parameter		AOK033V120X2Q	Units
V_{DS}	Drain-Source Voltage		1200	V
$V_{GS,\ MAX}$	Gate-Source Voltage	Maximum	-8/+18	V
$V_{GS,OP,TRANS}$		Max Transient(A)	-8/+20	
$V_{GS,OP}$		Recommended Operating (B)	-5/+15	
I_D	Continuous Drain Current	$T_C = 25°C$	68	A
		$T_C = 100°C$	48	
I_{DM}	Pulsed Drain Current(C)		120	
E_{AS}	Single Pulsed Avalanche Energy(D)		1000	mJ
P_D	Power Dissipation(C)		300	W
T_J, T_{STG}	Junction and Storage Temperature Range		-55 to 175	°C
T_L	Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	AOK033V120X2Q	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient (E,F)	40	°C/W
$R_{\theta JC}$	Maximum Junction-to-Case (G)	0.5	°C/W

Electrical Characteristics

(T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250 µA, V_{GS}=0 V, T_J=25°C		1200			V
		I_D=250 µA, V_{GS}=0 V, T_J=150°C			1200		
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=1200 V, V_{GS}=0 V, T_J=25°C				100	µA
I_{GSS}	Gate-Body Leakage Current	V_{DS}=0 V, V_{GS}=+15/-5 V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} , I_D=17.5 mA			2.8		V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=15 V, I_D=20 A	T_J=25°C		33	43	mΩ
			T_J=150°C		45		
g_{FS}	Forward Transconductance	V_{DS}=20 V, I_D=20A			15	-	S
V_{SD}	Diode Forward Voltage	I_S=17.5A, V_{GS}=-5 V			4	5	V
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0 V, V_{DS}=800 V, f=1 MHz			2908		pF
C_{oss}	Output Capacitance				128		pF
C_{rss}	Reverse Transfer Capacitance				9.9		pF
E_{oss}	Coss Stored Energy				63		µJ
R_G	Gate Resistance	f=1 MHz			1.7		Ω
SWITCHING PARAMETERS							
Q_g	Total Gate Charge	V_{GS}=-5/+15 V, V_{DS}=800 V, I_D=20A			104		nC
Q_{gs}	Gate Source Charge				37		nC
Q_{gd}	Gate Drain Charge				32		nC
$t_{d(on)}$	Turn-On Delay Time	V_{GS}=-5 V/+15 V, V_{DS}=800 V, I_D=40A, R_G=2 Ω, L=60 µH, FWD: AOK033V120X2Q			12.7		ns
t_r	Turn-On Rise Time				40.5		ns
$t_{d(off)}$	Turn-Off Delay Time				16.4		ns
t_f	Turn-Off Fall Time				4.7		ns
E_{on}	Turn-On Energy				980		µJ
E_{off}	Turn-Off Energy				72		µJ
E_{tot}	Total Switching Energy				1052		µJ
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=1500A/us, V_{GS}=-5 V V_{DS}=800 V			61.3		ns
I_{rm}	Peak Reverse Recovery Current				11.4		A
Q_{rr}	Body Diode Reverse Recovery Charge				227		nC

Notes:

A. t_{pulse} < 1 µs, f > 1 Hz
B. Device can be operated at V_{GS}=0/15 V. Actual operating VGS will depend on application specifics such as parasitic inductance and dV/dt but should not exceed maximum ratings.
C. The power dissipation P_D is based on $T_{J(MAX)}$= 175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
D. L=5 mH, I_{AS}=20A, R_G=25 Ω, Starting T_J=25°C.
E. The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25°C.
F. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
G. The value of $R_{\theta JC}$ is measured with the device mounted to a large heat-sink, assuming a maximum junction temperature of $T_{J(MAX)}$= 175°C.
H. The static characteristics in Figures 1 to 8 are obtained using < 300 ms pulses, duty cycle 0.5% max.
I. These curves are based on $R_{\theta JC}$ which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$ = 175°C. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

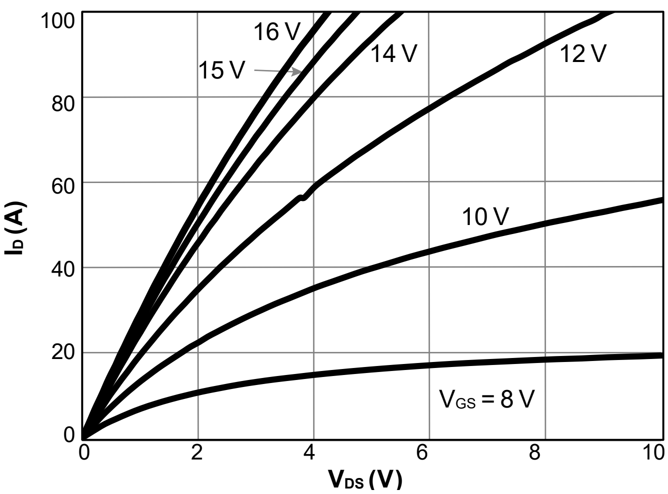


Figure 1. On-Region Characteristics T_J = 25°C

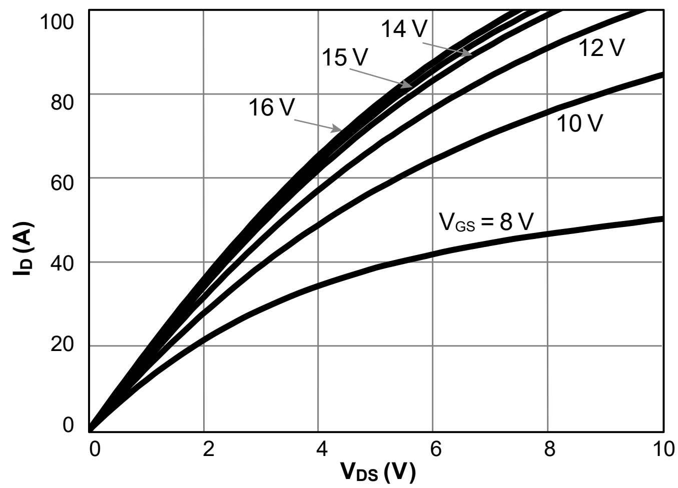


Figure 2. On-Region Characteristics T_J = 175°C

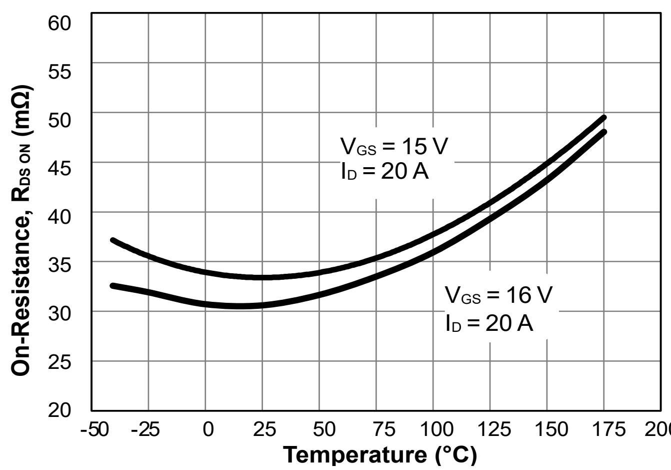


Figure 3. On-Resistance vs. Junction Temperature

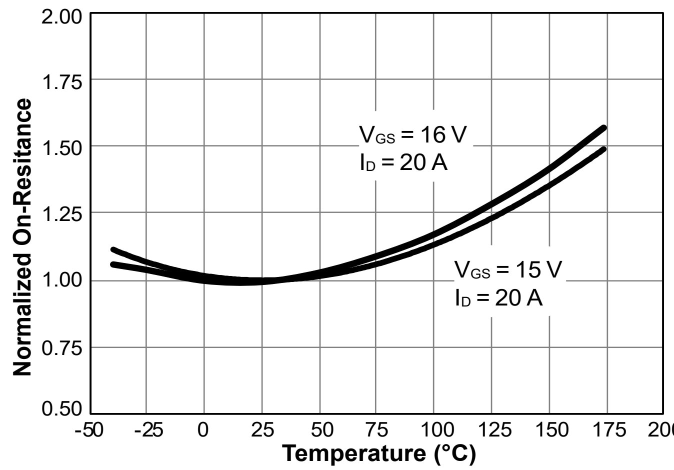


Figure 4. Normalized On-Resistance vs. Junction Temperature

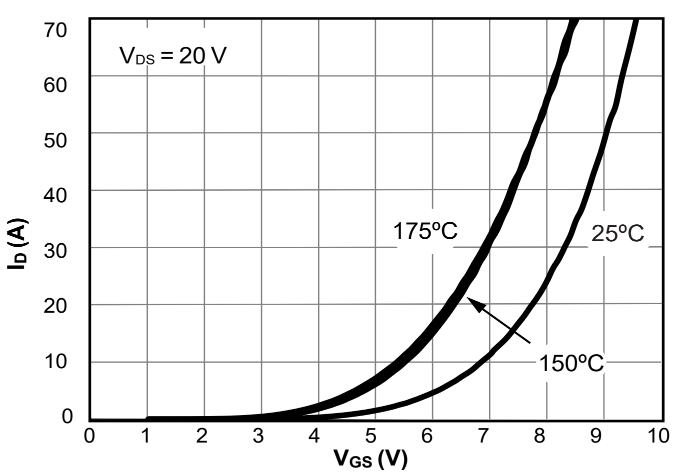


Figure 5. Transfer Characteristics

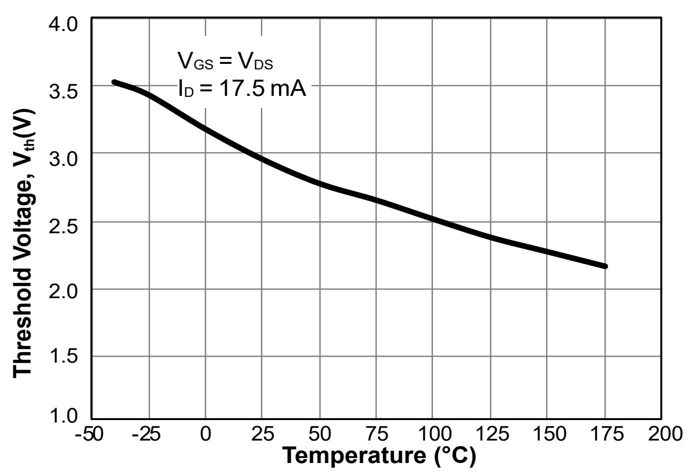


Figure 6. Threshold Voltage vs. Junction Temperature

Typical Electrical and Thermal Characteristics *(Continued)*

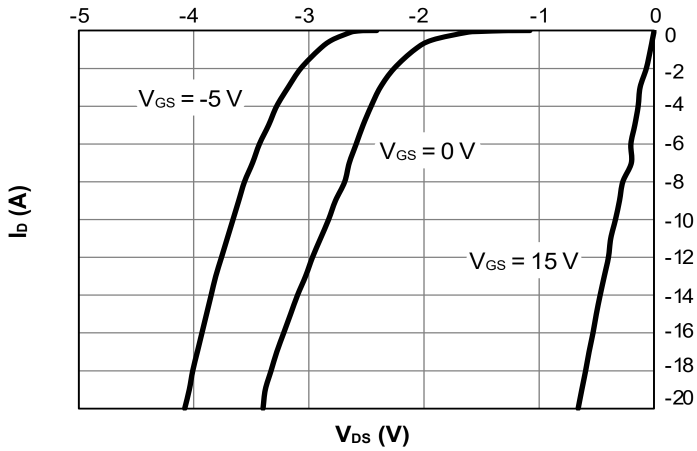


Figure 7. Body-Diode Characteristics at 25°C

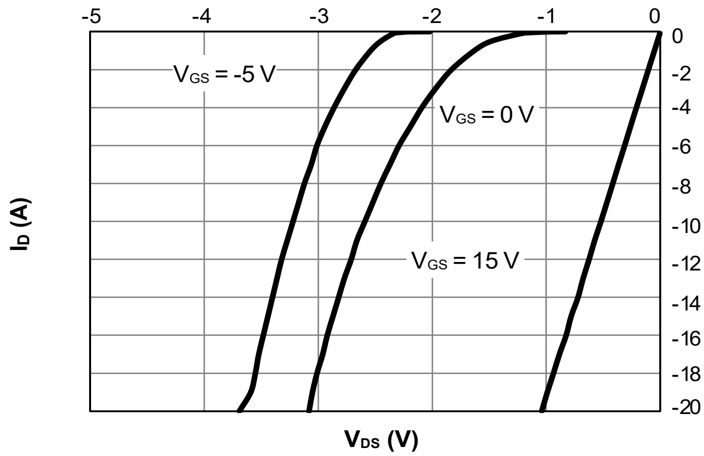


Figure 8. Body-Diode Characteristics at 175°C

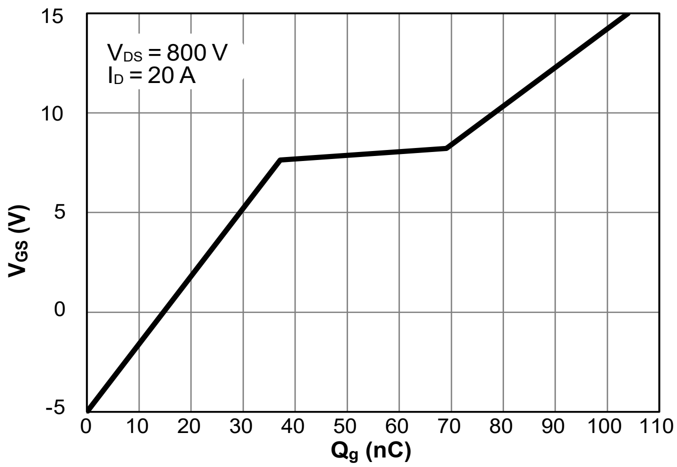


Figure 9. Gate-Charge Characteristics

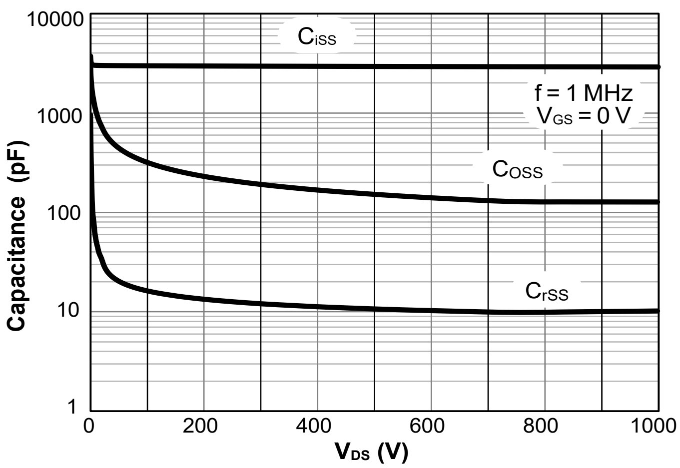


Figure 10. Capacitance Characteristics

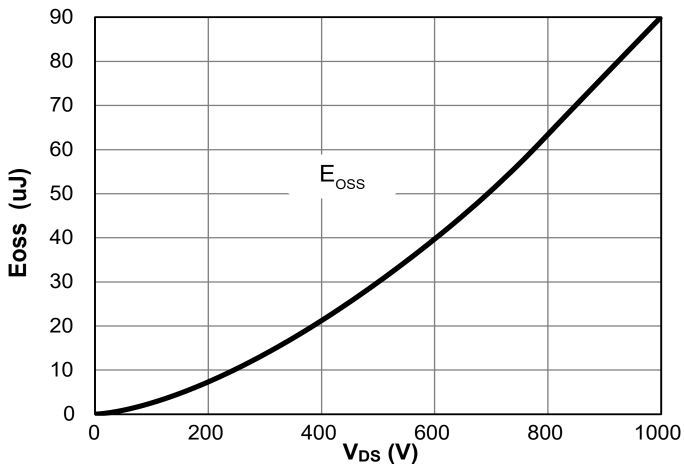


Figure 11. Coss Stored Energy

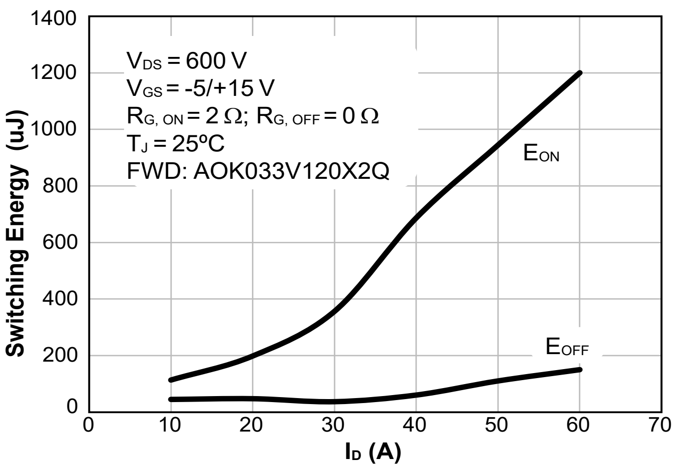


Figure 12. Switching Energy vs. Drain Current

Typical Electrical and Thermal Characteristics *(Continued)*

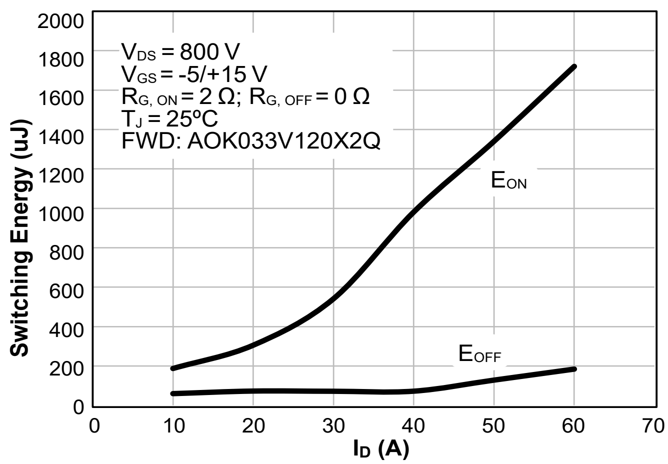


Figure 13. Switching Energy vs. Drain Current

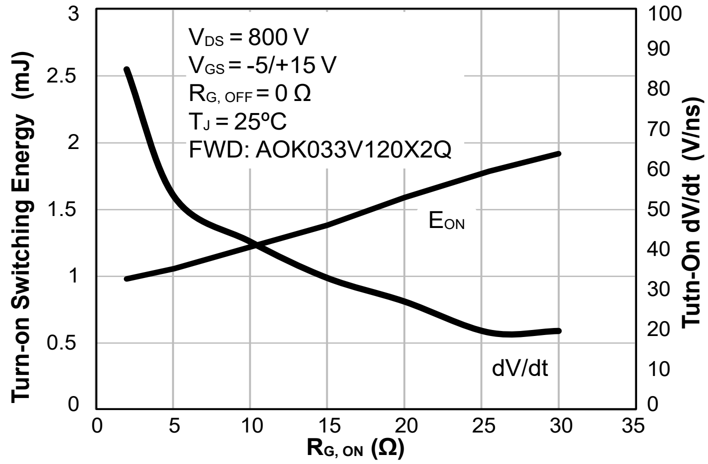


Figure 14. Turn-On Energy and dV/dt vs. External Gate Resistance

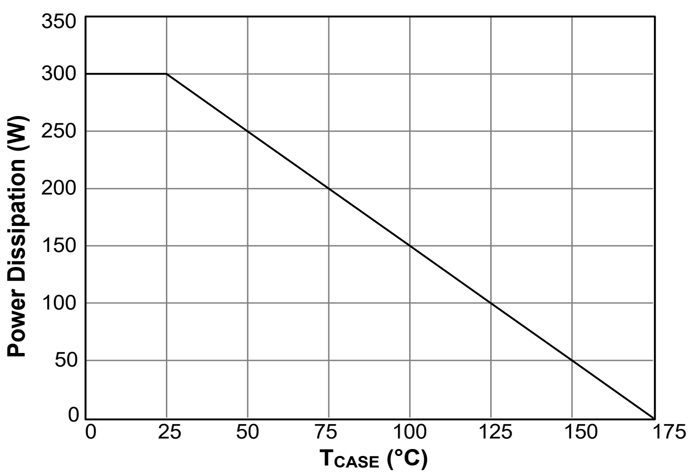


Figure 15. Power Derating vs. Case Temperature (Note I)

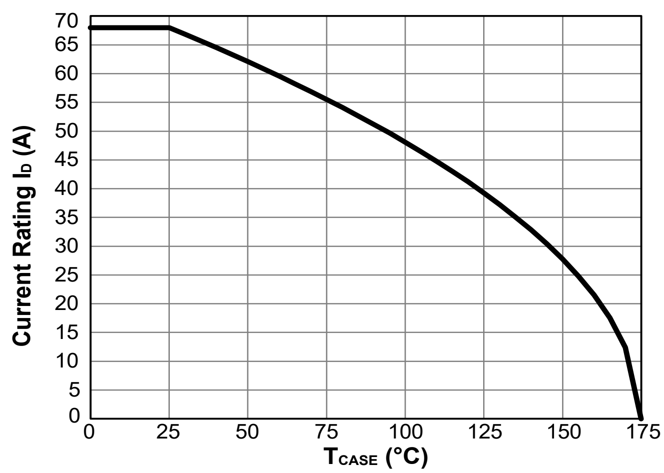


Figure 16. Current Derating vs. Case Temperature (Note I)

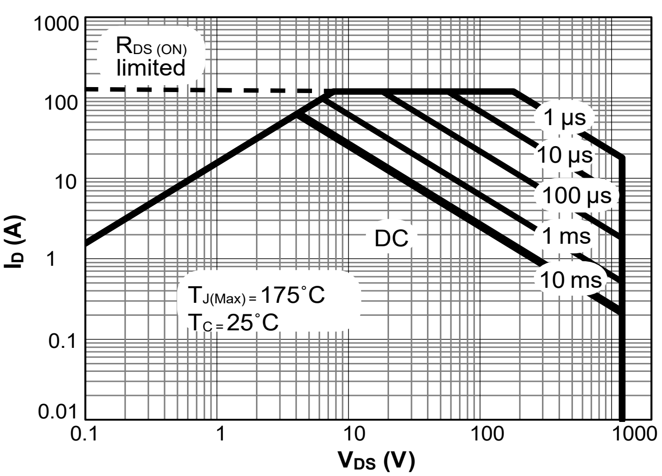


Figure 17. Maximum Forward Biased Safe Operating (Note I)

Typical Electrical and Thermal Characteristics *(Continued)*

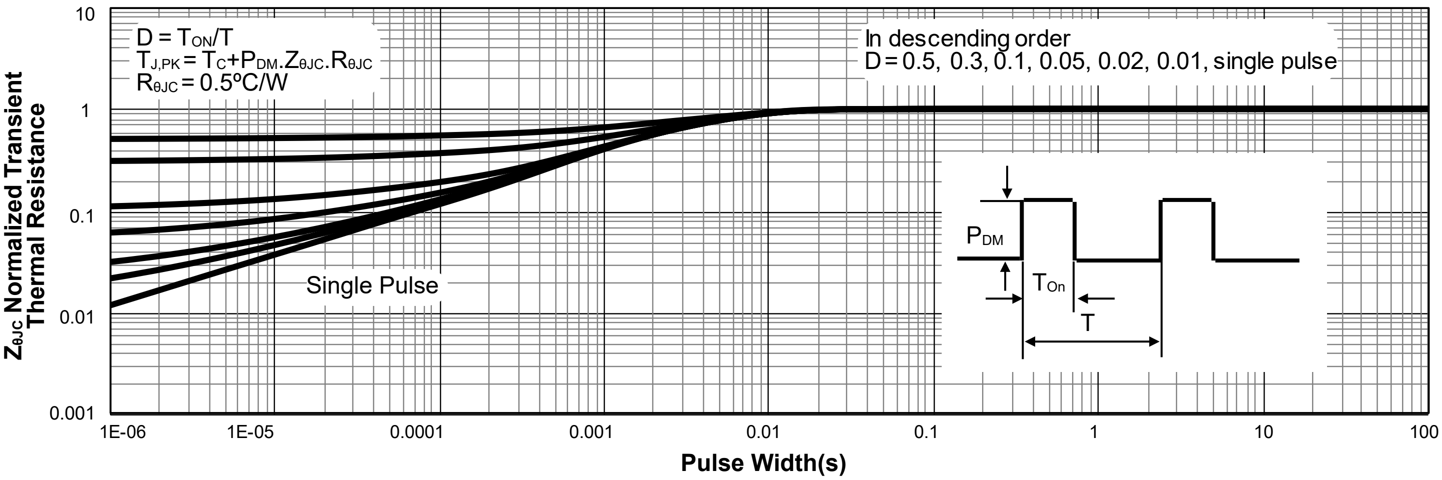


Figure 18. Normalized Maximum Transient Thermal Impedance for AOK033V120X2Q (Note I)

Test Circuits and Waveforms

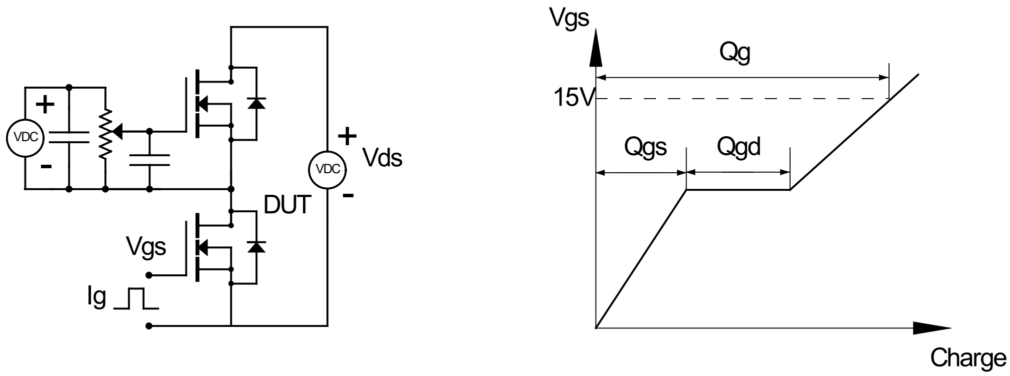


Figure 19. Gate Charge Test Circuits and Waveforms

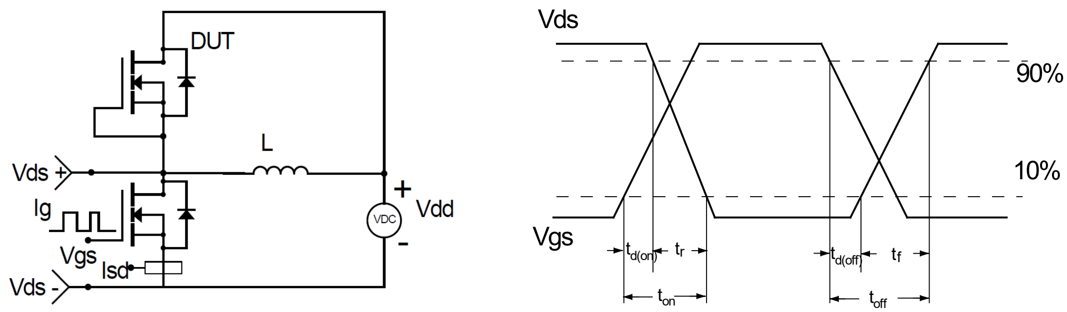


Figure 20. Inductive Switching Test Circuit and Waveforms

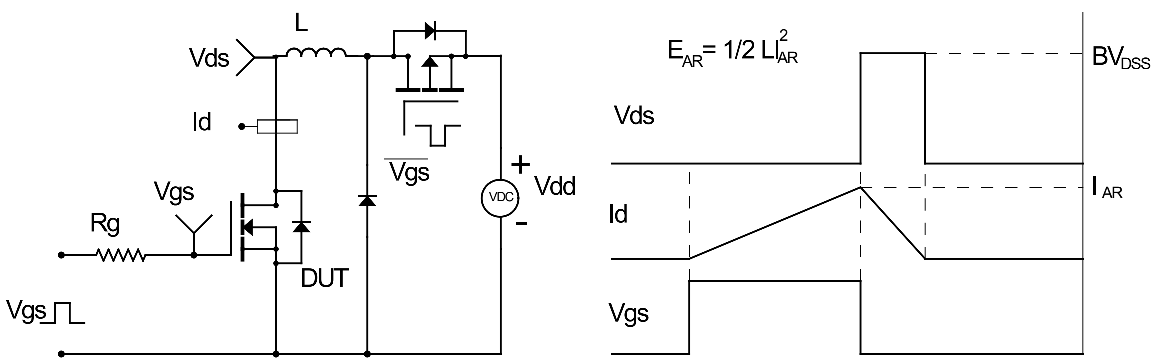


Figure 21. Unclamped Inductive Switching (UIS) Test Circuit and Waveforms

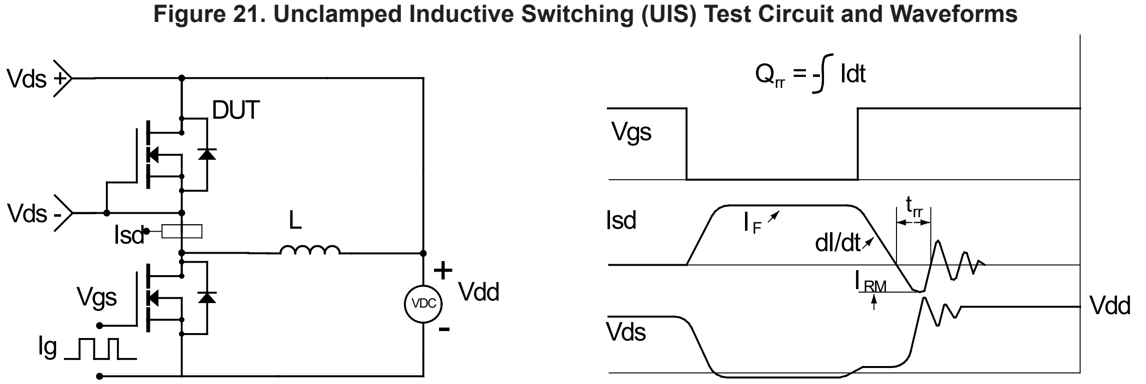
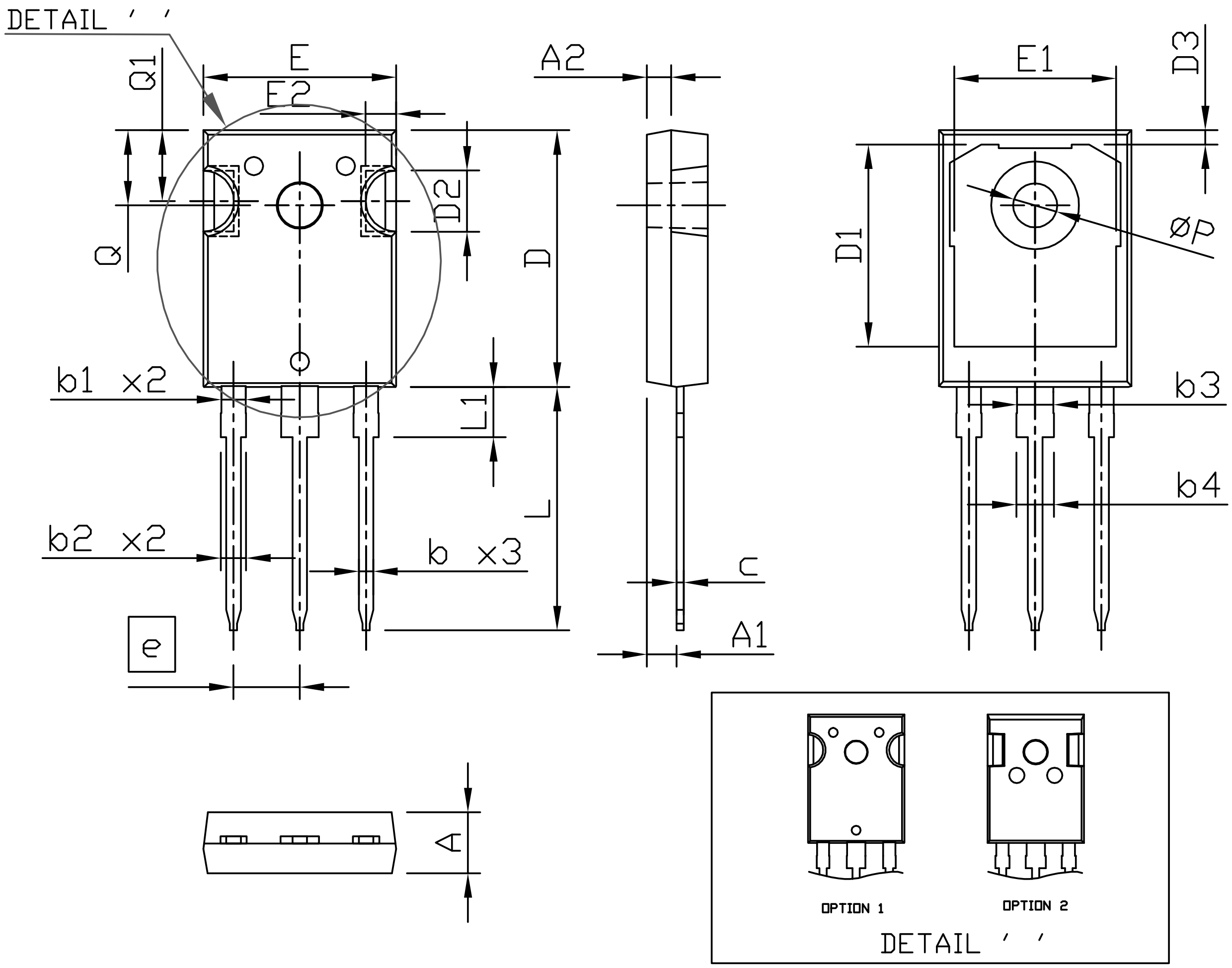
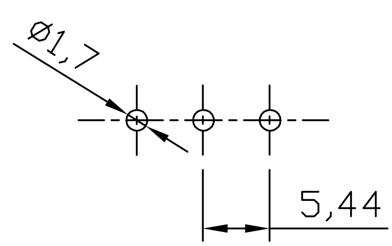


Figure 22. Diode Recovery Test Circuits and Waveforms

Package Dimensions, TO-247-3L



RECOMMENDED LAND PATTERN

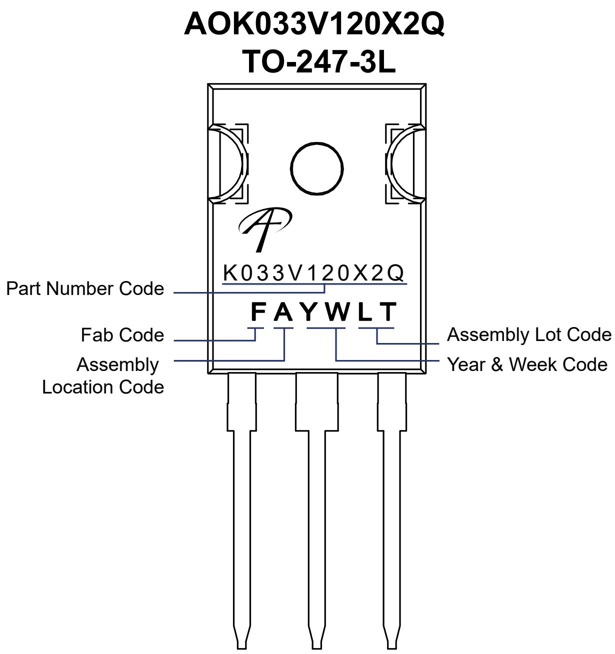


UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.90	5.00	5.10	0.193	0.197	0.201
A1	2.31	2.42	2.52	0.091	0.095	0.099
A2	1.90	2.00	2.10	0.075	0.079	0.083
b	1.16	1.22	1.27	0.046	0.048	0.050
b1	1.96	2.02	2.07	0.078	0.080	0.081
b2	2.00	2.10	2.20	0.079	0.083	0.087
b3	2.96	3.02	3.07	0.117	0.119	0.121
b4	3.00	3.10	3.20	0.118	0.122	0.126
c	0.59	0.62	0.66	0.023	0.024	0.026
D	20.90	21.00	21.10	0.823	0.827	0.831
D1	16.25	16.55	16.85	0.640	0.652	0.663
D2		5.00 TYP			0.197 TYP	
D3	1.05	1.20	1.35	0.041	0.047	0.053
e		5.44 BSC			0.214 BSC	
E	15.70	15.80	15.90	0.618	0.622	0.626
E1	13.06	13.26	13.50	0.514	0.522	0.530
E2		2.50 TYP			0.098 TYP	
L	19.72	19.92	20.12	0.776	0.784	0.792
L1	---	---	4.30	---	---	0.169
Q		6.15 BSC			0.242 BSC	
Q1	5.60	5.80	6.00	0.220	0.228	0.236
ØP	3.55	3.60	3.70	0.140	0.142	0.146

NOTE
1. PAKCAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Part Marking



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