

### General Description

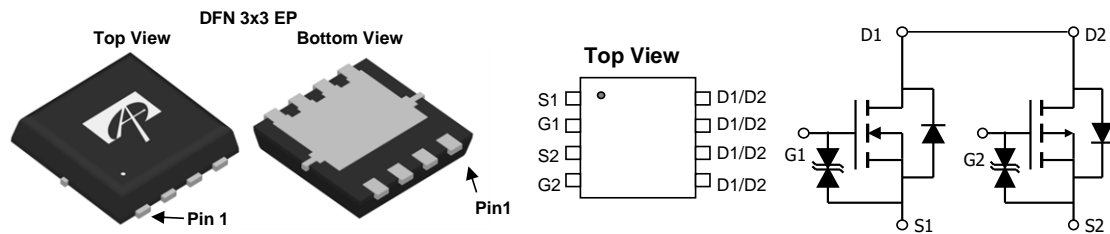
The AONR26309A uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used in inverter and other applications.

### Product Summary

N-channel	P-channel	
$V_{DS} (V) = 30V$	$V_{DS} (V) = -30V$	
$I_D = 14A$	$I_D = -21A$	( $V_{GS} = \pm 10V$ )
$R_{DS(ON)} < 20m\Omega$	$R_{DS(ON)} < 32m\Omega$	( $V_{GS} = \pm 10V$ )
$R_{DS(ON)} < 26m\Omega$	$R_{DS(ON)} < 55m\Omega$	( $V_{GS} = \pm 4.5V$ )

ESD protection

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max N-channel	Max P-channel	Units
Drain-Source Voltage	$V_{DS}$	30	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	14	A
		$T_C=100^\circ C$	9	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	35	-44	A
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	$T_A=25^\circ C$	6.5	W
		$T_A=70^\circ C$	5	
Avalanche Current <sup>C</sup>	$I_{AR}$	15	-20	A
Repetitive avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AR}$	11	20	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	7	W
		$T_C=100^\circ C$	2.8	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ C$	1.5	W
		$T_A=70^\circ C$	0.9	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	-55 to 150	$^\circ C$

### Thermal Characteristics: N-channel

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10s$	40	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	70	$^\circ C/W$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	15	18	$^\circ C/W$

### Thermal Characteristics: P-channel

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10s$	40	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	70	$^\circ C/W$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	5	6	$^\circ C/W$

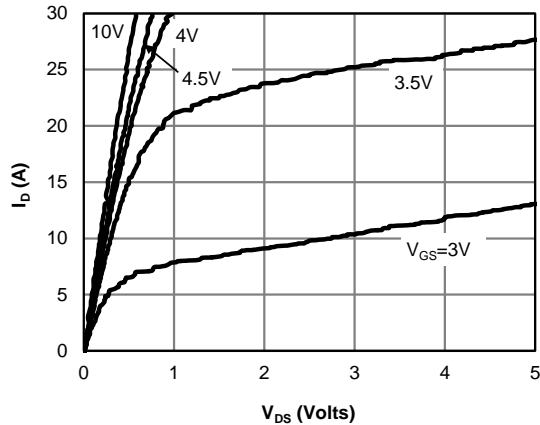
**N-channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.3	1.8	2.3	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =6.5A T <sub>J</sub> =125°C		16 24	20 30	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =6A		20	26	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =6.5A		33		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		600		pF
C <sub>oss</sub>	Output Capacitance			70		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			60		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1.2	2.4	3.6	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =6.5A		12	20	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			6	12	nC
Q <sub>gs</sub>	Gate Source Charge			2.2		nC
Q <sub>gd</sub>	Gate Drain Charge			2.5		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =2.307Ω, R <sub>GEN</sub> =3Ω		4.5		ns
t <sub>r</sub>	Turn-On Rise Time			4		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			20		ns
t <sub>f</sub>	Turn-Off Fall Time			4		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =6.5A, di/dt=500A/μs		5		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =6.5A, di/dt=500A/μs		6		nC

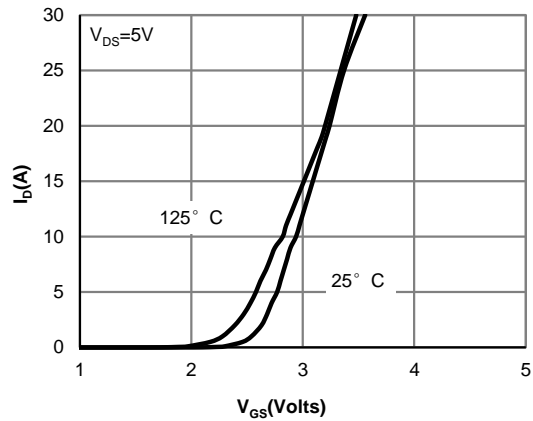
- A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.
- B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.
- D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C.
- G. The maximum current rating is limited by bond-wires.
- H. These tests are performed with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The SOA curve provides a single pulse rating.

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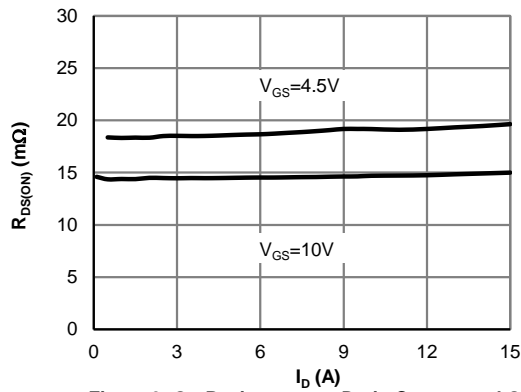
**N-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



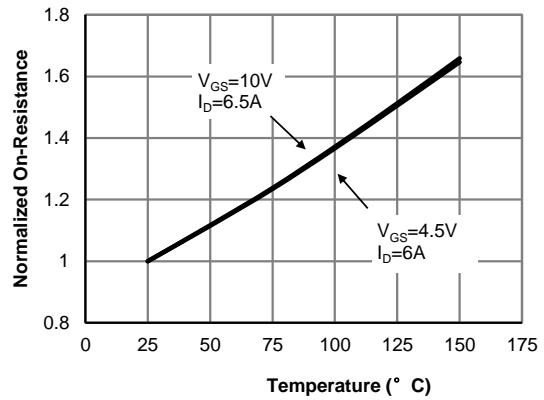
**Figure 1: On-Region Characteristics (Note E)**



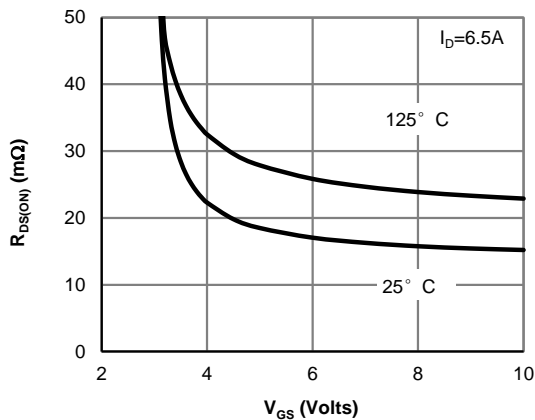
**Figure 2: Transfer Characteristics (Note E)**



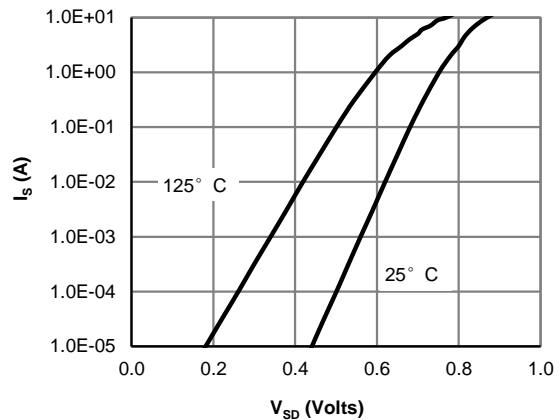
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

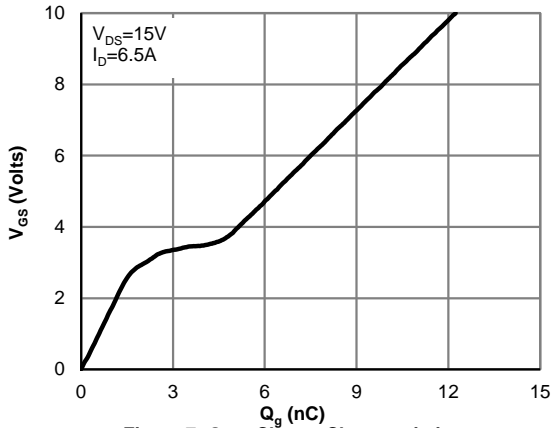


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

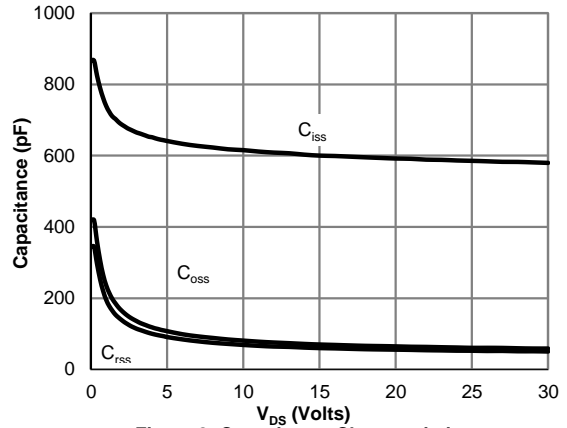


**Figure 6: Body-Diode Characteristics (Note E)**

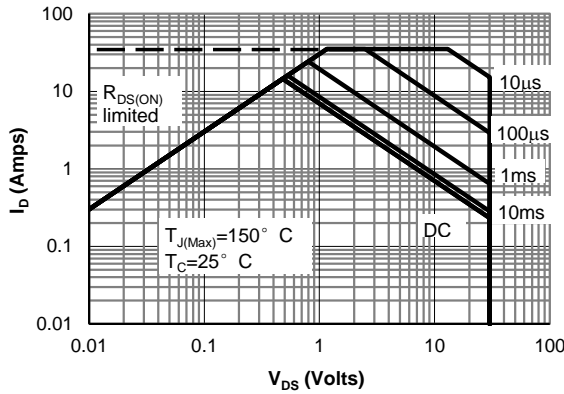
**N-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



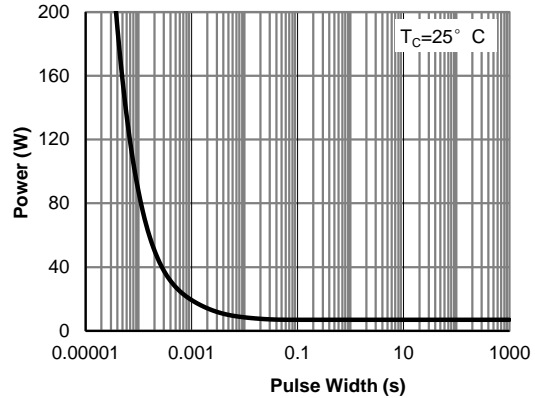
**Figure 7: Gate-Charge Characteristics**



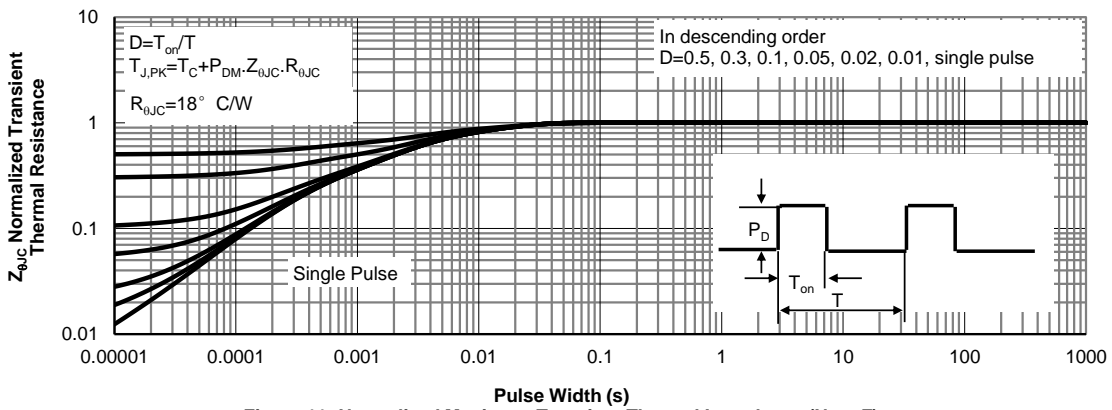
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**N-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

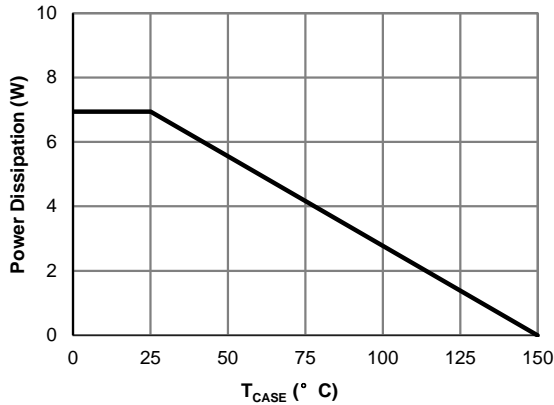


Figure 12: Power De-rating (Note F)

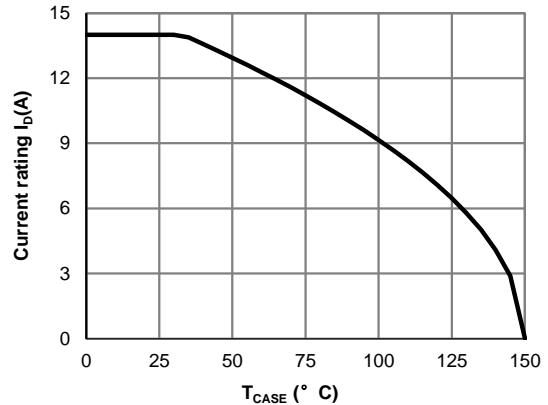


Figure 13: Current De-rating (Note F)

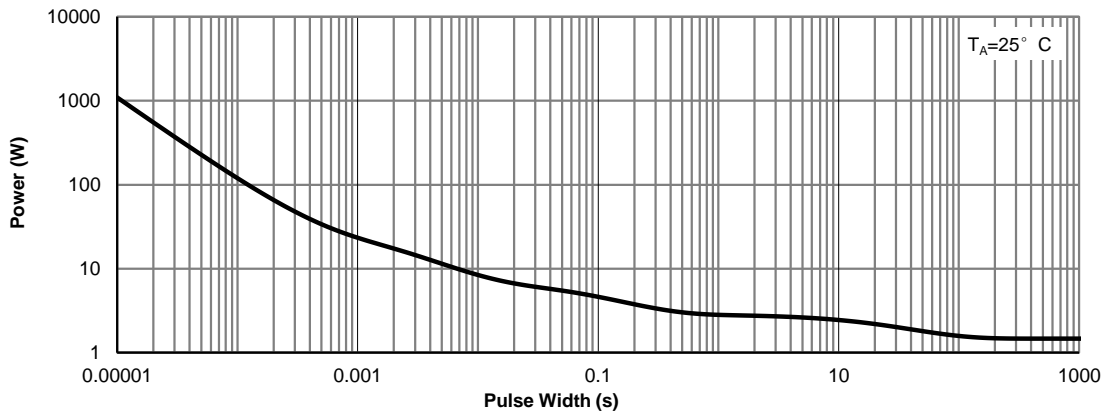


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

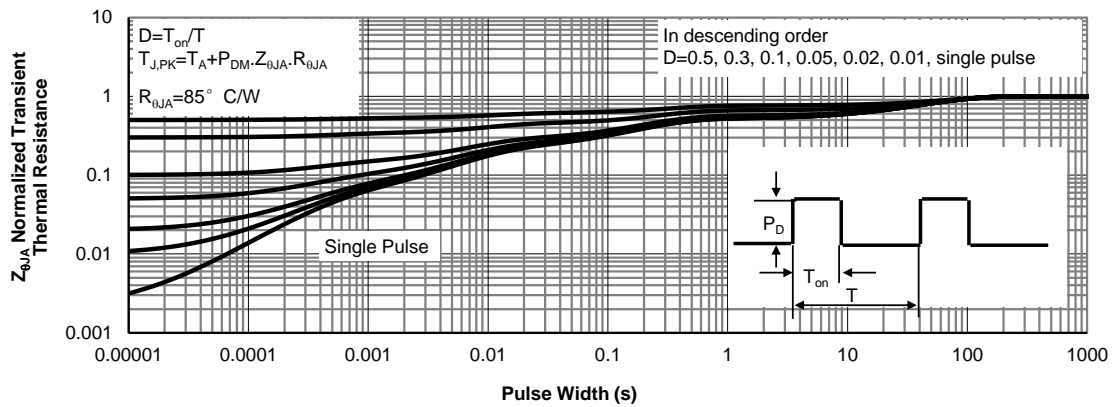
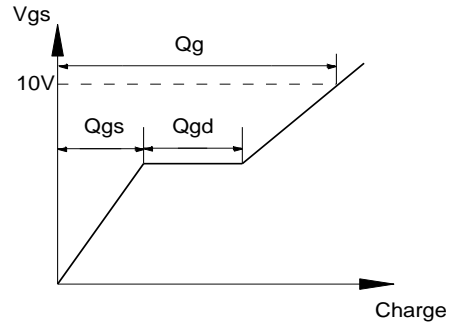
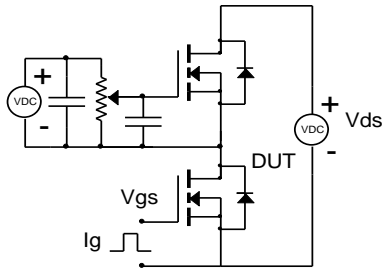
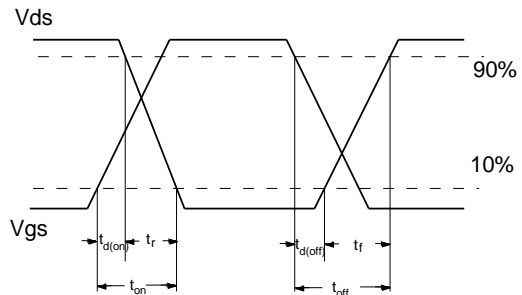
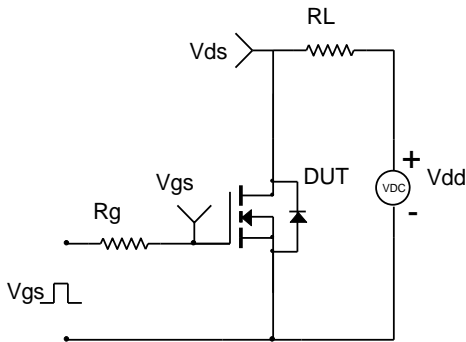


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

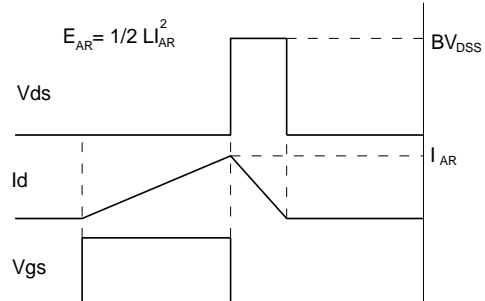
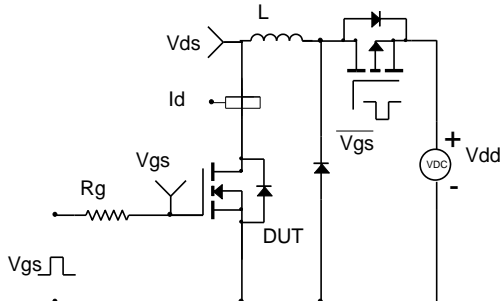
**Gate Charge Test Circuit & Waveform**



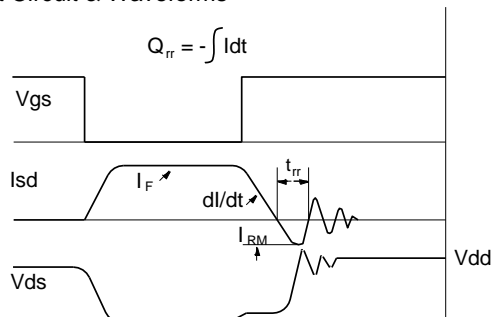
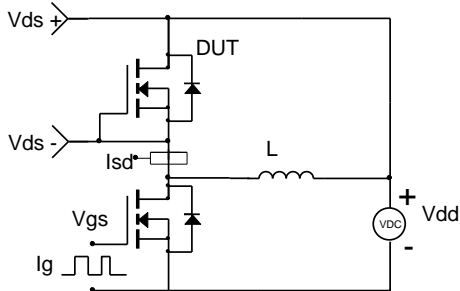
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



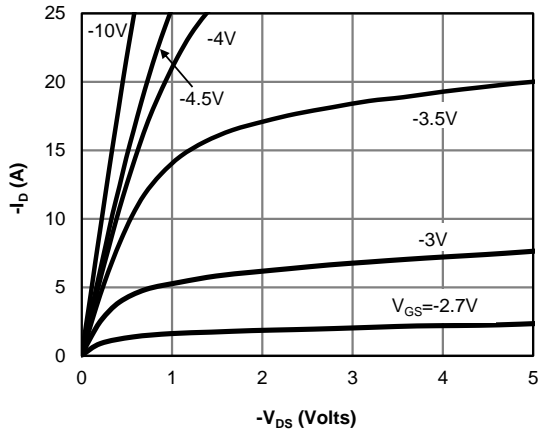
**P-channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±10	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.2	-1.7	-2.2	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-5.7A T <sub>J</sub> =125°C		25 32	32 41	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4.4A		35	55	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-5.7A		17		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.8	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-2	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz		1100		pF
C <sub>oss</sub>	Output Capacitance			120		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			105		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		11	18	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-5.7A		22	33	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			11	18	nC
Q <sub>gs</sub>	Gate Source Charge			2.5		nC
Q <sub>gd</sub>	Gate Drain Charge			6.5		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =2.63Ω, R <sub>GEN</sub> =3Ω		12		ns
t <sub>r</sub>	Turn-On Rise Time			9		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			55		ns
t <sub>f</sub>	Turn-Off Fall Time			19		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time		I <sub>F</sub> =-5.7A, di/dt=500A/μs		12	
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-5.7A, di/dt=500A/μs		17		nC

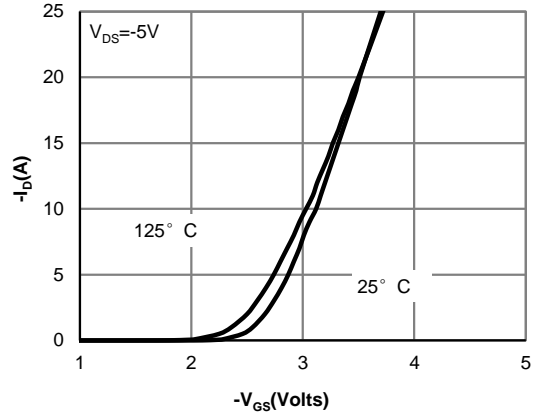
- A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.
- B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.
- D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C.
- G. The maximum current rating is limited by bond-wires.
- H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The SOA curve provides a single pulse rating.

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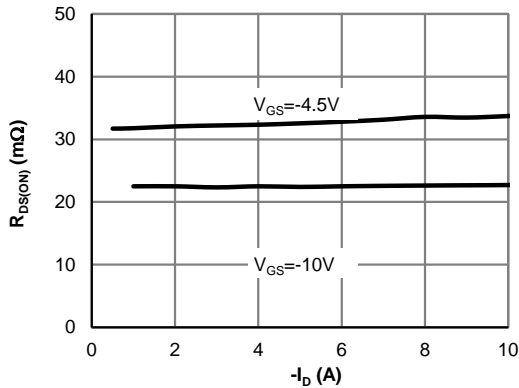
**P-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



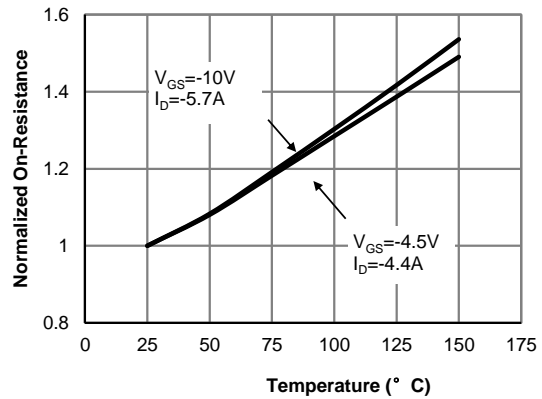
**Figure 1: On-Region Characteristics (Note E)**



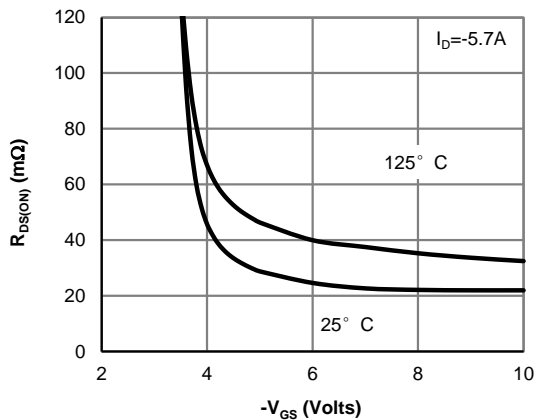
**Figure 2: Transfer Characteristics (Note E)**



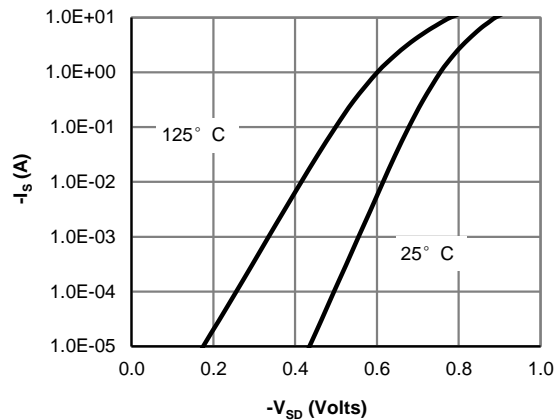
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



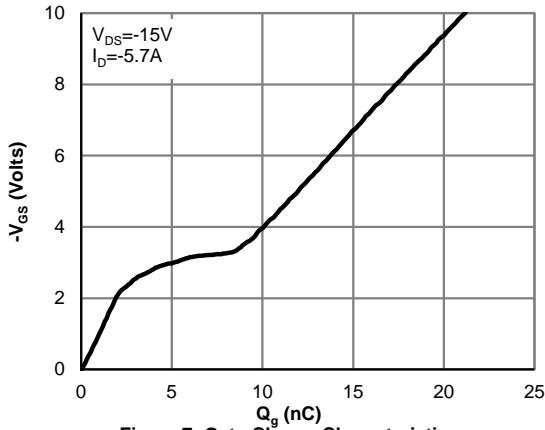
**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



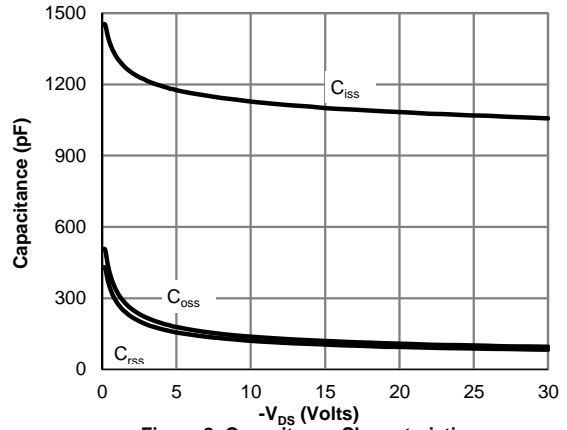
**Figure 6: Body-Diode Characteristics (Note E)**



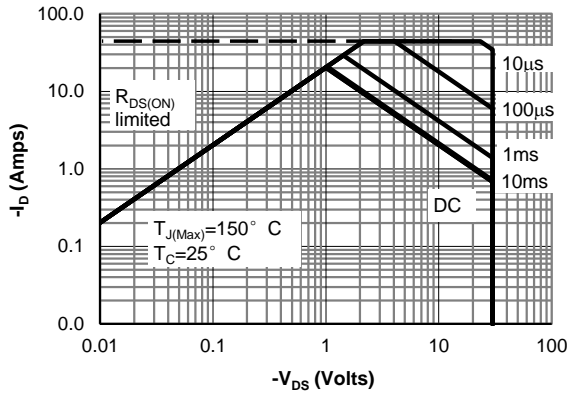
**P-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



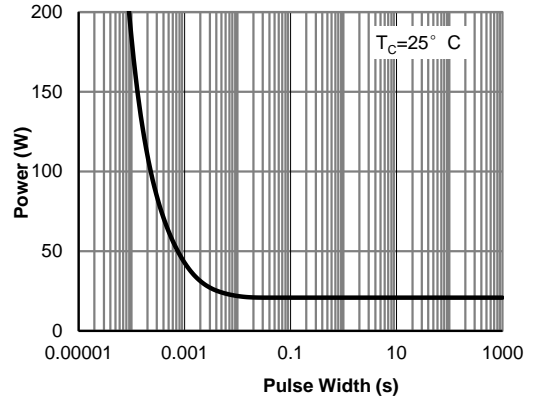
**Figure 7: Gate-Charge Characteristics**



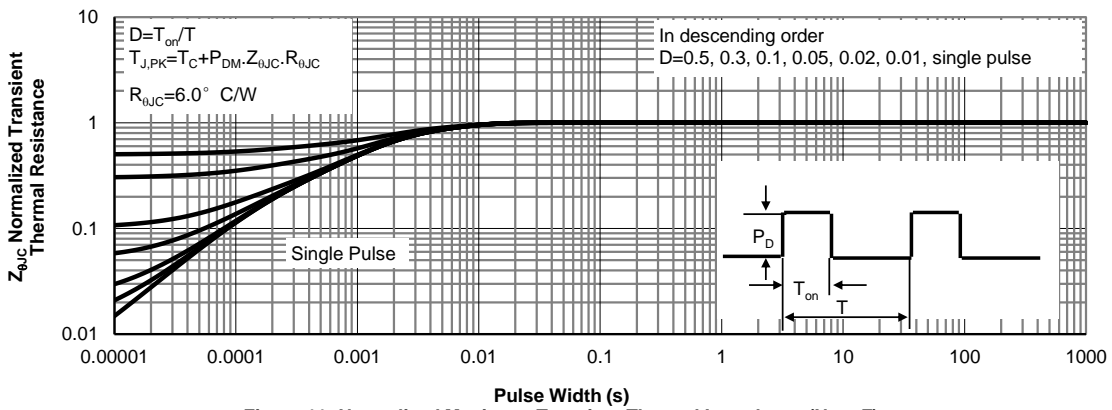
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**P-channel TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

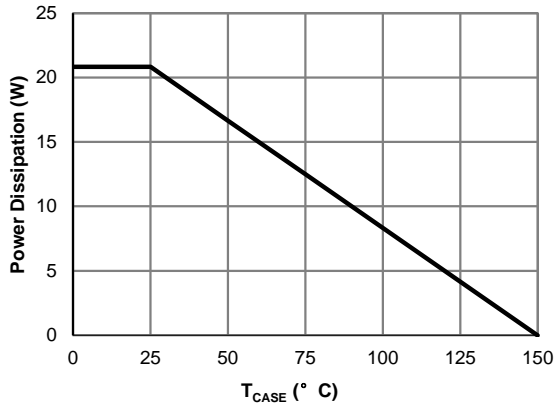


Figure 12: Power De-rating (Note F)

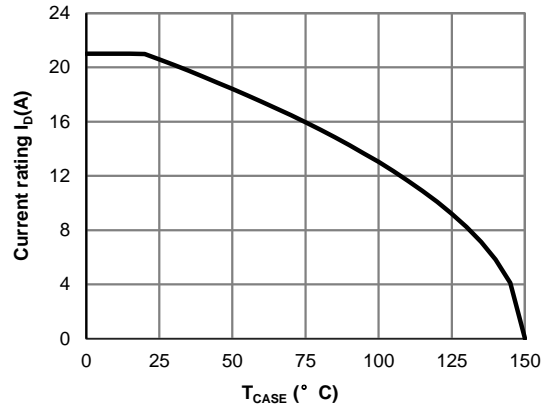


Figure 13: Current De-rating (Note F)

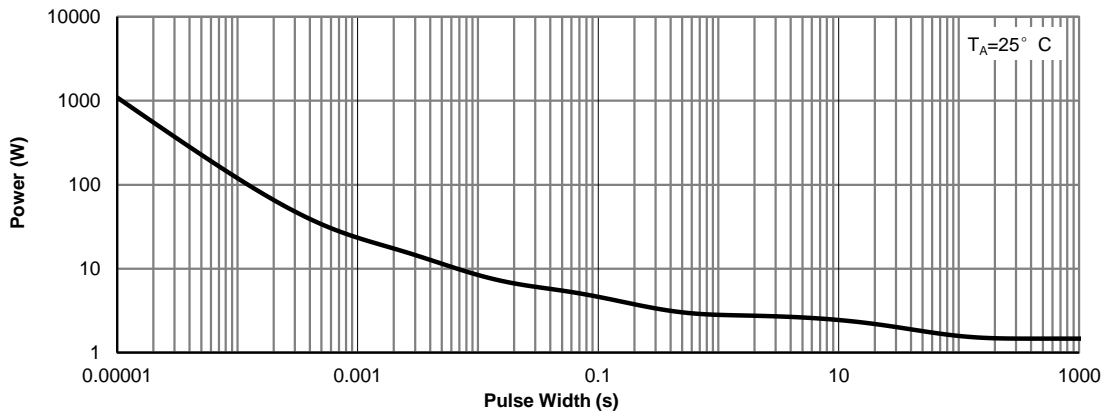


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

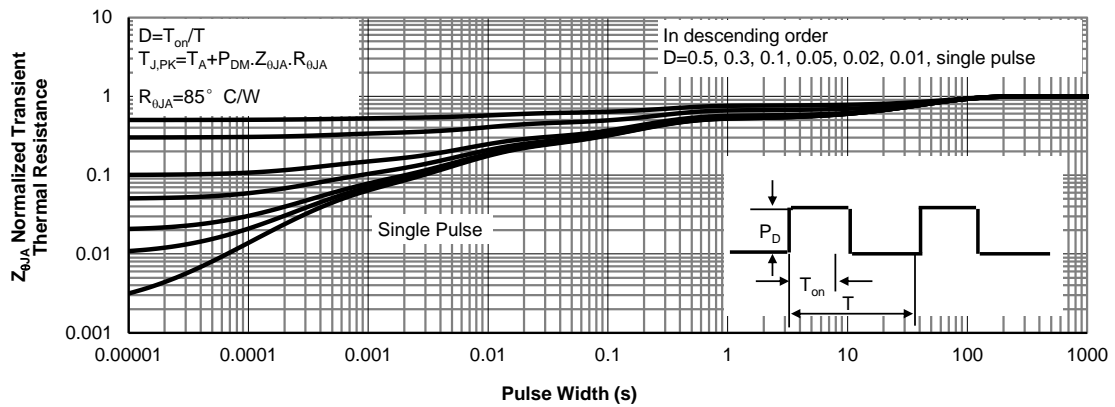
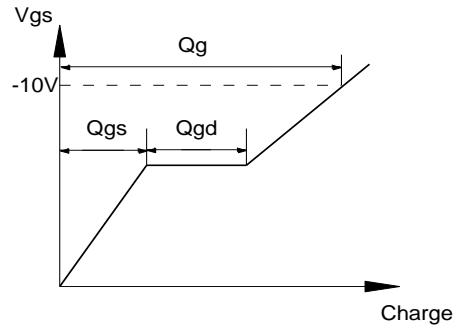
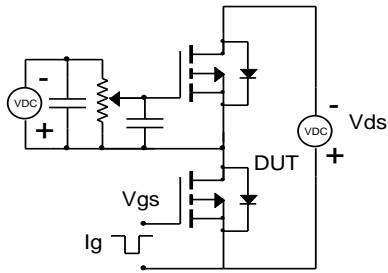
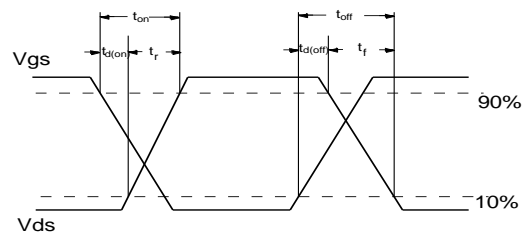
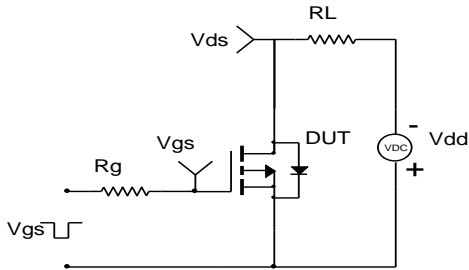


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

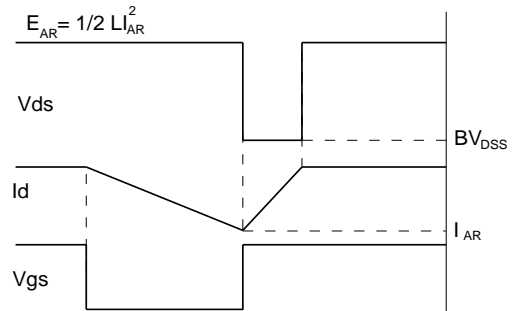
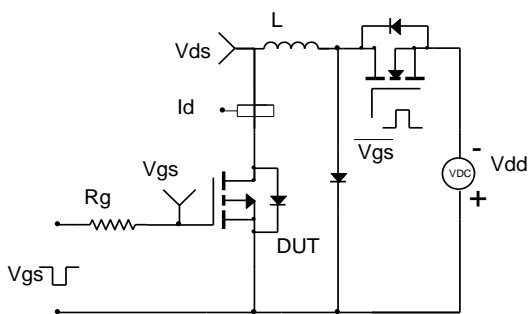
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

