ALPHA & OMEGA SEMICONDUCTOR

AONS1R6A70

700V, aMOS™ N-Channel Power Transistor

General Description

- Proprietary αMOS5™ technology
- Low $R_{DS(ON)}$
- Optimized switching parameters for better EMI performance
- Enhanced body diode for robustness and fast reverse recovery

Applications

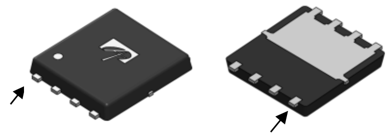
- Flyback for SMPS
- Charger, Adapter, lighting

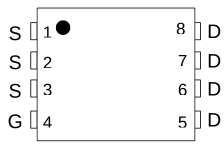
Product Summary

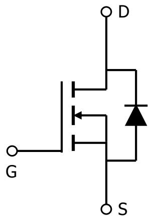
V_{DS} @ $T_{j,max}$	800V
I_{DM}	15A
$R_{DS(ON),max}$	< 1.6Ω
$Q_{g,typ}$	7.4nC
E_{oss} @ 400V	1μJ

100% UIS Tested
100% R_g Tested

DFN5x6F







Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS1R6A70	DFN5X6F	Tape&Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	700	V
Gate-Source Voltage		V_{GS}	±20	V
Gate-Source Voltage (dynamic) AC(f>1Hz)		V_{GS}	±30	V
Continuous Drain Current	T_C=25°C	I_D	4.6	A
	T_C=100°C		3	
Pulsed Drain Current C		I_{DM}	15	
Continuous Drain Current	T_A=25°C	I_{DSM}	1.1	A
	T_A=70°C		0.9	
Avalanche Current C	L=1mH	I_{AR}	1.1	A
Repetitive avalanche energy C		E_{AR}	0.6	mJ
Single pulsed avalanche energy G		E_{AS}	2.7	mJ
MOSFET dv/dt ruggedness		dv/dt	100	V/ns
Peak diode recovery dv/dt			20	
Power Dissipation B	T_C=25°C	P_D	78	W
	Derate above 25°C		0.6	W/°C
Power Dissipation A	T_A=25°C	P_{DSM}	4.1	W
	T_A=70°C		2.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient A	t ≤ 10s	$R_{\theta JA}$	25	30	°C/W
Maximum Junction-to-Ambient A D	Steady-State		45	55	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.2	1.6	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V, T_J=25°C	700			V
		I_D=250µA, V_{GS}=0V, T_J=150°C		800		
BV_{DSS} /∆TJ	Breakdown Voltage Temperature Coefficient	I_D=250µA, V_{GS}=0V		0.61		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=700V, V_{GS}=0V			1	µA
		V_{DS}=560V, T_J=125°C			10	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=5V, I_D=250µA	2.9	3.5	4.1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=1A		1.3	1.6	Ω
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=1.9A		3		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.81	1.2	V
I_S	Maximum Body-Diode Continuous Current				4.6	A
I_{SM}	Maximum Body-Diode Pulsed Current [C]				15	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz		354		pF
C_{oss}	Output Capacitance			12		pF
$C_{o(er)}$	Effective output capacitance, energy related [I]	V_{GS}=0V, V_{DS}=0 to 480V, f=1MHz		11		pF
$C_{o(tr)}$	Effective output capacitance, time related [J]			46		pF
C_{rss}	Reverse Transfer Capacitance	V_{GS}=0V, V_{DS}=100V, f=1MHz		1.3		pF
R_g	Gate resistance	f=1MHz		7.3		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=10V, V_{DS}=480V, I_D=1.9A		7.4		nC
Q_{gs}	Gate Source Charge			2.9		nC
Q_{gd}	Gate Drain Charge			2		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=400V, I_D=1.9A, R_G=5Ω		15		ns
t_r	Turn-On Rise Time			7.5		ns
$t_{D(off)}$	Turn-Off DelayTime			32		ns
t_f	Turn-Off Fall Time			13.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=1.9A, di/dt=100A/µs, V_{DS}=400V		176		ns
I_{rm}	Peak Reverse Recovery Current			11		A
Q_{rr}	Body Diode Reverse Recovery Charge			1.4		µC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. L=60mH, I_{AS}=0.3 A, R_G=25Ω, Starting T_J=25° C.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.
I. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS.}$
J. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS.}$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

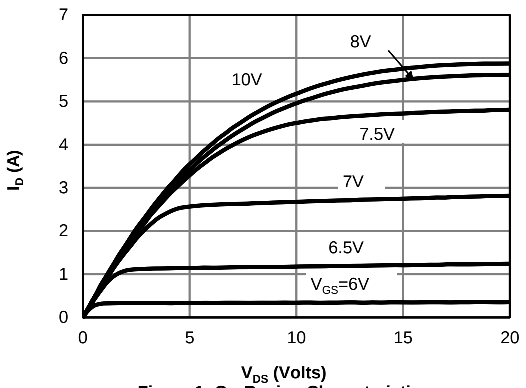


Figure 1: On-Region Characteristics

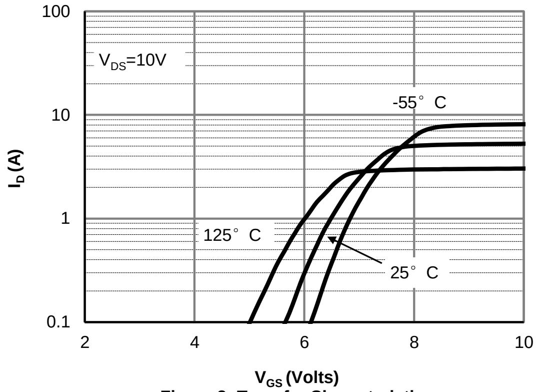


Figure 2: Transfer Characteristics

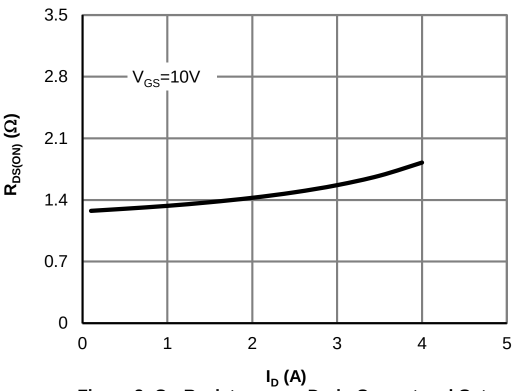


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

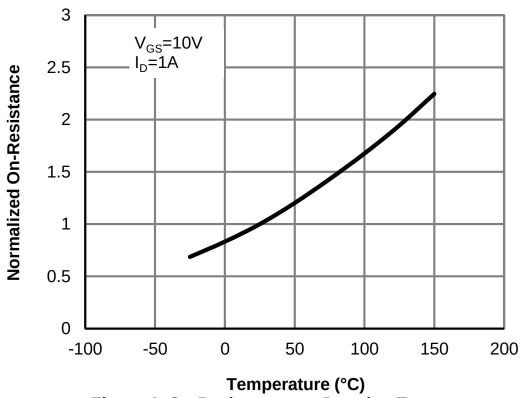


Figure 4: On-Resistance vs. Junction Temperature

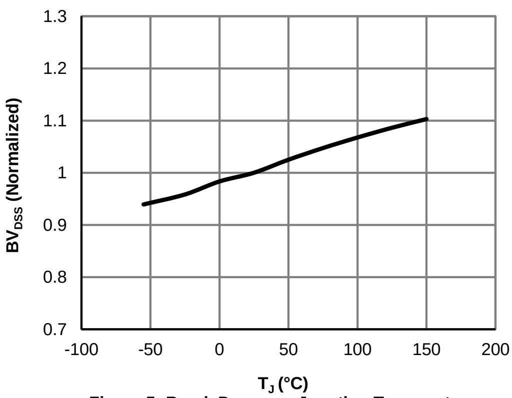


Figure 5: Break Down vs. Junction Temparature

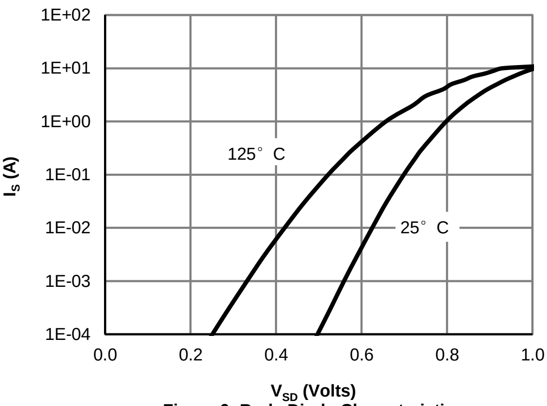


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

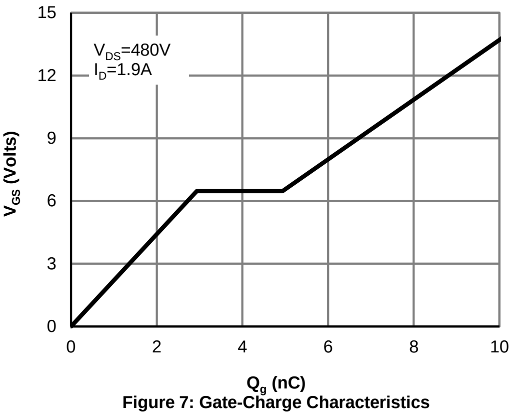


Figure 7: Gate-Charge Characteristics

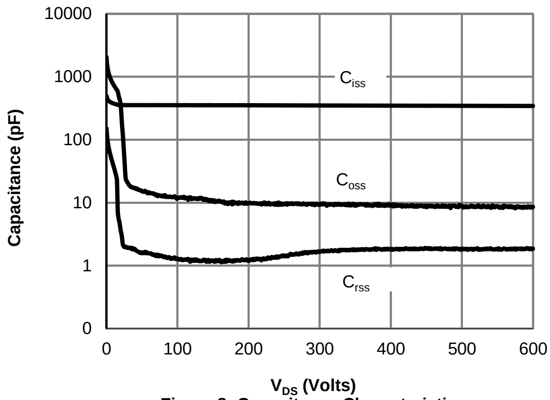


Figure 8: Capacitance Characteristics

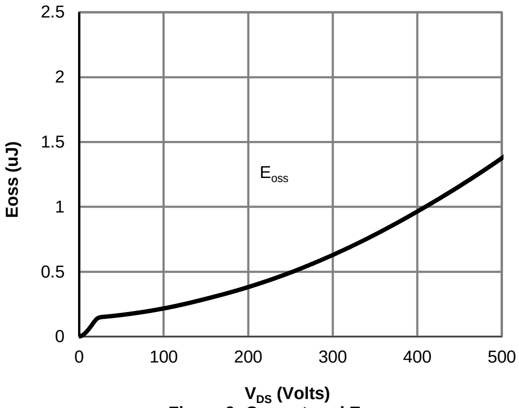


Figure 9: Coss stored Energy

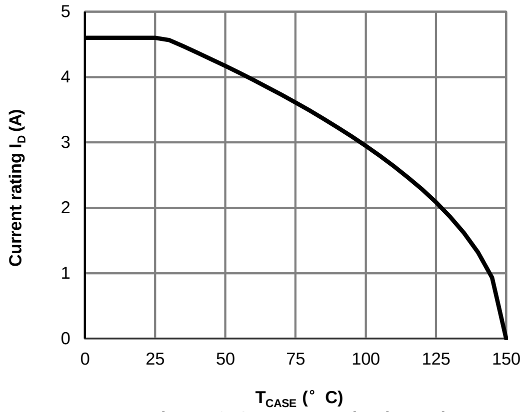


Figure 10: Current De-rating (Note F)

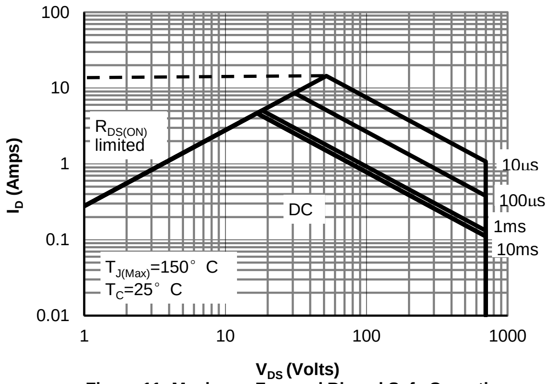


Figure 11: Maximum Forward Biased Safe Operating Area (Note F)

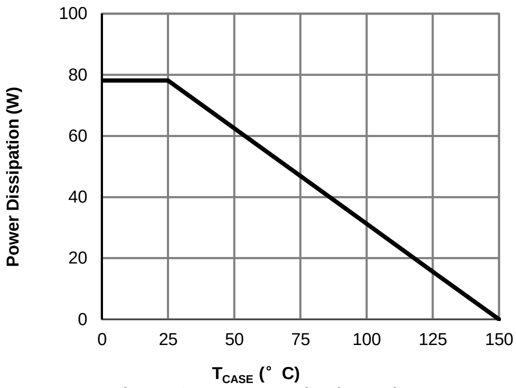


Figure 12: Power De-rating (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

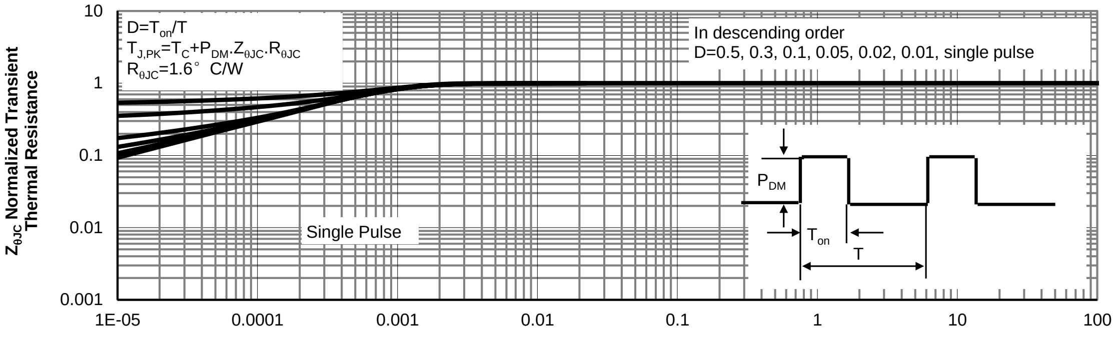


Figure 13: Normalized Maximum Transient Thermal Impedance (Note F)

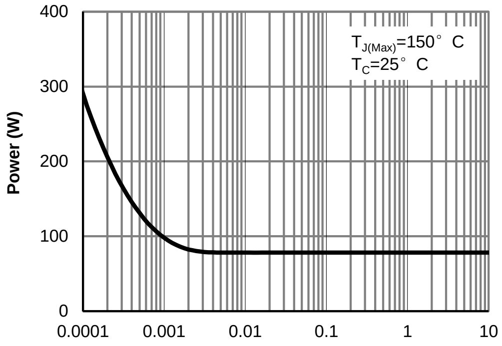


Figure 14: Single Pulse Power Rating Junction-to-Case (Note F)

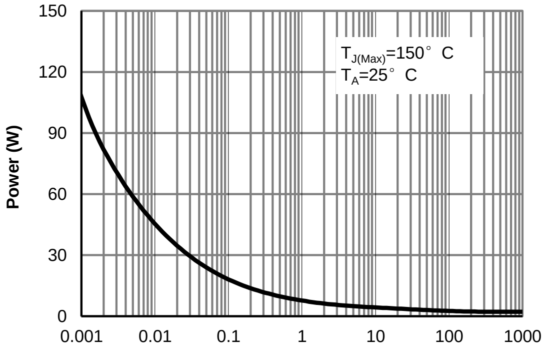


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

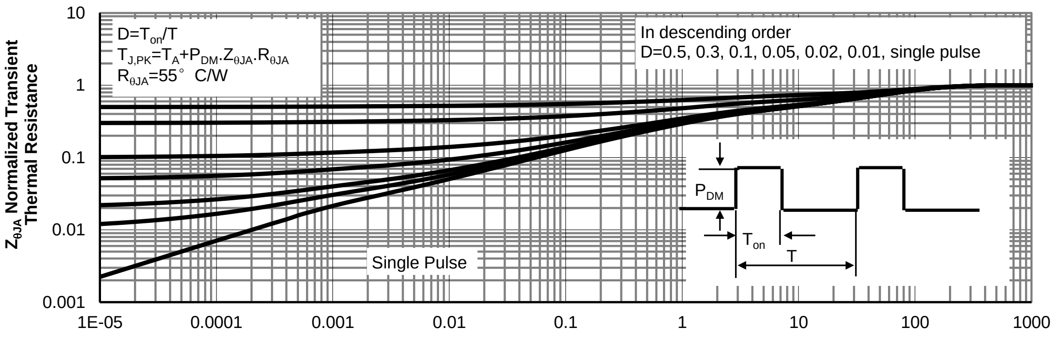
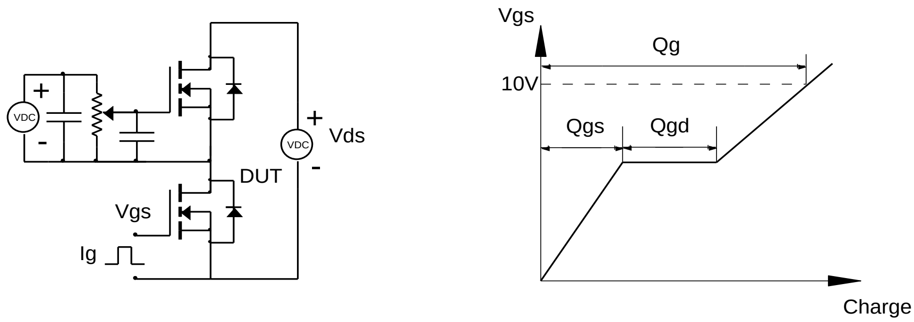
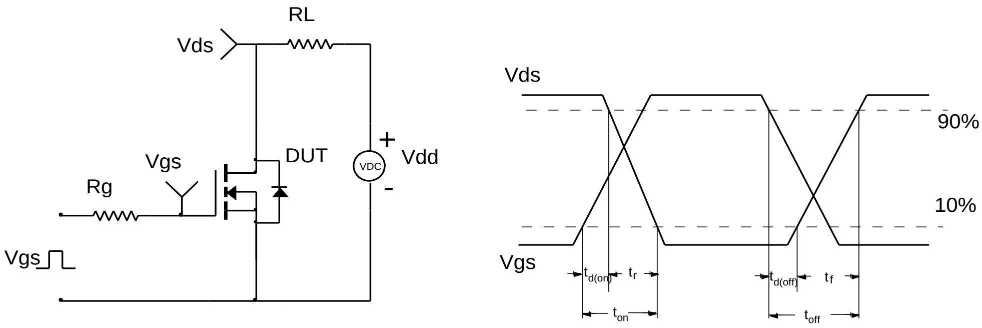


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

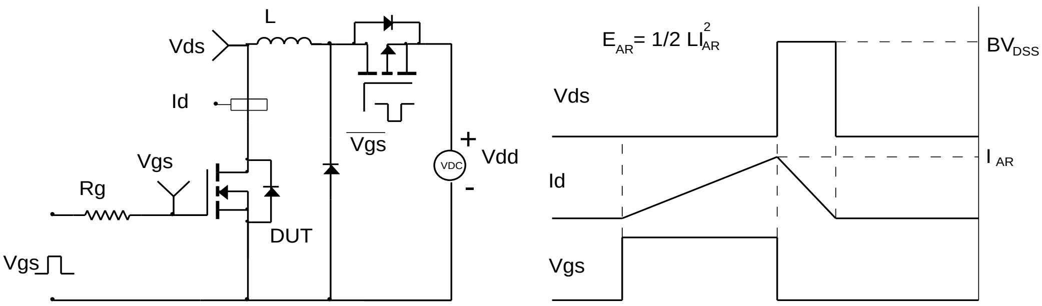
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms