AOZ32103MQV-06

60V, Three-Phase Motor Driver

General Description

The AOZ32103MQV-06 is a high performance three-phase motor driver. It is able to drive three half-bridges consisting of six N-channel power MOSFETs for three-phase application.

AOZ32103MQV-06 has a very low shutdown current (<1µA) when nSLEEP pin is low, which is very suitable for portable products. Built-in trickle charge pump allows the high side driver output to maintain a high level. It also has a built-in current amplifier, which can be used to feed back the total current of the system. The device features multiple protection functions such as internal safety features including shoot-through protection, adjustable dead-time control, VDD under voltage protection and over temperature protection, and has a reporting mechanism.

The AOZ32103MQV-06 is available in a 5mm x 4mm QFN-28L package and is rated over a -40ºC to +125ºC ambient temperature range.

Features

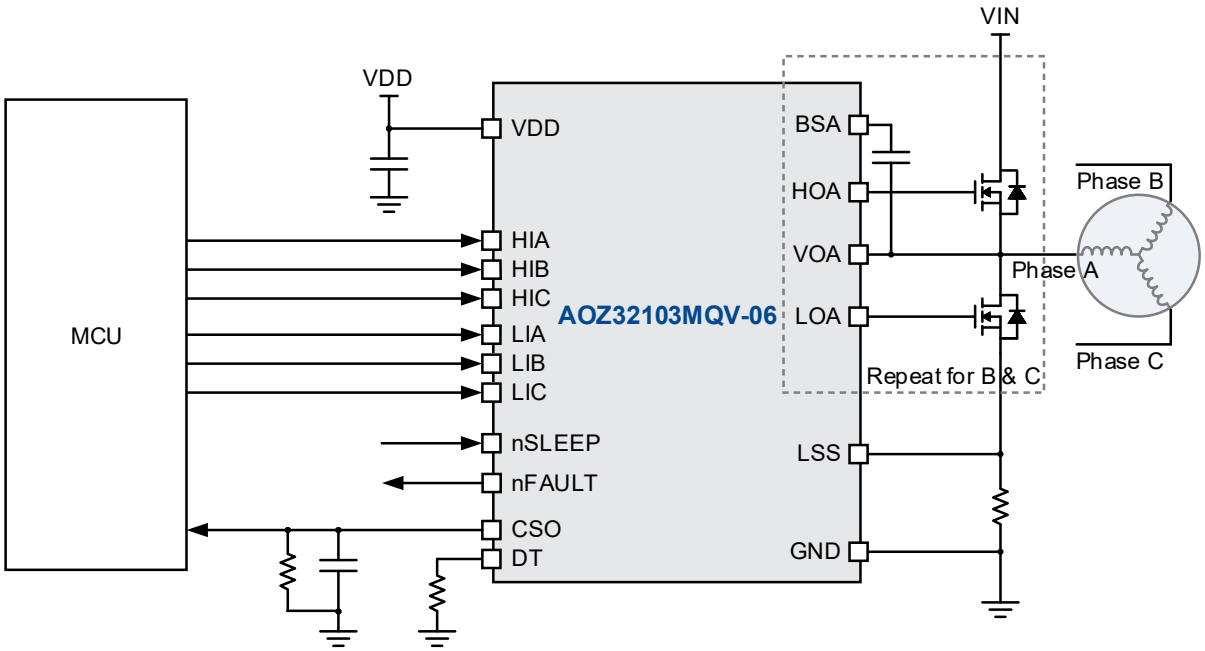
- Support 60V input voltage range
- 0.8A source and 1A sink current capability
- Integrated bootstrap circuit and 70V V_{BST} maximum voltage
- Trickle charge pump support 100% PWM duty cycling when VDD>11V
- Integrated current sense amplifier to feedback the total current
- Adjustable dead-time control to prevent shoot-through
- Sleep mode for power saving of battery powered application
- Thermal shutdown and VDD UVLO protection
- Fault indication output

Applications

- Brushless DC motors and permanent magnet synchronous motors
- Fans and pumps
- Power tools
- E-bike

GREEN Product

Typical Application (3 Phase Motor)



Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ32103MQV-06	-40 °C to +125 °C	QFN5x4-28L	Green

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

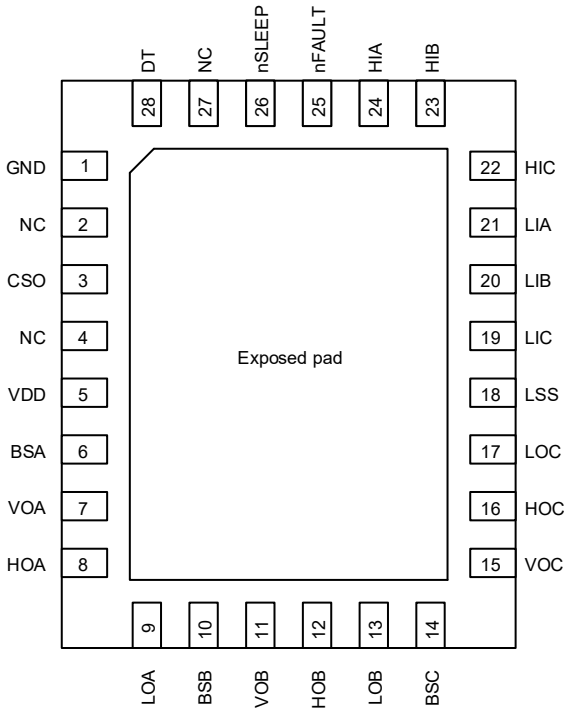


Figure 1. QFN5x4-28L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	GND	Ground.
2	NC	No connection.
3	CSO	Current sense output.
4	NC	No connection.
5	VDD	Gate driver supply voltage.
6	BSA	Bootstrap output, phase A.
7	VOA	High-side source connection phase A.
8	HOA	High-side gate driver output, phase A.
9	LOA	Low-side gate driver output, phase A.
10	BSB	Bootstrap output, phase B.
11	VOB	High-side source connection phase B.
12	HOB	High-side gate driver output, phase B.
13	LOB	Low-side gate driver output, phase B.
14	BSC	Bootstrap output, phase C.
15	VOC	High-side source connection phase C.
16	HOC	High-side gate driver output, phase C.
17	LOC	Low-side gate driver output, phase C.
18	LSS	Low side source connection and this pin is also the current sense amplifier input.
19	LIC	Low-side gate driver input, phase C.
20	LIB	Low-side gate driver input, phase B.
21	LIA	Low-side gate driver input, phase A.
22	HIC	High-side gate driver input, phase C.
23	HIB	High-side gate driver input, phase B.
24	HIA	High-side gate driver input, phase A.
25	nFAULT	Fault indication. Open-drain output. Logic low when in a fault state.
26	nSLEEP	Sleep mode set pin. Logic low to enter sleep mode, high to enable. Internal pull down.
27	NC	No connection.
28	DT	Dead-time set pin.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VDD to GND	-0.3 V to +14.5 V
BSA/B/C to GND	-0.3 V to +70 V
HOA/B/C	-0.3 V to (BSx(1)-VOx(1)) +0.3V
HOA/B/C (transient, 2µs)	-8 V to (BSx(1)-VOx(1)) +0.3V
VOA/B/C to GND	-5 V to +65 V
VOA/B/C to GND (transient, 2µs)	-8 V to +65 V
LOA/B/C to GND	-0.3 V to +14.5 V
LSS to GND	-0.3 V to +4 V
LSS to GND (transient, 2µs)	-1 V to +4 V
All other pins to GND	-0.3 V to +6.5 V
Junction Temperature (T_J)	+150 °C
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating	2 kV

Note:

1. x = A,B,C

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
DC bus Voltage (V_{IN})	8 V to 60 V
Input Voltage (VDD)	8.5 V to 14 V
Ambient Temperature (T_A)	-40 °C to +125 °C
Package Thermal Resistance (Θ_{JA}) (Θ_{JC})	 51 °C/W 7 °C/W

Electrical Characteristics

T_A = 25 °C, VDD = 12 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power Supply						
VDD	Gate Driver Supply Voltage		8.5		14	V
I_{QVDD}	Quiescent VDD Supply Current	nSLEEP = 1, gate no switching		2		mA
I_{SLEEP}	VDD supply current in sleep mode	nSLEEP = 0		1		µA
Logic Input (HIx, LIx, nSLEEP)						
V_{INH}	Logic “High” Input Voltage		2			V
V_{INL}	Logic “Low” Input Voltage				0.8	V
I_{INH}	Logic “High” Input Bias Current	V_{IH} = 5 V			14	µA
I_{INL}	Logic “Low” Input Bias Current	V_{IL} = 0.8 V			3	µA
$R_{SLEEP-PD}$	nSLEEP Pull-down Resistance			500		kΩ
R_{PD}	Internal Pull-down Resistance			500		kΩ

Electrical Characteristics *(Continued)*

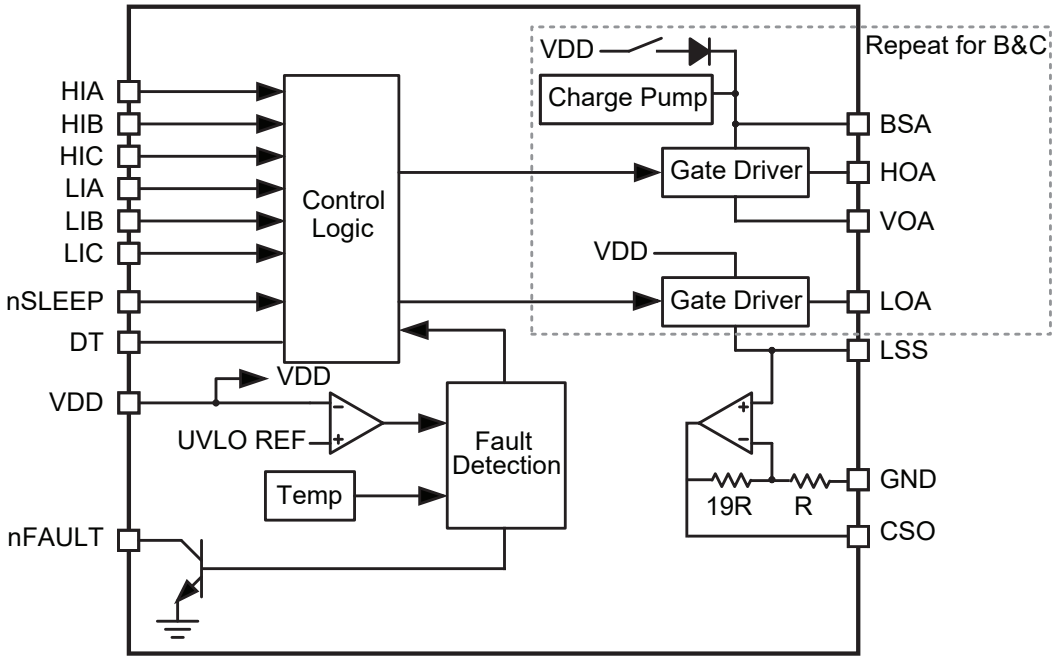
T_A = 25 °C, VDD = 12 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Bootstrap						
V_{F_BOOT}	Bootstrap Switch Forward Voltage	I_{F_BOOT} = 10 mA			2	V
		I_{F_BOOT} = 30 mA			3	
I_{F_LIMIT}	Bootstrap Current Limit	VF = 4 V		30		mA
Gate Driver						
I_{SOURCE} (2)	Maximum Source Current			0.8		A
I_{SINK} (2)	Maximum Sink Current			1		A
R_{UP}	Gate Drive Pull-up Resistance	VDS = 1 V		5		Ω
R_{HS-DN}	HS Gate Drive Pull-Down Resistance	VDS = 1 V	0.5		5.5	Ω
R_{LS-DN}	LS Gate Drive Pull-Down Resistance	VDS = 1 V	0.5		5.5	Ω
t_{HS_OFF}	High Side Minimum Off-time				900	ns
Dead Time						
T_{DEAD}	Dead Time	DT pin tied to GND		150		ns
		RDT = 1 kΩ		0.2		µs
		DT pin open		6		µs
Current Sense						
G	Gain of Amplifier	V_{LSS} = DC value, 50 mV to 200 mV		20		V/V
Protection Circuits						
VDD_{UVLO_R}	VDD UVLO Rising Threshold		6.9	7.8	8.6	V
VDD_{UVLO_F}	VDD UVLO Falling Threshold		6	6.8	7.6	V
VDD_{HYS}	VDD UVLO Hysteresis			1		V
VBS_{UVLO_R}	VBS Rising UVLO Threshold	Voltage between BSx and VOx		7.6		V
VBS_{UVLO_F}	VBS Falling UVLO Threshold	Voltage between BSx and VOx		6.9		V
t_{SLEEP}	SLEEP Wake-up Time			90		µs
T_{OTP}	Thermal Shutdown Temperature			150		°C
Fault Output (Open-Drain Output)						
V_{OL}	Output Low Voltage	IO = 5 mA			0.1	V
I_{OH}	Output High Leakage Current	VO = 5V			1	µA

Note:

2. Guaranteed by design.

Functional Block Diagram



Detailed Description

VDD Power Up and UVLO

In order to ensure the normal operation of the gate driver, if the nSLEEP pin is pulled high (normal working state), the gate driver will not work before VDD is higher than the UVLO rising threshold (about 7.6V). AOZ32103MQV-06 pulls the nFAULT pin low, and the report is now undervoltage protection state, until VDD>7.6V, nFAULT pin is pulled high, the gate driver can work normally.

When VDD drops to the UVLO falling threshold (about 6.8V), the gate driver stops working, and the nFAULT pin is pulled low.

Bootstrap Circuit and Charge Pump

Different from the traditional bootstrap architecture, in addition to the diode on the bootstrap path, AOZ32103MQV also adds a switch (S1) to limit the current. When the charging current exceeds 30mA, it is limited to 30mA. The purpose is to limit the large current of the bootstrap charging moment. In addition, if the charging current is too large, the reverse recover current of the diode will also be too large. The above two reasons may cause damage to the circuit, so the current limiting function can effectively protect the bootstrap diode.

When the high side remains high for a long time, the bootstrap capacitor slowly discharges. In order to maintain the bootstrap (BSx) voltage, AOZ32103MQV has a built-in charge pump circuit to maintain sufficient voltage so that the high side can remain on.

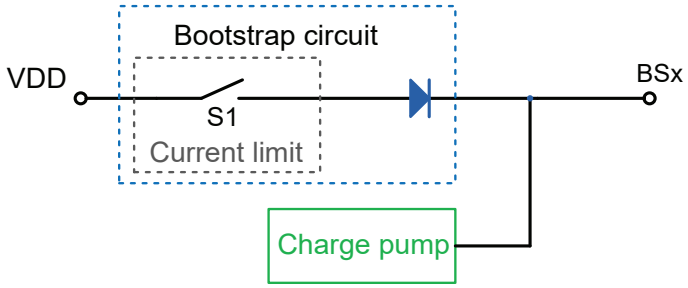


Figure 2. Bootstrap Circuit Architecture

Sleep

AOZ32103MQV-06 has very low sleep power consumption. When entering sleep mode, most of the circuits are turned off, and the power consumption can be less than 1μA.

Control whether the system enters sleep through nSLEEP pin when:

- nSLEEP = high, enable, normal operation mode
- nSLEEP = low, sleep mode

When the system wakes up from sleep, after about 100μs, the gate driver will start to work.

Control Logic

When nSLEEP is pulled high, HOx and LOx follow their respective HIx and LIx signals through the gate driver to drive MOSFETs, and the internal circuit will also judge whether the HIx/LIx signals are high at the same time to avoid shoot-through of High/Low side MOSFETs.

The truth table of the control logic is as follows:

Table 1. Truth Table of the Control Logic

HIx	LIx	HOx	LOx	VOx
L	L	L	L	High Impedance
H	L	H	L	VIN
L	H	L	H	GND
H	H	L	L	High Impedance

Dead Time and Shoot-through Prevention

AOZ32103MQV-06 has a built-in dead time adjustment function. The dead time can be adjusted only by adjusting the resistance value of the DT pin to ground. Users can set different dead time for different application conditions.

DT pin has three settings, as shown in the table below:

Table 2. DT Pin Settings

DT Pin	Dead Time (μs)
Open	6
Tied to GND	0.15
Add R	Calculated by the following formula: t_{dead} (μs) = 0.04 x R_{DT} (KΩ) + 0.15

The high side and low side are independently controlled by individual signals. In order to prevent the high side and low side MOSFETs from being turned on at the same time, AOZ32103MQV-06 has a built-in shoot-through prevention mechanism. The following figure illustrates the dead time and shoot-through prevention mechanism.

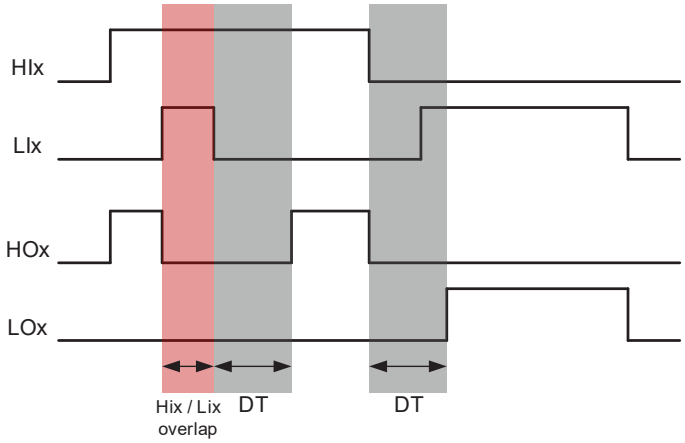


Figure 3. Dead Time and Shoot-through Prevention

Current Sense

AOZ32103MQV-06 has a built-in amplifier circuit with a gain of 20V/V, which is used to feed back the total current of the system.

The LSS pin is the input terminal of the amplifier. When the low side MOSFET is turned on, the total current of the system flows through the shunt resistor between LSS and GND, and the voltage difference generated by the shunt resistor is the voltage of LSS, which is amplified 20 times by the internal amplifier. The current is output by CSO ,and charge the external capacitor. The capacitance of this CSO to ground is recommended to be 1nF.

When the low side MOSFET is turned off, no current flows through the shunt resistance of LSS to ground. At this time, the capacitance of CSO can only be discharged through the internal resistance of CSO (about 475KΩ), causing the discharge rate to be too slow to keep up with the actual current discharge rate, so it is recommended to connect a resistor of about 1KΩ in parallel to maintain the accuracy of current feedback.

The recommended operating range of LSS is 50mV~200mV, in this range, the amplification factor of the amplifier will be close to 20 times, because the voltage of CSO is limited to about 4V.

Therefore, it is recommended to design the operating voltage of LSS below 200mV in order to obtain accurate feedback.

Over Temperature Protection

When the system is working, if the temperature of the die is too high and exceeds the internally set temperature protection level (about 150°C), AOZ32103MQV-06 automatically enters the over-temperature protection, the gate driver stops working and does not output signals, and the nFAULT pin is pulled low at the same time.

Fault Report

The nFAULT pin is an open-drain output and requires an external pull-up resistor to report a fault. Users can use this signal to judge whether the AOZ32103MQV-06 is in a normal or faulty state. The fault pin reports the following two types of faults.

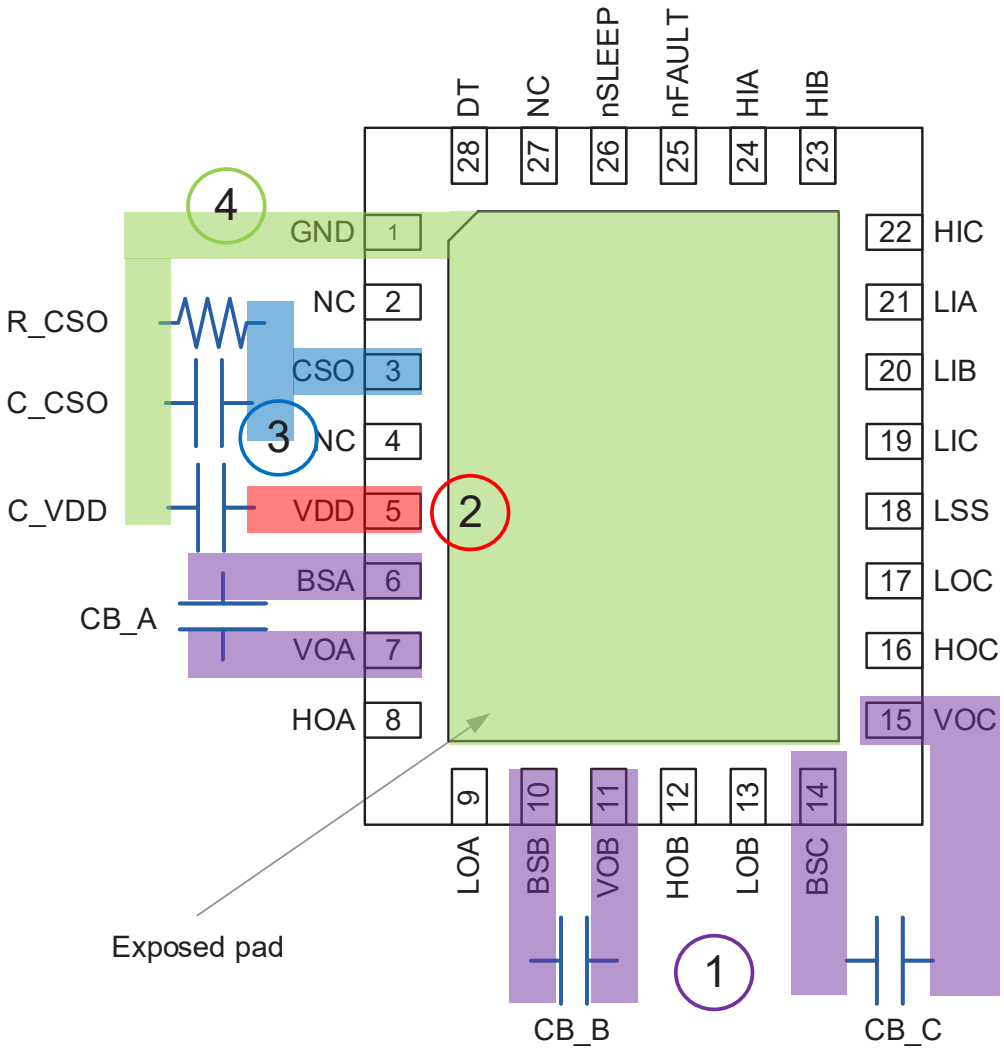
1. VDD UVLO:
   - When VDD power up and VDD < VDD UVLO rising threshold
   - When VDD power down and VDD < VDD UVLO falling threshold
2. Over temperature: junction temperature > 150°C

When a fault occurs, nFAULT pin pull low.

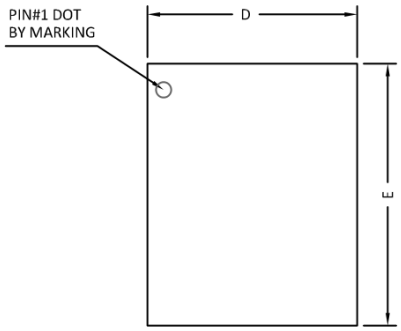
Layout Considerations

A good layout is very important for noise suppression and driver performance. List the following four layout suggestions and refer to the figure below:

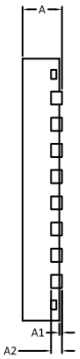
1. The bootstrap capacitor needs to be close to the corresponding pin.
2. The VDD capacitor should be placed as close as possible to the VDD pin, which can effectively reduce noise.
3. The external components of the CSO should be close to the corresponding pins.
4. The GND of the VDD capacitor is close to the GND pin and connected to the exposed pad.



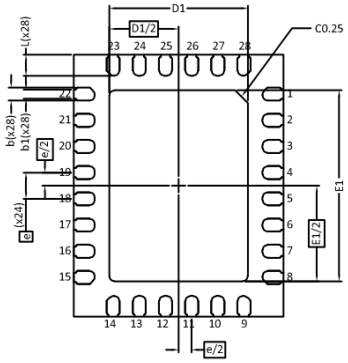
Package Dimensions, QFN5x4-28L



TOP VIEW

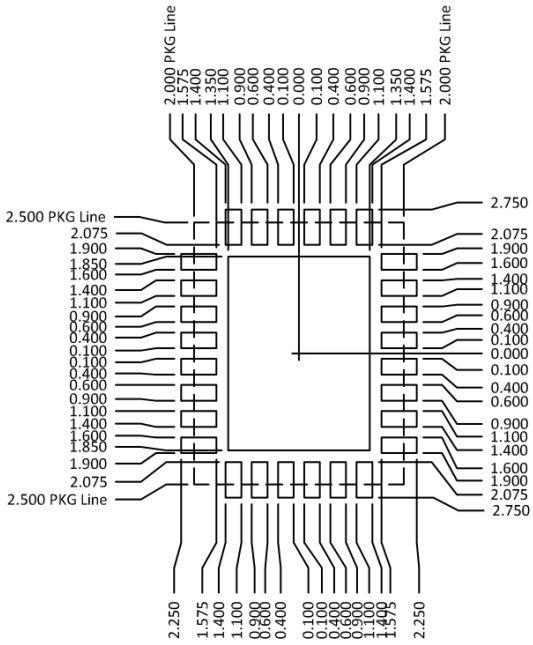


SIDE VIEW



BOTTOM VIEW

RECOMMENDED LAND PATTERN



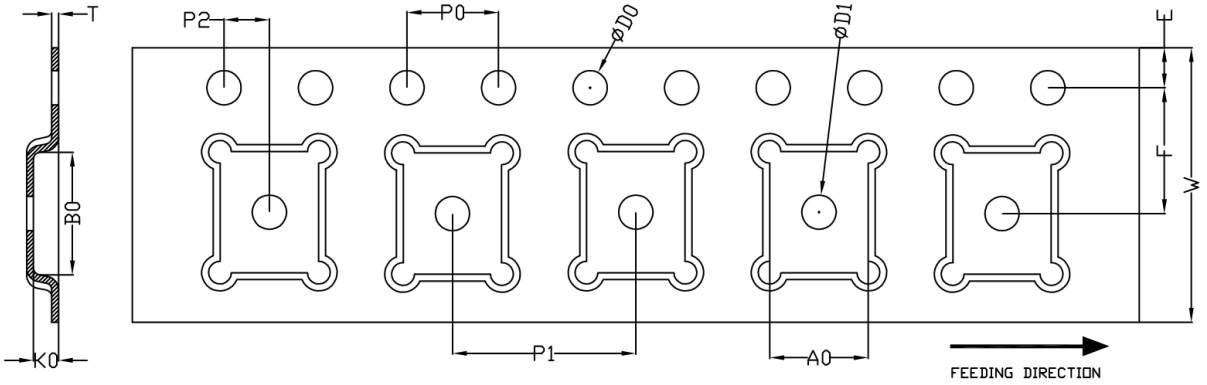
UNIT: mm

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	----	0.002
A2	0.15	0.20	0.25	0.006	0.008	0.010
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.175 REF			0.007 REF		
D	3.90	4.00	4.10	0.154	0.157	0.161
D1	2.55	2.65	2.75	0.100	0.104	0.108
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	3.55	3.65	3.75	0.140	0.144	0.148
e	0.50BSC			0.020BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018

NOTE:
1. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN5x4-28L

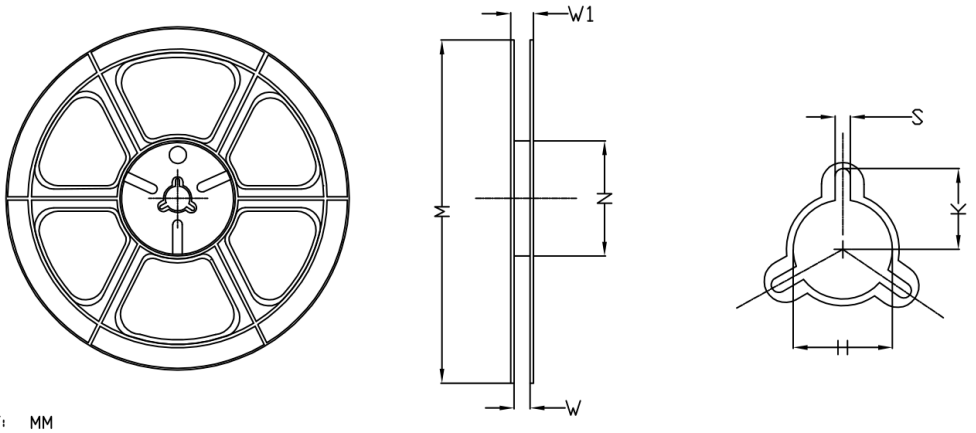
QFN5x4_24L_EP3_S/QFN5x4_28L_EP1_S Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E	F	P0	P1	P2	T
QFN5x4 -0.75	4.30 ±0.10	5.30 ±0.10	1.10 ±0.10	Ø1.50 +0.10 -0.00	Ø1.50 ±0.10	12.00 ±0.3	1.75 ±0.10	5.50 ±0.05	4.00 ±0.10	8.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN5x4_24L_EP3_S/QFN5x4_28L_EP1_S Reel



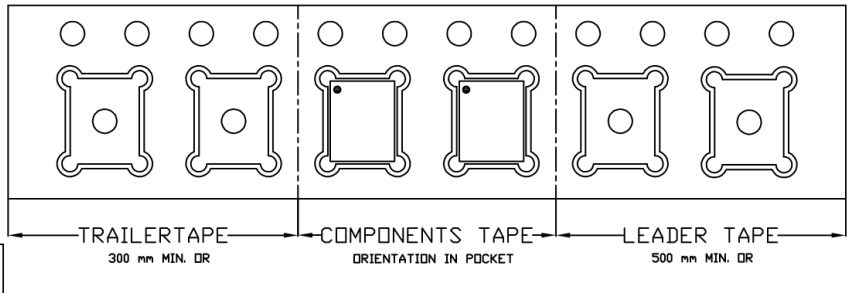
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S			
12 mm	Ø330	Ø330 ±0.50	Ø97.00 ±0.10	13.0 ±0.30	17.40 ±1.00	Ø13.0 +0.5 -0.2	10.6	2.00 ±0.50			

QFN5x4_24L_EP3_S
QFN5x4_28L_EP1_S Tape

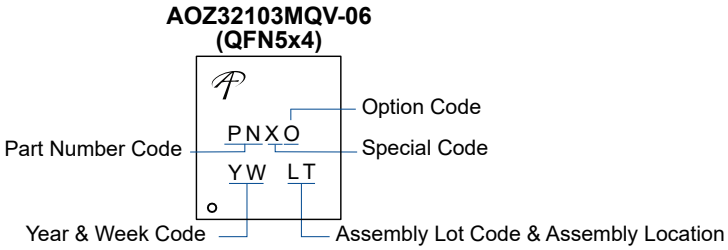
Leader / Trailer
& Orientation

Unit Per Reel:
3000pcs



All Dimensions Comply with EAI-481

Part Marking



Part Number	Description	Code
AOZ32103MQV-06	Green Product	ACM6

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