ALPHA & OMEGA SEMICONDUCTOR

AOZ97774QE

Dual Digital Multi-Phase Controller
Product Brief

General Description

The AOZ97774QE is high performance dual-channel digital controller designed to power processors, ASICs, or FPGAs. All required parameters are programmable through PMBus™ interface.

The device utilizes digital technology to implement all control and power management functions to provide maximum flexibility and performance. It can be configured using PMBus or Pin-strap to select custom configurations stored in Non-Volatile Memory (NVM) and/or Read Only Memory (ROM).

The AOZ97774QE features up to 3+1 phase programmable operation. The device assures fast and independent protection against load over current, under/over voltage and feedback disconnection. In addition to being able to store the device configurations in the NVM, the device can hold up to 15 custom configurations in the ROM. These configurations and up to 31 output voltage settings can be selected by pin-strapping.

The device is available in QFN-40L 5x5mm.

Device Summary

Order Code	Package	Packing
AOZ97774QE	QFN 5x5mm	Tape and Reel

Features

- INTEL VR13 3+1 phase compact digital controller
- VR13 compliant w/ 25MHz SVID bus rev1.7
- Powered from a single 3.3V supply
- High-performance digital control loop (Digital COT™)
- Fully configurable through PMBus™ revision 1.2
- Auto DPM - Automatic Dynamic Phase Management
- Configuration and output voltage selection supported through Pin-strap (15 configurations).
- Remote sense; 0.5% Vout accuracy
- Telemetry: VIN, IIN, PIN, VOUT, IOUT, POUT, TEMP
- Programmable voltage positioning
- Output OV, UV, OC and FB disconnection protection
- Embedded NVM and/or ROM
- Black-Box fault recorder captures critical fault information in NVM
- QFN 5x5mm package

Applications

- General Purpose, up to 3-phase applications
- Network Processor, ASIC, and FPGA Power
- High-current power regulation for VR13 Intel® based microprocessors
- DDR Memory power regulation for VR13 Intel® based systems

Green Product

Typical Application Circuit

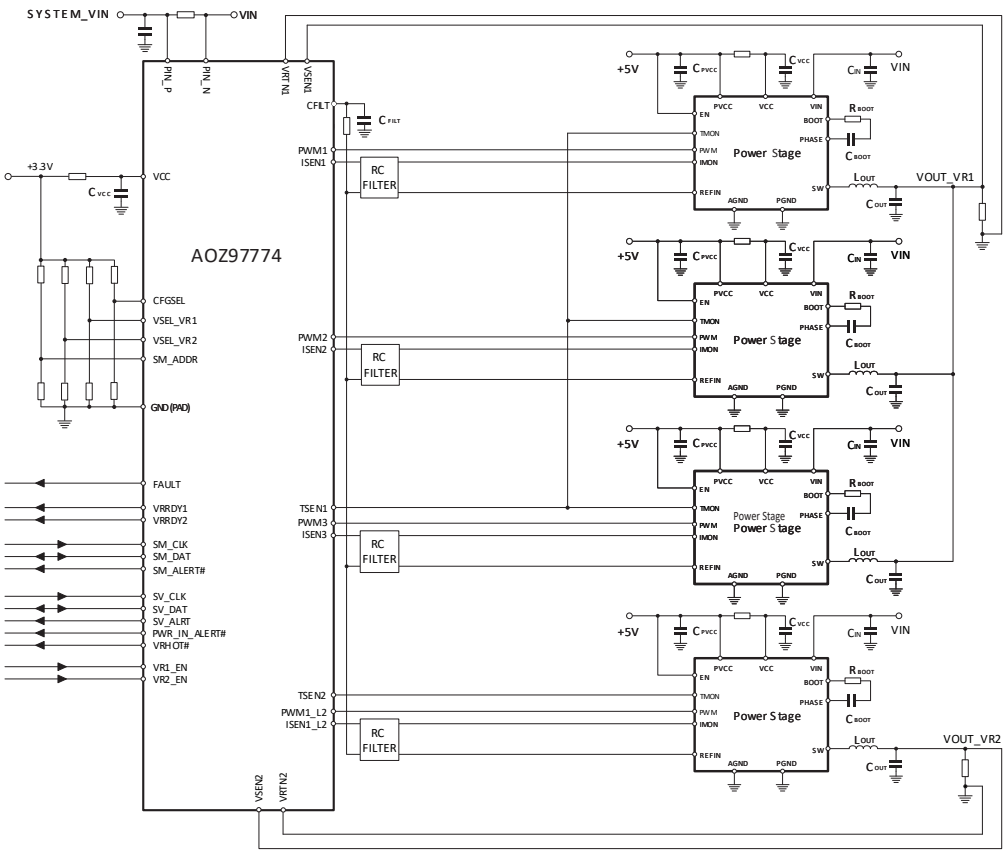


Figure 1. 3+1 AOZ97774QE Application Circuit with Smart Power Stages

Pin Configuration

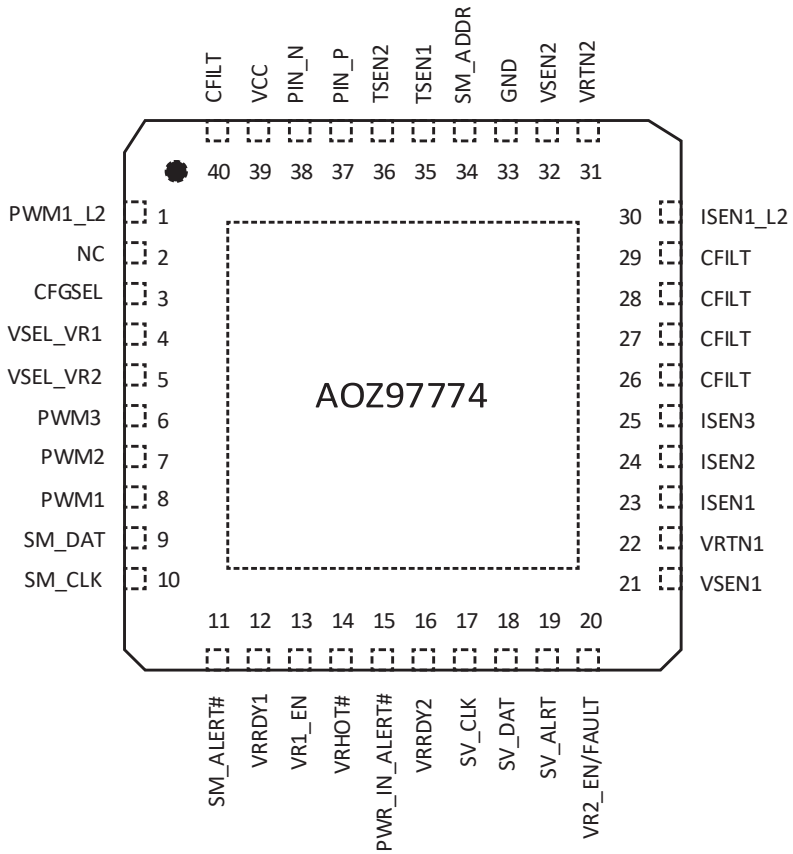


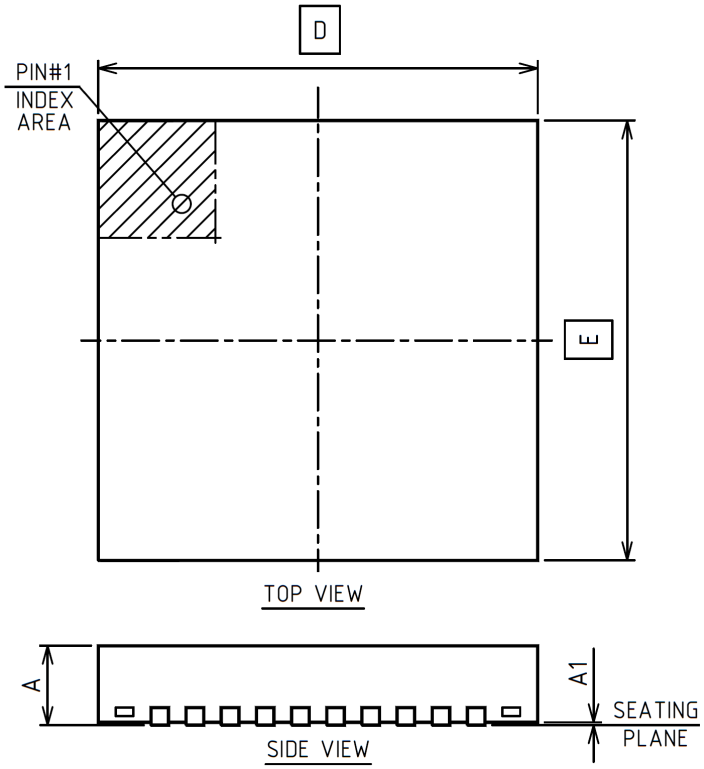
Figure 2. QFN5x5-40L
(Top View)

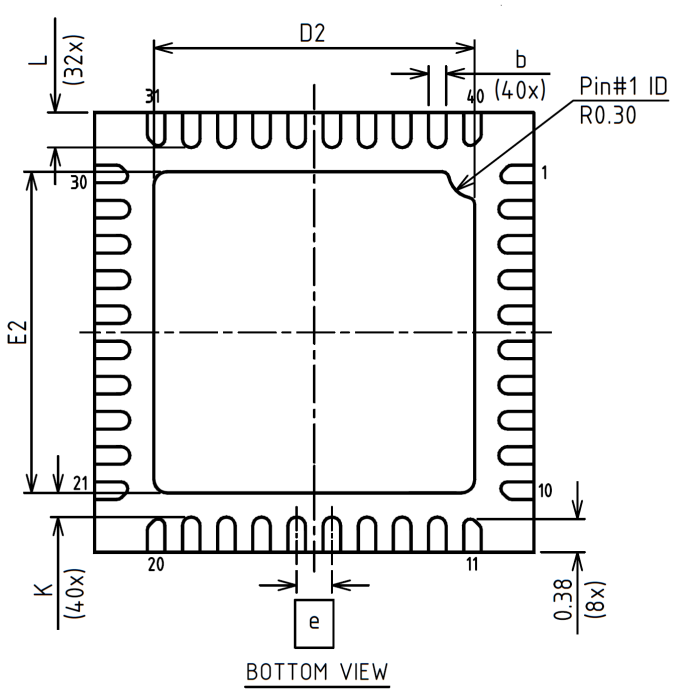
Pin Descriptions

Pin#	Name	I/O	Type	Function
1	PWM1_L2	O	Digital	VR2 PWM Output. Used to drive PWM input of external Power Stage. PWM is a tri-state signal: High, Low and HiZ. Leave floating if not used.
2	NC	-	-	Not Connected. Can be left floating.
3	CFGSEL	I	Analog	Select signal for configurations. The voltage applied to this pin using Pin-strap (by resistor divider) is measured at startup to select the configuration mode from those listed in Table 1
4	VSEL_VR1	I	Analog	Voltage select pin for VR1. The voltage applied to this pin using Pin-strap (by resistor divider) is measured at startup to select from the list of available voltages in Table 1.
5	VSEL_VR2	I	Analog	Voltage select pin for VR2. The voltage applied to this pin using Pin-strap (by resistor divider) is measured at startup to select from the list of available voltages in Table 1.
6	PWM3	O	Digital	VR1 PWM Output. Used to drive PWM input of external Power Stage. PWM is a tri-state signal: High, Low and HiZ.. Leave floating if not used
7	PWM2	O	Digital	
8	PWM1	O	Digital	
9	SM_DAT	I/O	Open Drain	PMBus Bi-directional Data Signal. Pull-up externally up to 3.3V.
10	SM_CLK	I	Open Drain	PMBus Clock Signal. Pull-up externally up to 3.3V.
11	SM_ALERT#	O	Open Drain	PMBus Alert Signal. Pull-up externally up to 3.3V.
12	VRRDY1	O	Open Drain	VR1 ready signal. Asserted when the controller's VR1 is ready to accept SVID commands. Pulled low when controller is shutdown or any fault occurs. Pull-up externally up to 3.3V. If not used it can be left floating.
13	VR1_EN	I	Digital	Enable Signal for VR1 or both VRs, according to System Register setting. Pulling this pin high activates the controller's VR1. Pulling VR1_EN high clears any fault detected for VR1.
14	VRHOT#	O	Open Drain	VR_HOT#. Active Low indicator, for VR1. It is asserted when the monitored temperature exceeds the TMAX threshold programmed. Pull-up to VCC when not used
15	PWR_IN_ALERT#	O	Open Drain	Asserted low when Input Power measured reaches the programmed threshold. Pull-up to VCC when not used.
16	VRRDY2	O	Open Drain	VR2_READY Signal. Asserted when the controller's VR2 is ready to accept SVID commands. Pulled low when controller is shutdown or any fault occurs. Pull-up externally up to 3.3V, if not used it can be left floating.
17	SV_CLK	I	Open Drain	SVI Clock Signal.
18	SV_DAT	I/O	Open Drain	SVI Data Signal.
19	SV_ALRT	O	Open Drain	SVI Alert Signal.
20	VR2_EN / FAULT	I/O	Open Drain	VR2 enable or fault pin configurable according to System Register setting. When configured as Enabled Signal for VR2, pulled high activates the controller's VR2. Pulling VR2_EN high clears any fault for VR2. When configured as FAULT indicator, it is used to monitor system faults. The assertion can be configured through System Register setting and may include OV, UV, OC and OT.

Pin#	Name	I/O	Type	Function
21	VSEN1	I	Digital	VR1 remote voltage sense inputs. VSEN1 is for the remote voltage and VRTN1 is for the remote ground. These are inputs of a precision differential voltage amplifier and are to be routed differentially and connected to the sense pins/location of the remote load. VRTN1 has to be grounded (locally or remotely) under any condition. If not used, connect VSEN1 and VRTN1 to ground.
22	VRTN1	I	Analog	
23	ISEN1	I	Analog	VR1 Phase #1 differential current sense inputs: ISEN1 is the positive sense and CFILT is the return. These are to be routed differentially and connected to IMON/ REFIN output of smart power stage, such as AOZ5473. The controller expects to sense a 5mV/A signal. If not used, short to CFILT.
24	ISEN2	I	Analog	VR1 Phase #2 differential current sense inputs: ISEN2 is the positive sense and CFILT is the return. These are to be routed differentially and connected to IMON/ REFIN output of smart power stage, such as AOZ5473. The controller expects to sense a 5mV/A signal. If not used short to CFILT.
25	ISEN3	I	Analog	VR1 Phase #3 differential current sense inputs: ISEN3 is the positive sense and CFILT is the return. These are to be routed differentially and connected to IMON/ REFIN output of smart power stage, such as AOZ5473. The controller expects to sense a 5mV/A signal. If not used short to CFILT.
26	CFILT	-	-	Not Used. Must be shorted to CFILT.
27	CFILT	-	-	
28	CFILT	-	-	
29	CFILT	-	-	
30	ISEN8/ISEN1_L2	-	-	VR2 Phase #1 or VR1 Phase #8 differential current sense inputs: ISEN8/ISEN1_L2 is the positive sense and CFILT is the return. These are to be routed differentially and connected to IMON/REFIN output of the external power stage. The controller expects to sense a 5mV/A signal. If not used short to CFILT.
31	VRTN2	I	Analog	VR2 remote voltage sense inputs. VSEN2 is for the remote voltage and VRTN2 is for the remote ground. These are inputs of a precision differential voltage amplifier and are to be routed differentially and connected to the sense pins/location of the remote load. VRTN2 has to be grounded (locally or remotely) under any condition.
32	VSEN2	I	Analog	
33	GND	-	-	Connect to contiguous ground plane.
34	SM_ADDR	I	Analog	PMBus and SVID addresses are set by connecting an external resistor divider between VCC and GND. See Table 1 for details on how to set the device address.
35	TSEN1	I	Analog	VR1/2 external temperature sense. Connect to smart power stage's TMON output, such as AOZ5473. The controller expects to sense a 8mV/C signal. Basing upon SPS_READY configuration in System Registers, the device expects to read a voltage (>0.25V typ) prior to initializing any start-up at -40ºC. In the same manner, if the condition is not satisfied, even during switching operation, the device sets PWMx to HiZ. TSEN1 acts on VR1 and TSEN2 acts on VR2. Whenever the pin is pulled to 3V (SPS_FAULT) the device immediately stops switching setting PWM to HiZ. If not used connect TSEN1 to TSEN2.
36	TSEN2	I	Analog	
37	PIN_P	I	Analog	Differential Input sense pins for Power In sense measurement. PIN_P has to be connected to the positive side of the sensing element (either DCR or sense resistor) while PIN_N has to be connected to the negative side. Max signal has to be limited within 25mV under any condition. DCR sense requires external time-constant matching network. Input voltage is sensed through the same pins while input current is computed starting from PIN and VIN measured. If PIN reading is not used, those two pins need to be shorted together and connected to VIN.
38	PIN_N	I	Analog	
39	VCC	I	Power	+3.3V Power Supply Input. To be connected to the system 3.3V rail and decoupled typically by 1uF and 0.1uF MLCC cap to GND.
40	CFILT	O	Power	Internally generated 1.8V Supply for digital core, decoupled typically by 1uF and 0.1uF MLCC to GND. Also used as current sense reference, to be connected to REFIN pin of smart power stage(s), such as AOZ5473.
PAD	PAD	--	Power	Exposed pad. To be soldered to the PCB GND plane.

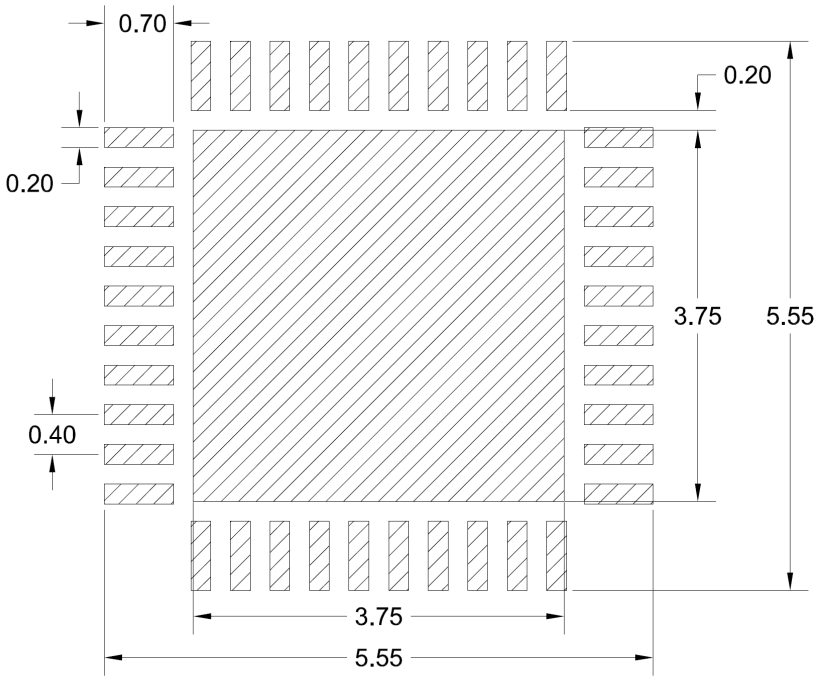
Package Dimensions, QFN5x5-40L





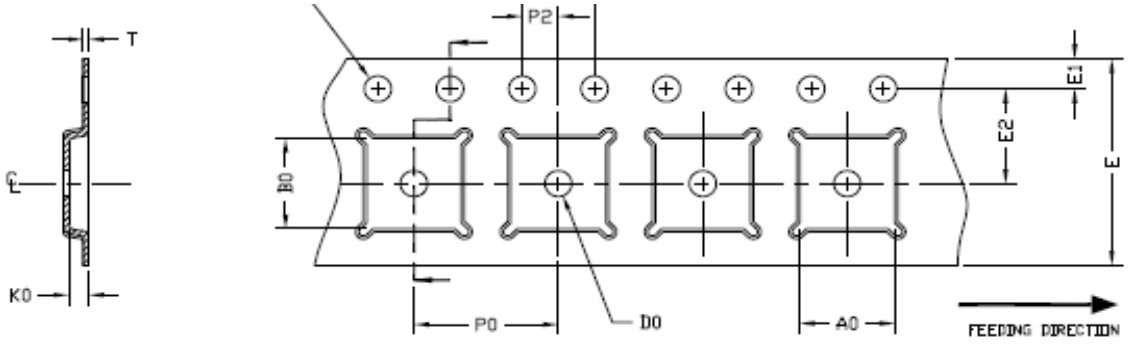
Thickness / Symbol	Dimension Table		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
e		0.40 BSC	
D2	3.50	3.65	3.75
E2	3.50	3.65	3.75
K	0.20	---	---
L	0.30	0.40	0.50

NOTE:
1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.



RECOMMENDED FOOTPRINT

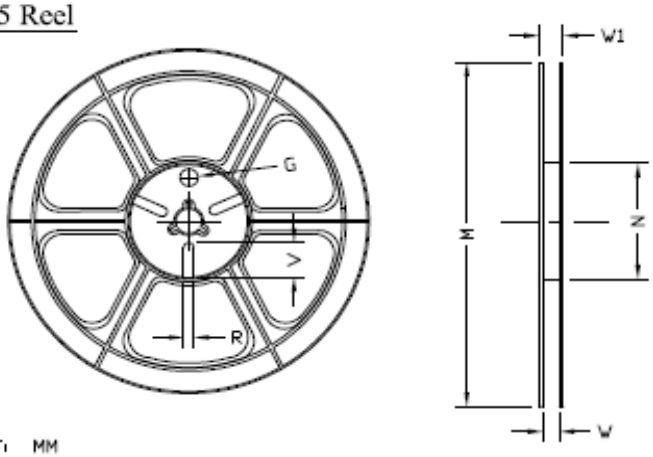
Tape and Reel Dimmensions, QFN 5x5-40L



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 -0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN5x5 Reel

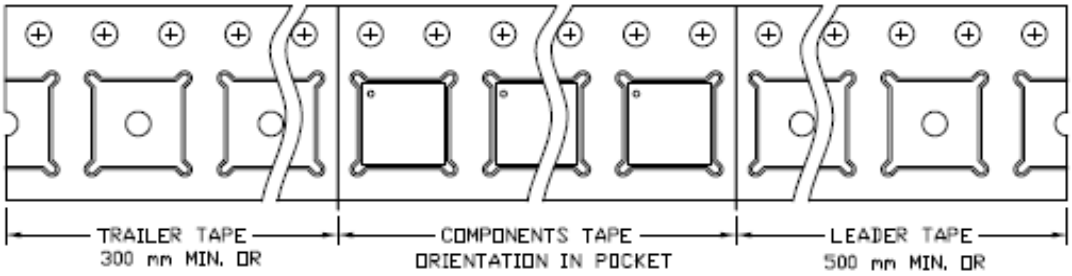


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø100.0 ±1.0	12.4 +2.0 -0.0	17.0 +2.6 -1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

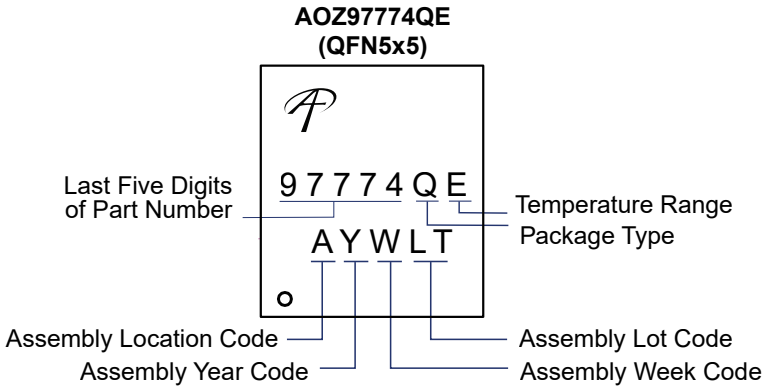
QFN5x5 Tape

Leader / Trailer
& Orientation



Unit Per Reel:
3000pcs

Part Marking



Part Number	Description	Marking Code
AOZ97774QE	Green Product	97774QE