

General Description

- Trench Power LV (P-ch) MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- ESD protected
- RoHS and Halogen-Free Compliant

Applications

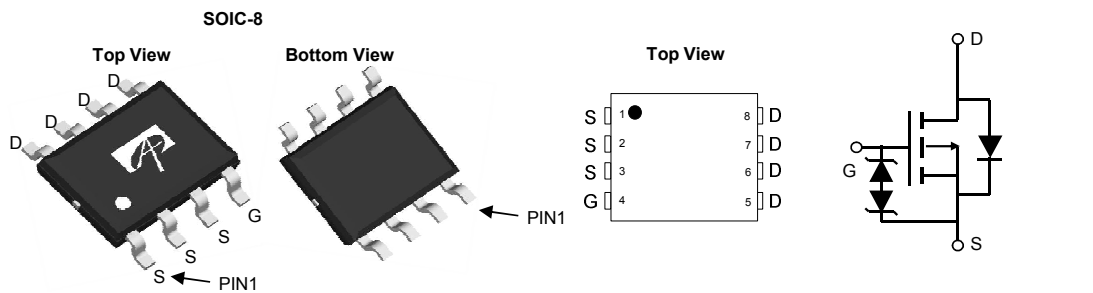
- This device is suitable for use as a load switch or in PWM applications.

Product Summary

V_{DS}	-30V
I_D (at $V_{GS}=-10V$)	-6A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	< 45m Ω
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	< 80m Ω

Typical ESD protection **HBM Class 1C**

100% UIS Tested
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AO4405E	SO-8	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	-24	A
Avalanche Current ^C	I_{AS}, I_{AR}	15	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	11	mJ
V_{DS} Spike	V_{SPIKE}	-36	V
Power Dissipation ^B	P_D	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	42	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D}		70	85	
Maximum Junction-to-Lead	$R_{\theta JL}$	20	30	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
B _V DSS	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-2.5	-2	-1.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-6A T _J =125°C		29 40	45 65	mΩ
		V _{GS} =-4.5V, I _D =-4A		50	80	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-6A		14		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.76	-1	V
I _S	Maximum Body-Diode Continuous Current				-3	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		495		pF
C _{oss}	Output Capacitance			100		pF
C _{riss}	Reverse Transfer Capacitance			56		pF
R _g	Gate resistance	f=1MHz	3.5	7.5	11.5	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-6A		8.8	16	nC
Q _{g(4.5V)}	Total Gate Charge			4.2	8	nC
Q _{gs}	Gate Source Charge			1.8		nC
Q _{gd}	Gate Drain Charge			2.0		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =2.5Ω, R _{GEN} =3Ω		9		ns
t _r	Turn-On Rise Time			4.5		ns
t _{D(off)}	Turn-Off DelayTime			15.5		ns
t _f	Turn-Off Fall Time			4.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-6A, dI/dt=500A/μs		9		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-6A, dI/dt=500A/μs		13.5		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

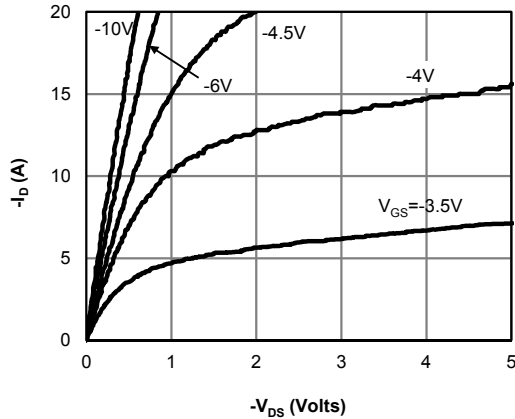


Figure 1: On-Region Characteristics (Note E)

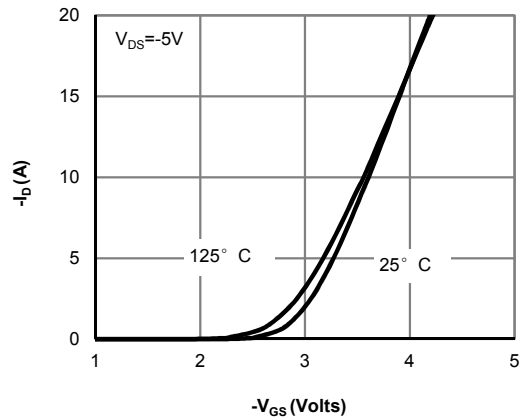


Figure 2: Transfer Characteristics (Note E)

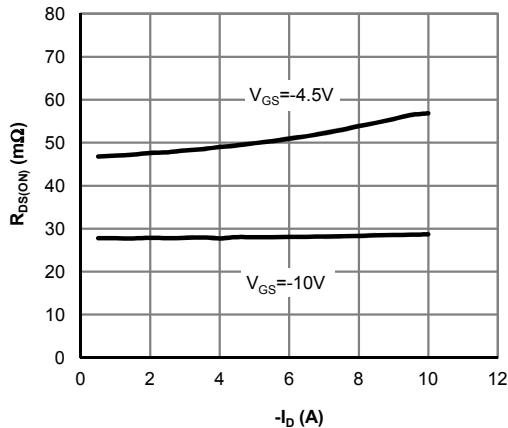


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

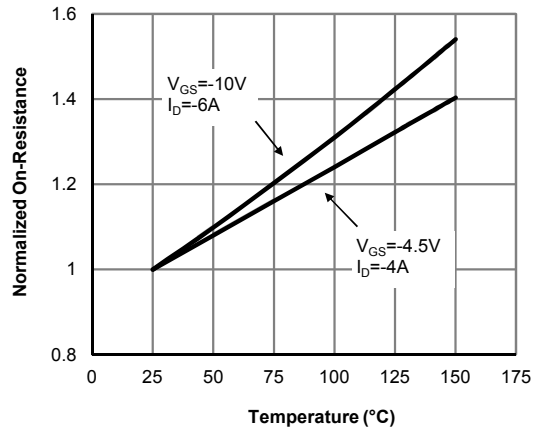


Figure 4: On-Resistance vs. Junction Temperature (Note E)

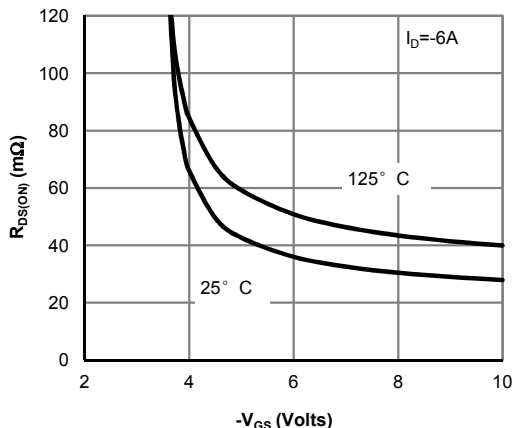


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

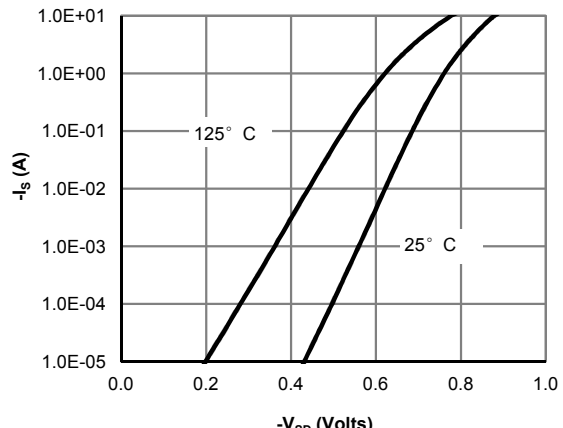


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

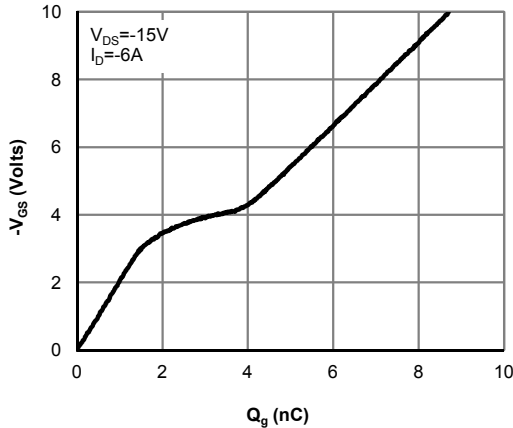


Figure 7: Gate-Charge Characteristics

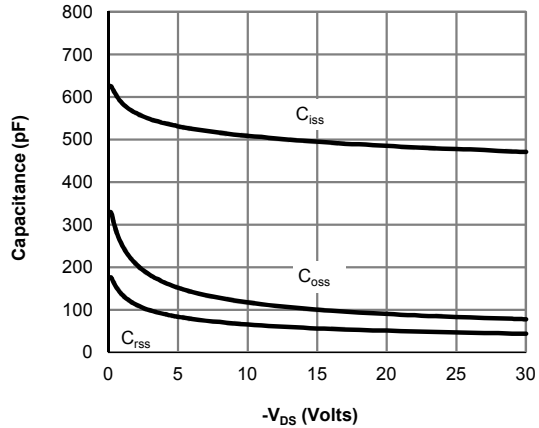


Figure 8: Capacitance Characteristics

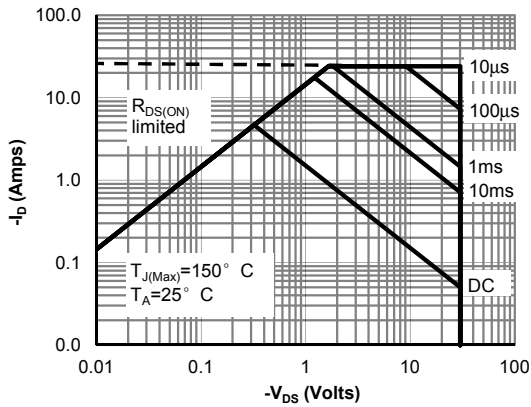


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

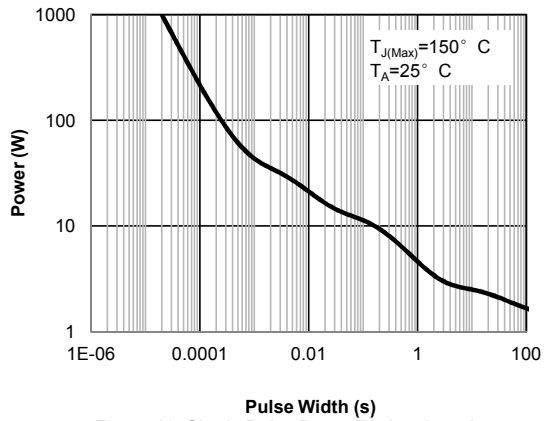


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

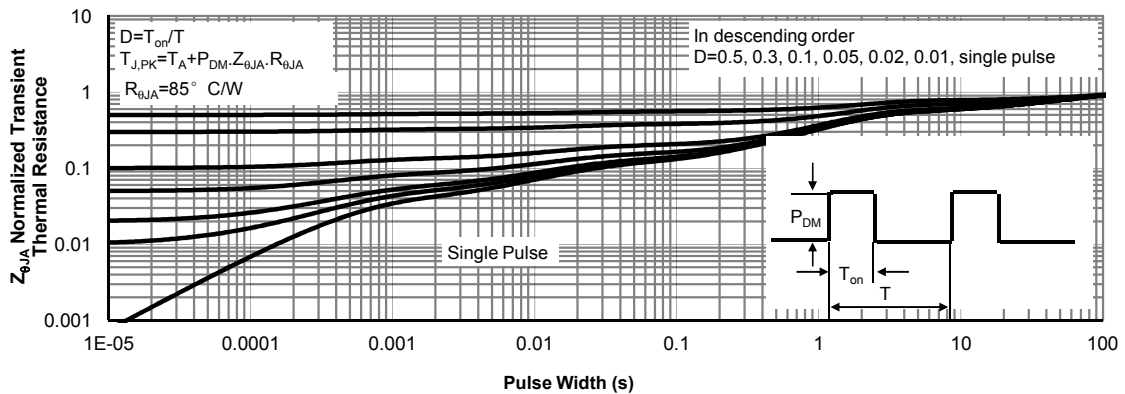
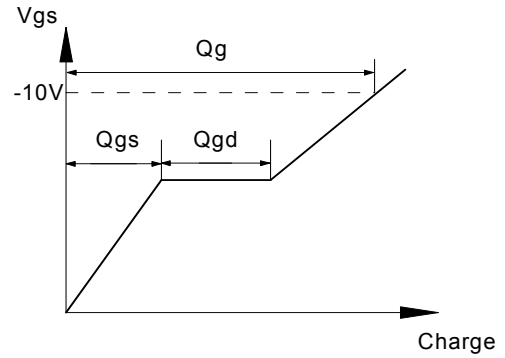
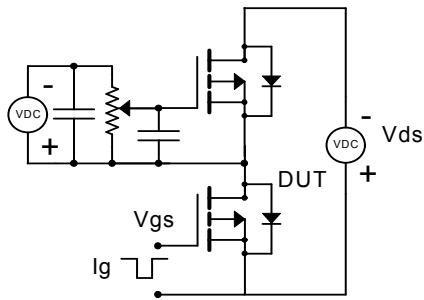
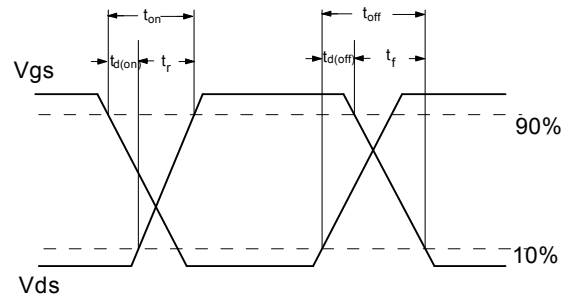
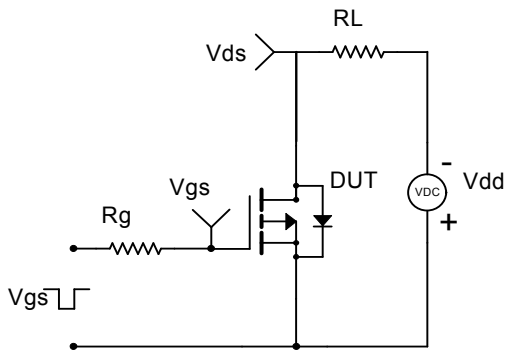


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

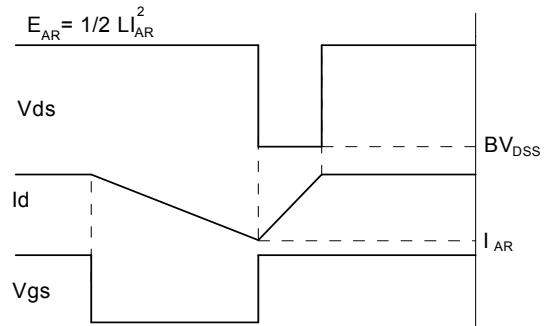
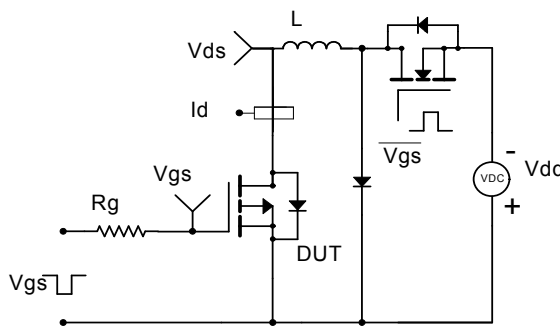
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

