

## AOD402

### N-Channel Enhancement Mode Field Effect Transistor

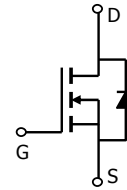
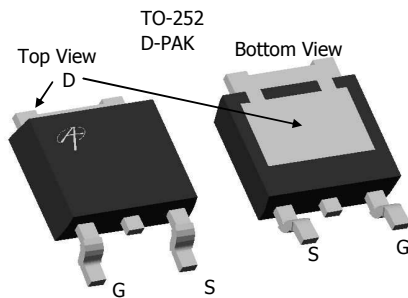
#### General Description

The AOD402 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

- RoHS Compliant
- Halogen Free\*

#### Features

- $V_{DS}$  (V) = 30V
- $I_D$  = 18 A ( $V_{GS}$  = 20V)
- $R_{DS(ON)} < 15 \text{ m}\Omega$  ( $V_{GS}$  = 20V)
- $R_{DS(ON)} < 18 \text{ m}\Omega$  ( $V_{GS}$  = 10V)
- $R_{DS(ON)} < 44 \text{ m}\Omega$  ( $V_{GS}$  = 4.5V)
- 100% UIS Tested!**
- 100% Rg Tested!**



#### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$	18
		$T_C=100^\circ\text{C}$	12
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	40	A
Avalanche Current <sup>C</sup>	$I_{AR}$	18	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	40	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	60
		$T_C=100^\circ\text{C}$	30
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	2.5
		$T_A=70^\circ\text{C}$	1.6
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	16.7	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	40	$^\circ\text{C/W}$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	1.9	2.5	$^\circ\text{C/W}$

**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=24\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1	$\mu\text{A}$
					5	
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 25\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1	2.4	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=20\text{V}$ , $I_D=18\text{A}$ $T_J=125^\circ\text{C}$		12	15	m $\Omega$
				17.4	21	
				15	18	
		$V_{GS}=4.5\text{V}$ , $I_D=6\text{A}$	36	44	m $\Omega$	
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=18\text{A}$		24		S
$V_{SD}$	Diode Forward Voltage	$I_S=18\text{A}$ , $V_{GS}=0\text{V}$		0.8	1	V
$I_S$	Maximum Body-Diode Continuous Current				18	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=15\text{V}$ , $f=1\text{MHz}$		769		pF
$C_{oss}$	Output Capacitance			185		pF
$C_{rss}$	Reverse Transfer Capacitance			131		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		0.7		$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_{g(10V)}$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=10\text{V}$ , $I_D=18\text{A}$		15.9		nC
$Q_{gs}$	Gate Source Charge			2.44		nC
$Q_{gd}$	Gate Drain Charge			4.92		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $I_D=18\text{A}$ , $R_L=0.82\Omega$ , $R_{GEN}=3\Omega$		6.2		ns
$t_r$	Turn-On Rise Time			10.9		ns
$t_{D(off)}$	Turn-Off Delay Time			16		ns
$t_f$	Turn-Off Fall Time			4.8		ns
$t_{rr}$	Body Diode Reverse Recovery Time		$I_F=18\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		18	
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=18\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		8.1		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any a given application depends on the user's specific board design, and the maximum temperature up to  $175^\circ\text{C}$  may be used if the PCB allows it.

B: The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

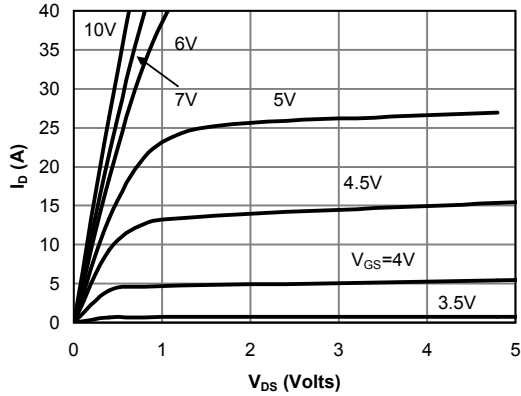
G: The maximum current rating is limited by bond-wires.

\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

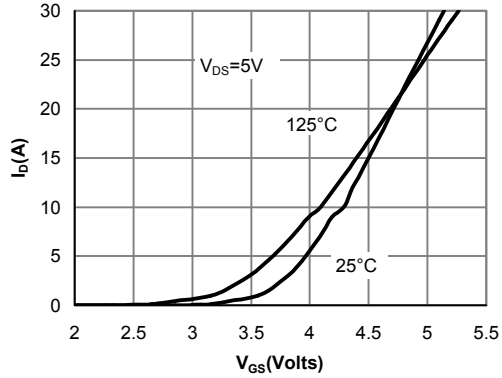
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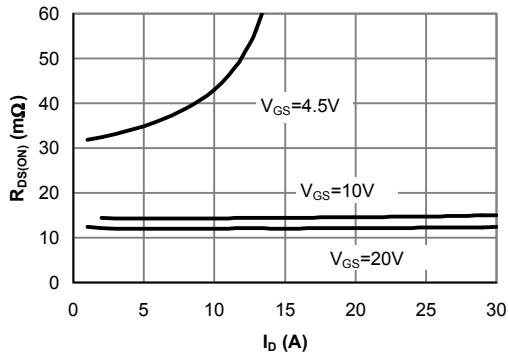
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



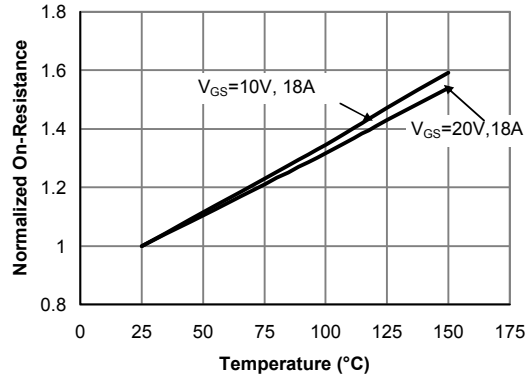
**Fig 1: On-Region Characteristics**



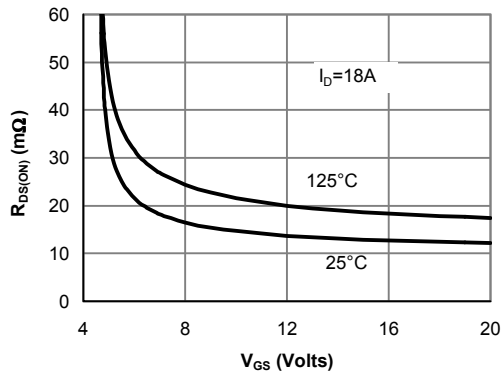
**Figure 2: Transfer Characteristics**



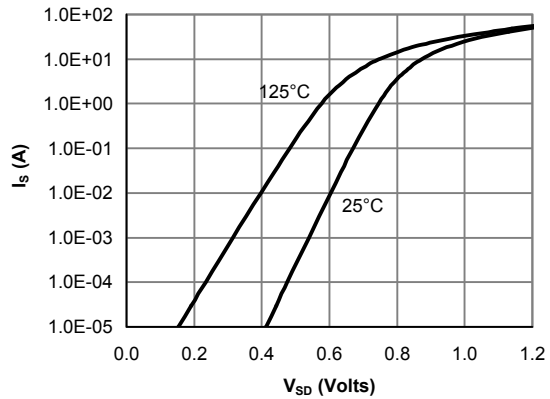
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**

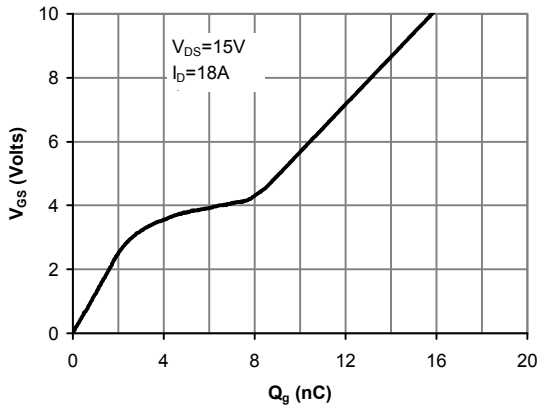


**Figure 5: On-Resistance vs. Gate-Source Voltage**

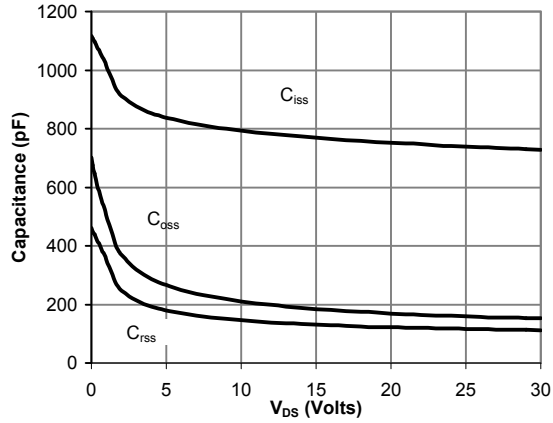


**Figure 6: Body-Diode Characteristics**

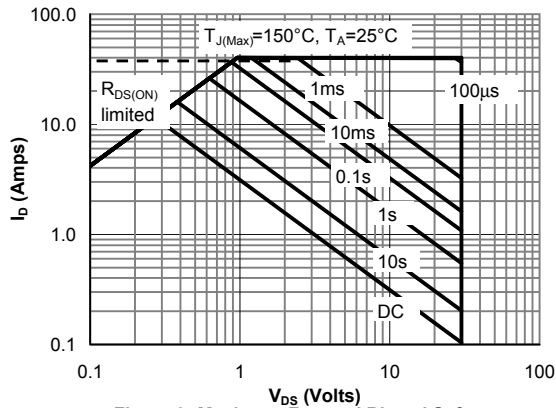
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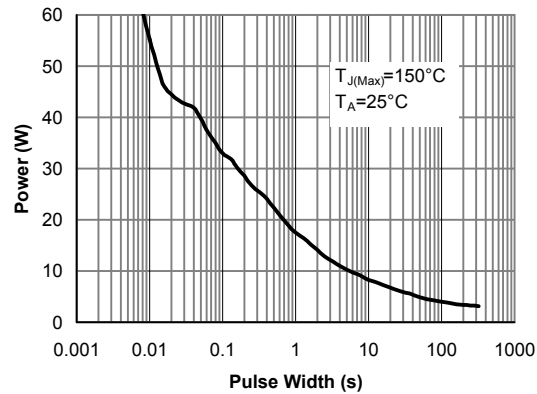
**Figure 7: Gate-Charge Characteristics**



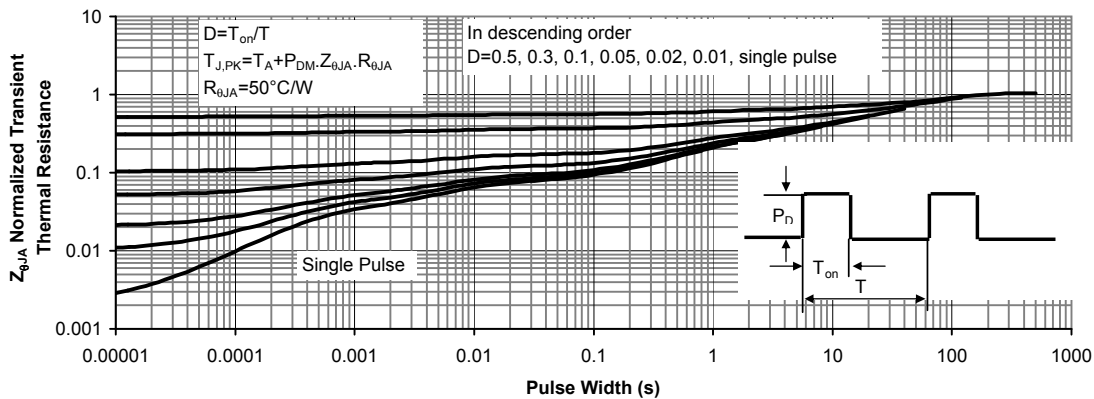
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

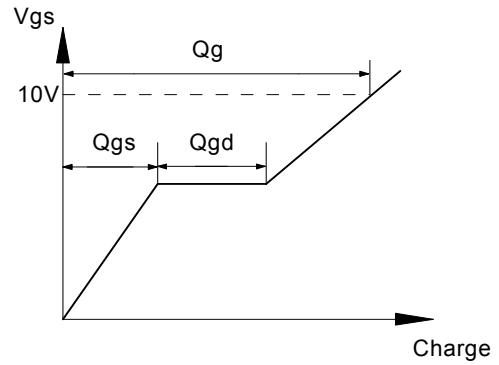
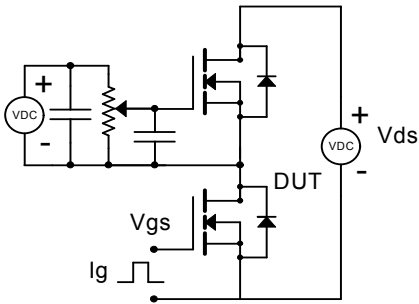


**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)**

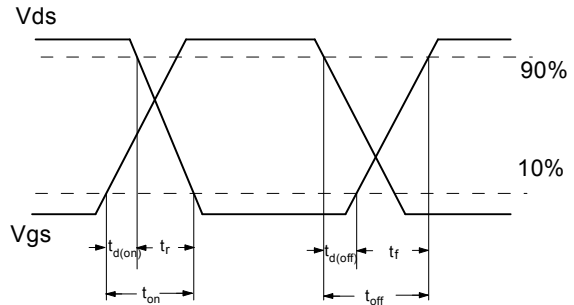
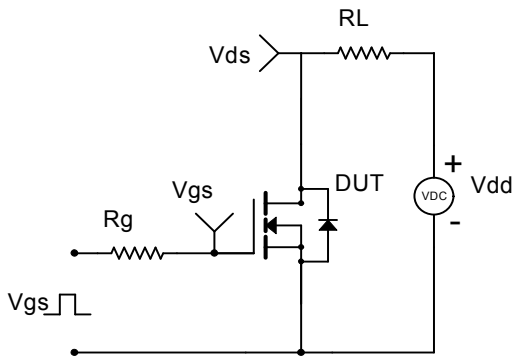


**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

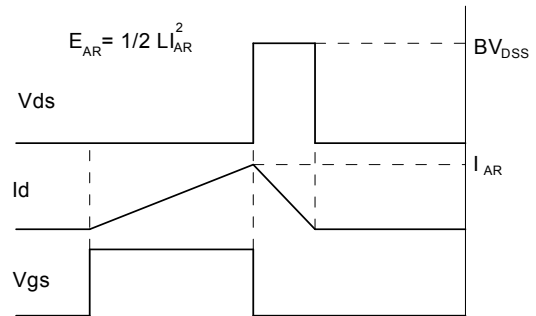
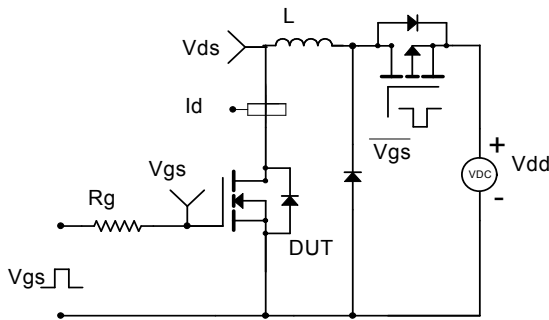
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### Diode Recovery Test Circuit & Waveforms

