

## AOL1444

### N-Channel Enhancement Mode Field Effect Transistor

#### General Description

The AOL1444 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , shoot-through immunity and body diode characteristics. This device is ideally suited for use as a low side switch in CPU core power conversion.

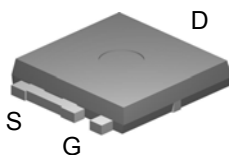
- RoHS Compliant
- Halogen and Antimony Free Green Device\*

#### Features

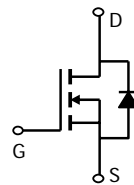
$V_{DS} (V) = 30V$   
 $I_D = 85A (V_{GS} = 10V)$   
 $R_{DS(ON)} < 4.3m\Omega (V_{GS} = 10V)$   
 $R_{DS(ON)} < 6.3m\Omega (V_{GS} = 4.5V)$

UIS Tested  
 $R_g, C_{iss}, C_{oss}, C_{rss}$  Tested

Ultra SO-8™ Top View



Bottom tab connected to drain



#### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B,G</sup>	$T_C=25^\circ C$ <sup>G</sup>	85	A
	$T_C=100^\circ C$ <sup>B</sup>	73	
Pulsed Drain Current	$I_{DM}$	200	
Continuous Drain Current <sup>G</sup>	$T_A=25^\circ C$	17	A
	$T_A=70^\circ C$	14	
Avalanche Current <sup>C</sup>	$I_{AR}$	30	A
Repetitive avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AR}$	45	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ C$	100	W
	$T_C=100^\circ C$	50	
Power Dissipation <sup>A</sup>	$T_A=25^\circ C$	2.1	W
	$T_A=70^\circ C$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	19.6	25	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	48	60
Maximum Junction-to-Case <sup>C</sup>	$R_{\theta JC}$	1	1.5	$^\circ C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C		0.005	1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1.45	1.8	3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	200			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		3.2 4.3	4.3 5.2	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		4.9	6.3	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		85		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				85	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		6070	7000	pF
C <sub>oss</sub>	Output Capacitance			638		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			375		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		0.45	0.6	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		96.4	115	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			46.4	55	nC
Q <sub>gs</sub>	Gate Source Charge			13.6		nC
Q <sub>gd</sub>	Gate Drain Charge			15.6		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		15.7	21	ns
t <sub>r</sub>	Turn-On Rise Time			14.2	21	ns
t <sub>D(off)</sub>	Turn-Off DelayTime			55.5	75	ns
t <sub>f</sub>	Turn-Off Fall Time			14	21	ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=100A/μs		31	38	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=100A/μs		24	29	nC

A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C.

G: Surface mounted on a 1 in 2 FR-4 board with 2oz. Copper.

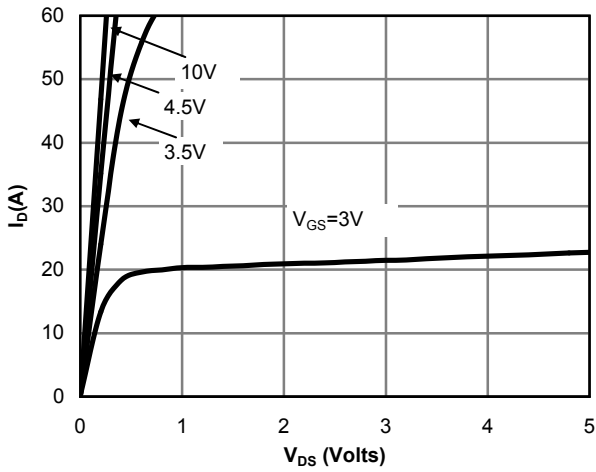
H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating. Rev1. July 2008

\* This device is guaranteed green after date code 8P11 (June 1ST 2008)

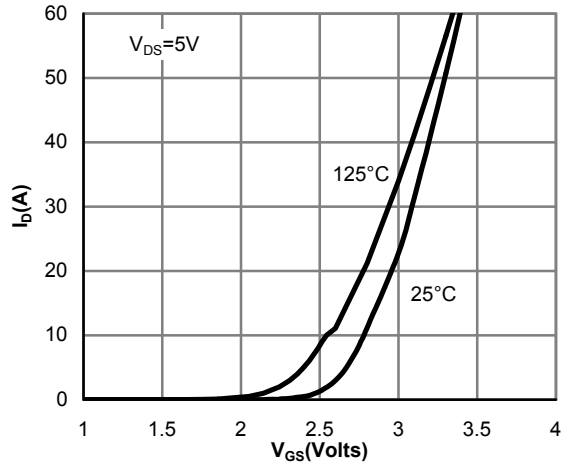
Revision 2: June 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE

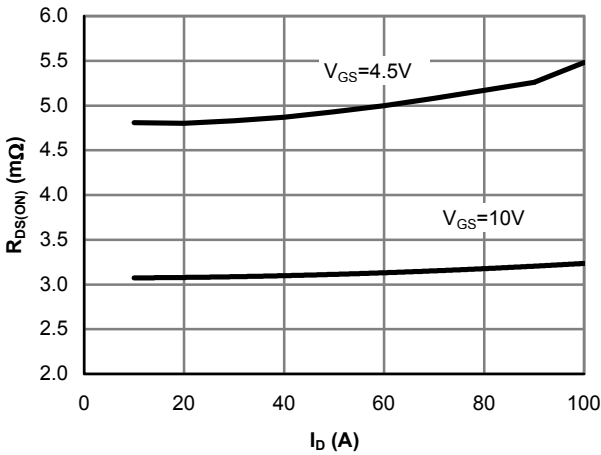
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



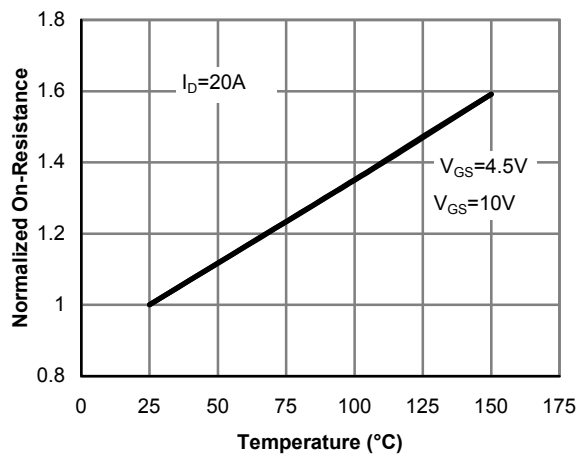
**Figure 1: On-Region Characteristics**



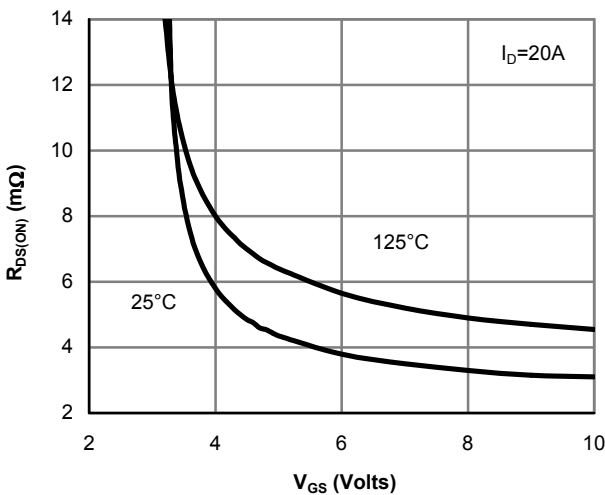
**Figure 2: Transfer Characteristics**



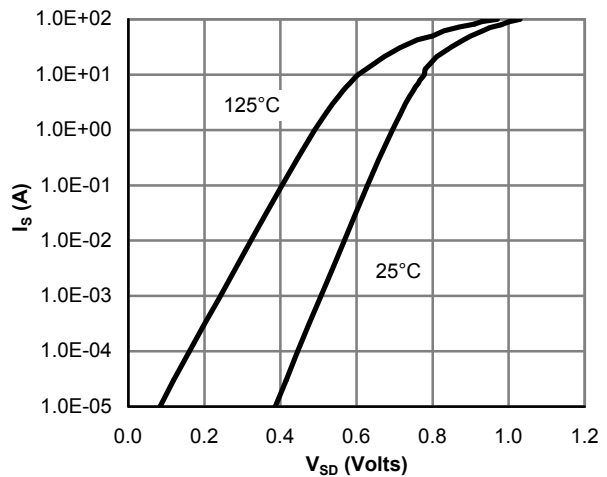
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



**Figure 5: On-Resistance vs. Gate-Source Voltage**



**Figure 6: Body-Diode Characteristics**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

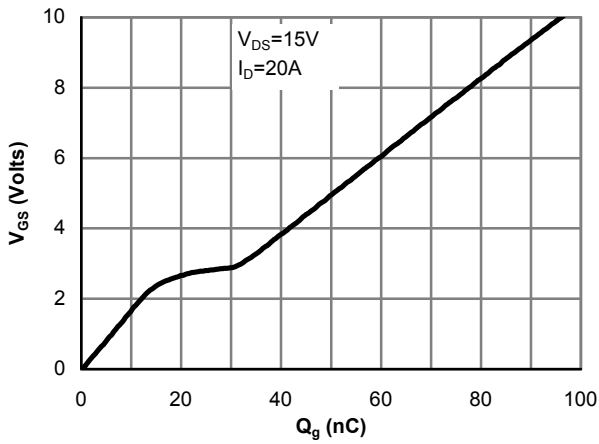


Figure 7: Gate-Charge Characteristics

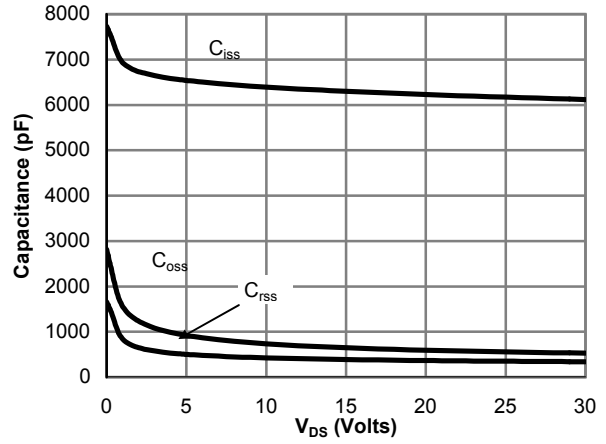


Figure 8: Capacitance Characteristics

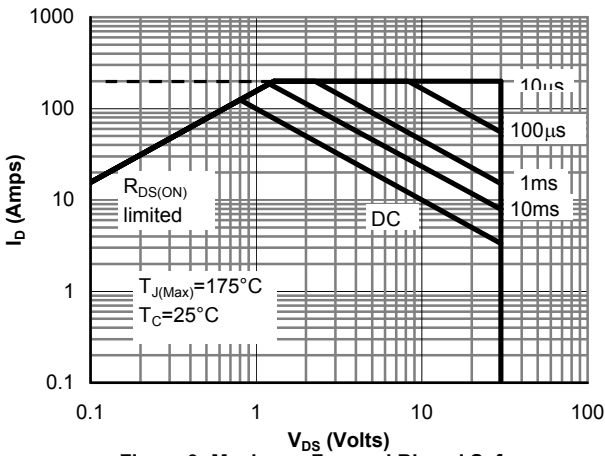


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

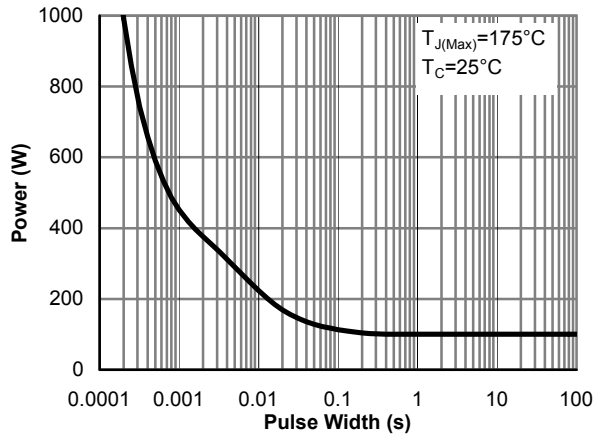


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

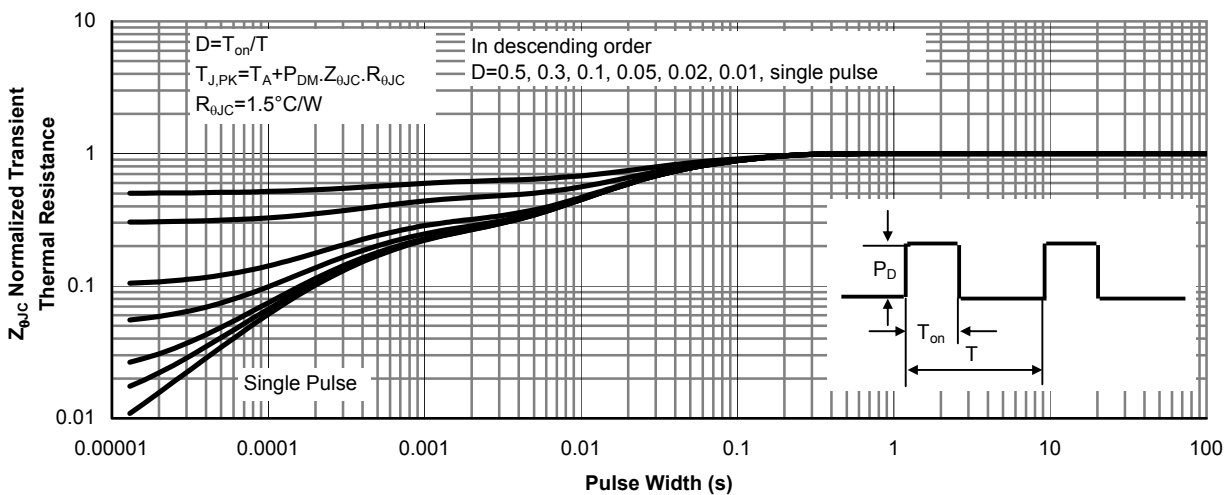


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

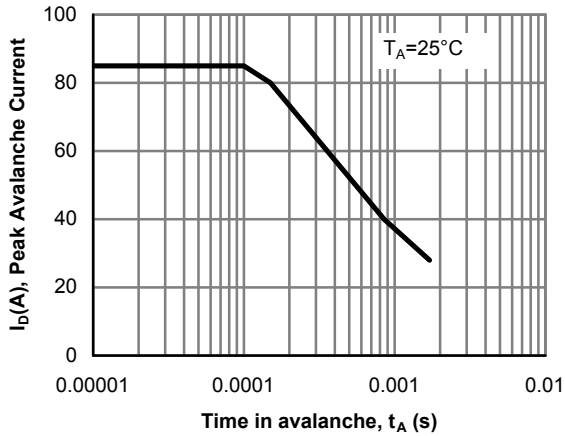


Figure 12: Single Pulse Avalanche capability

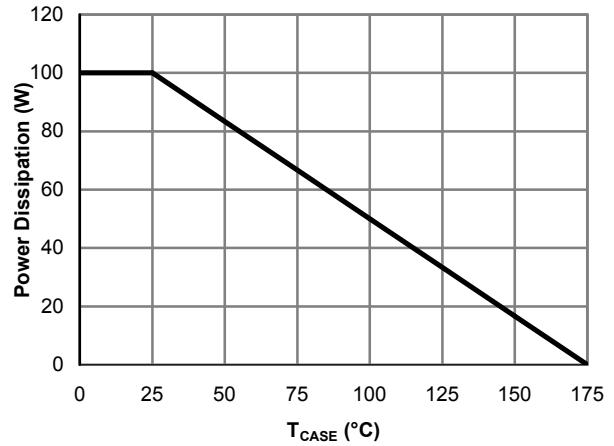


Figure 13: Power De-rating (Note B)

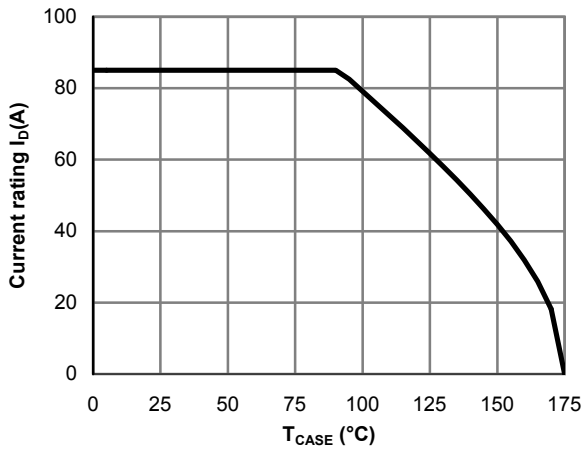


Figure 14: Current De-rating (Note B)

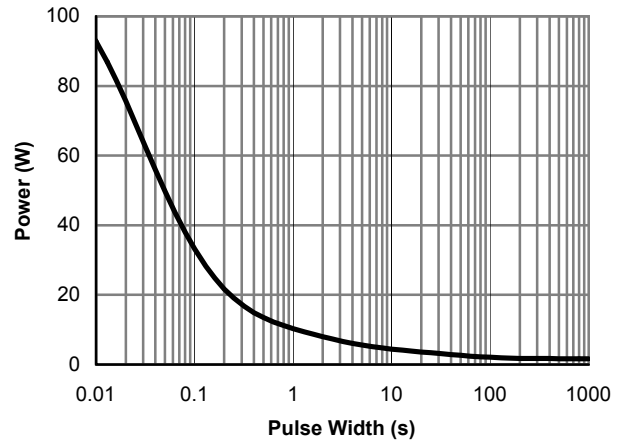


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

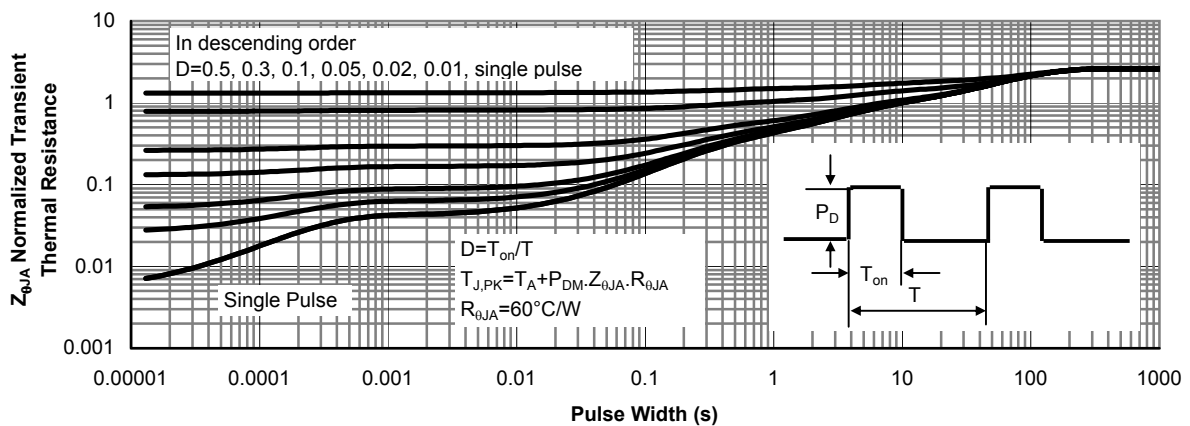
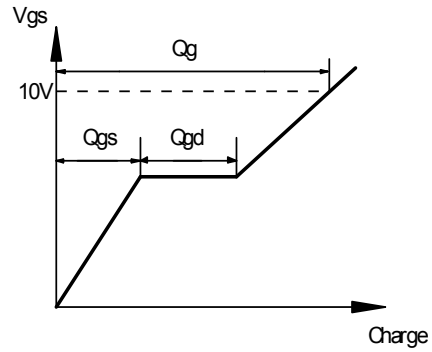
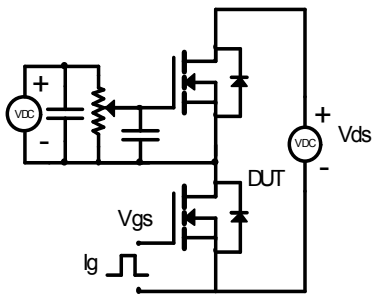
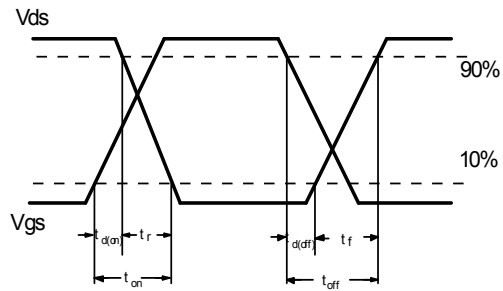
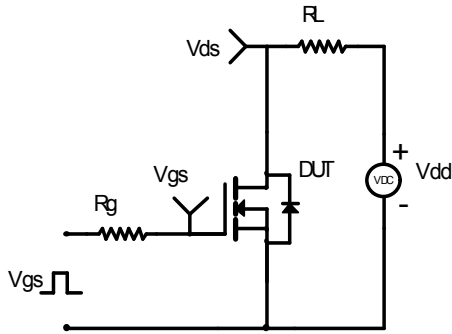


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

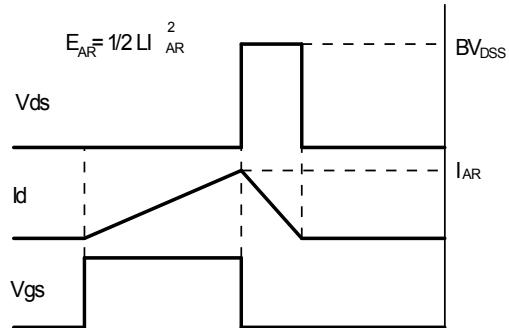
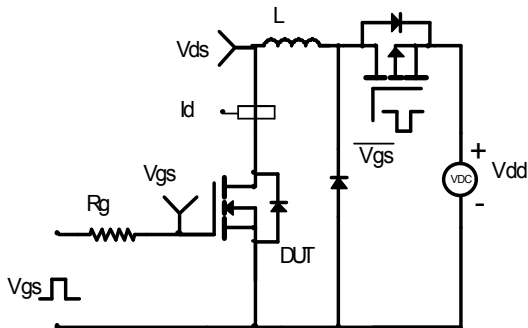
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

