



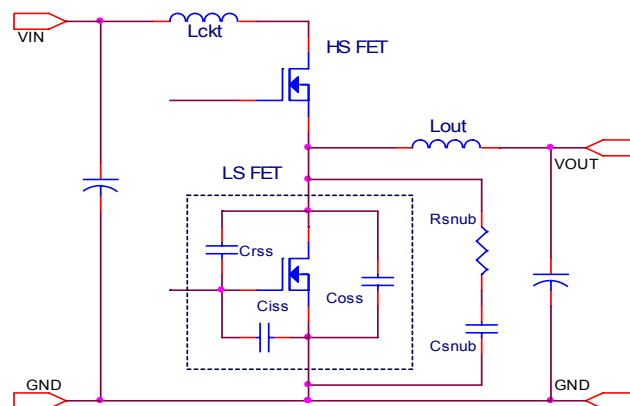
SNUBBER DESIGN FOR NOISE REDUCTION IN SWITCHING CIRCUITS

Introduction

In high frequency switching converters the designers face a common challenge of dealing with switching noise. In particular when the high side Mosfet turns on, the body diode of the low side FET, which was in conduction before, turns off. During the turn off process the body diode draws a peak reverse recovery current and then abruptly snaps off. Since there is a small but finite parasitic inductance in the circuit, the reverse recovery current will circulate through the circuit until it dies down. This will result in voltage overshoot and ringing at the phase node which is quite undesirable. If the overshoot is severe enough, the low side FET may turn on again or go into avalanche breakdown. On the other hand the ringing may cause negative spikes with respect to ground, and these spikes may get coupled to the sensitive electronic components in the load causing malfunctions. One obvious solution is to use a low side FET with an integrated Schottky diode, such as the AOS SR-FET™. The Schottky has a much lower reverse recovery current which reduces the circulating energy in the circuit to start with.

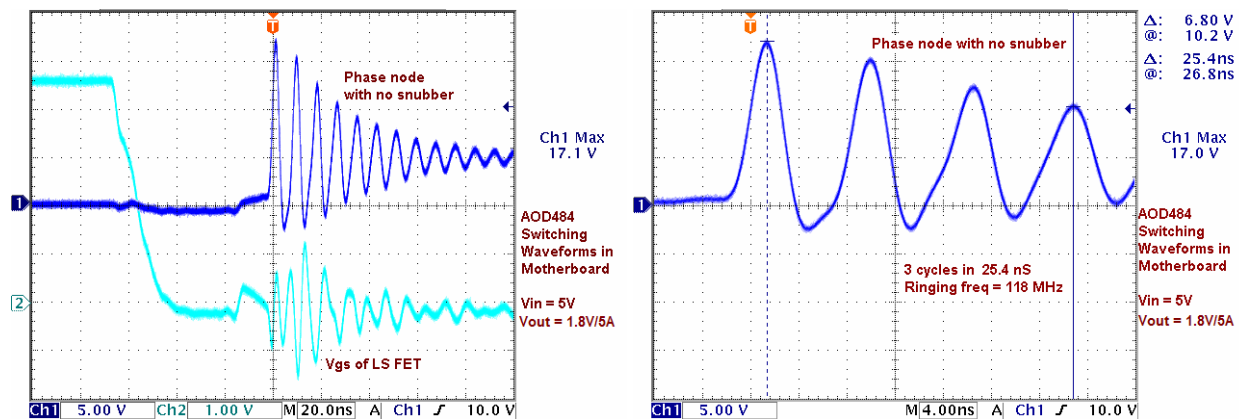
During the system design, the best way to reduce the switching noise is to minimise the parasitic inductances. The sources of parasitic inductances are the long traces between input capacitor and the switching devices. Additionally the bonding wires within power packages also contribute to the undesirable inductance. Good layout practices should be followed such as locating bypass capacitors very close to leads of switching devices, minimising the area of the primary current loop. Packages with low source inductance such as Ultra SO-8® should be used where switching noise is a major concern.

However, the parasitic inductances cannot be eliminated altogether in a practical circuit. It may not be easy to do an ideal layout in a large and complex system such as a computer motherboard. In these situations a practical solution to the ringing issue is a snubber across the phase node to ground. Here we will consider the simple RC snubber and describe how to design one for optimum performance.



Identifying the Circuit Parasitics

The schematic above is a simplified diagram of a synchronous buck converter. All the parasitic inductances have been lumped together and shown as L_{ckt} . As mentioned above they include trace inductance as well package inductances. The parasitic capacitances that ring with L_{ckt} come mainly from the output capacitor C_{oss} of the low side FET which is in the off state. Our goal is to calculate values of R_{snub} and C_{snub} as well as the power rating of the snubber resistor. The method will be illustrated with a practical example. The waveforms were taken in an auxiliary synchronous buck converter on a motherboard feeding a DDR memory. The input is 5V, output 1.8V/5A. The FETs are AOD484 in D-Pak. The picture below shows severe ringing without any snubbers in the circuit. The peak overshoot is three times the input voltage



Characteristic Impedance

From classical circuit theory it is known that the optimum value of the snubber resistor must equal the characteristic impedance of the LC circuit. In this case the capacitor value is known from the FET datasheet but the inductance is distributed all over the pc board and hard to predict. A practical way to determine L_{ckt} is to look at the ringing waveform in detail and measure its frequency. The waveform on the right above shows a ringing frequency of 118 MHz or 8.5 nS period. Since

$$T_{ring} = 2 * \pi * \text{SQRT} (L_{ckt} * C_{oss}) \quad \text{or, having measured } T_{ring}$$

$$L_{ckt} = T_{ring}^2 / (4 * \pi^2 * C_{oss})$$

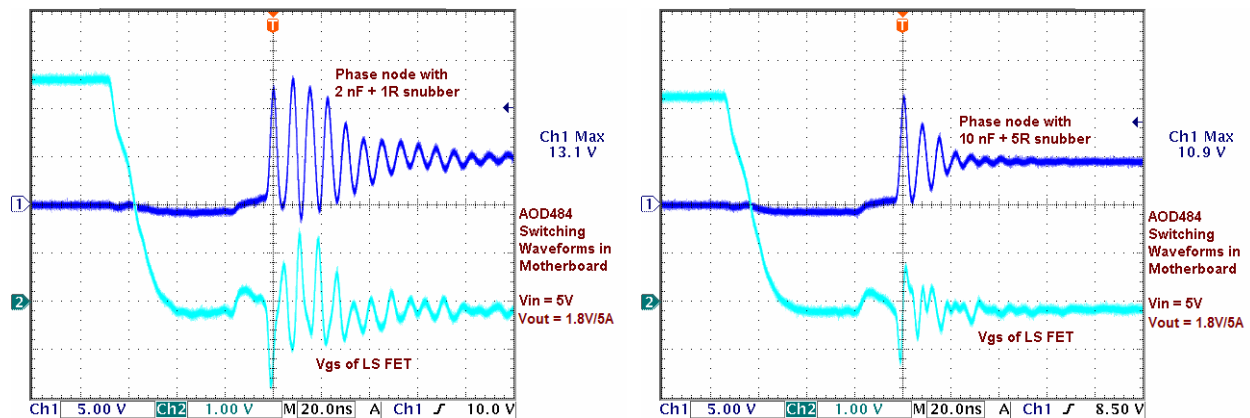
AOD484 datasheet gives the C_{oss} value as 142 pF at $V_{ds} = 15V$. However, C_{oss} is a function of V_{ds} and can be significantly higher at low supply voltages. At our supply of 5V, it is close to 220 pF, as seen from the characteristic curves. Using this value, L_{ckt} is calculated as 8.3 nH and the characteristic impedance of the freely oscillating circuit is $\text{SQRT} (L_{ckt} / C_{oss}) \cong 6 \text{ Ohm}$. This is the effective value of the desired resistance to attenuate the oscillations. Given that some resistance is already present in the circuit, we can choose 5 Ohm as the snubber resistor.

Capacitor Calculations

The snubber capacitor value is a trade off. Larger capacitor will provide overdamping and reduce the number of oscillations. But the capacitor also stores an energy of $\frac{1}{2} CV^2$ and dissipates it every cycle which has a marginal effect on efficiency. A useful parameter is the $R_{snub} \times C_{snub}$ time constant which is expressed as a multiple of the ringing period T_{ring} . The standard practice is to use a multiple of 3 or higher.

$$C_{snub} = 3 \times T_{ring} / R_{snub}$$

In our example minimum value of C_{snub} is 4.7 nF. In the motherboard a value of 10 nF was chosen to provide extra damping. Since the input is only 5V, this does not cause excessive losses in the snubber. The picture on the left below shows the effects of a lower value snubber, 2 nF + 1 Ohm. Compare it to the one on the right with the optimised snubber of 10 nF + 5 Ohm



Finally the snubber resistor should be sized for dissipating the energy stored in the capacitor

$$P_{snub} = \frac{1}{2} * C_{snub} * V_{in}^2 * F_{sw}$$

Remember that F_{sw} is the switching frequency of the converter, not that of ringing. In our case the switching frequency is 300 kHz which gives the power loss as 37 mW, less than 0.5% of output power.

Conclusion

It is worth repeating that parasitic inductance in the circuit is distributed over the entire PCB and includes the package inductances. While the snubber components are calculated assuming their effective values, there is no way to physically put them in the circuit to provide ideal damping. The best way to reduce overshoots and ringing is to actually minimise the undesirable inductances in the circuit with good layout practices. Choosing the right low side FETs with low inductance packages and/or integrated Schottky body diodes will offer additional benefits.