300 W Gaming Power Adapter with AOS AlphaZBL™, αMOS5™, and AlphaSGT™ Technology

By Miles Lin and Peter Huang

Introduction

A high-efficiency universal offline power supply is widely used in many applications, such as notebook adapters, LCD TV, ATX power, etc. With the advance in technology, the power demand for consumer electronics is getting higher and higher. In order to satisfy the 80 PLUS certification and achieve high power density, the efficiency improvement of power converters becomes critical in the selection of components. For instance, a typical cost-effective resonant power supply for a 100 W ~ 300 W notebook adapter consists of a boost PFC and an LLC converter (Figure 1). To achieve 80 PLUS Titanium efficiency, at least two issues need to be considered, which are the conduction loss of conventional bridge diode rectification and the converter light load efficiency. An AOS solution for a 300 W gaming power adapter is implemented with the AOS AlphaZBL™, αMOS5™, and AlphaSGT™ techniques as an example.

In this application note, we will make a comparison between different semiconductor products and the AOS solution to each stage of the converter, including the AC-DC rectifier, boost PFC, LLC resonant converter, and the secondary synchronous rectification. In addition, to demonstrate a higher power density solution, the thermal and efficiency performance comparison were made and revealed the switching waveforms with different parameters of MOSFET in this document.

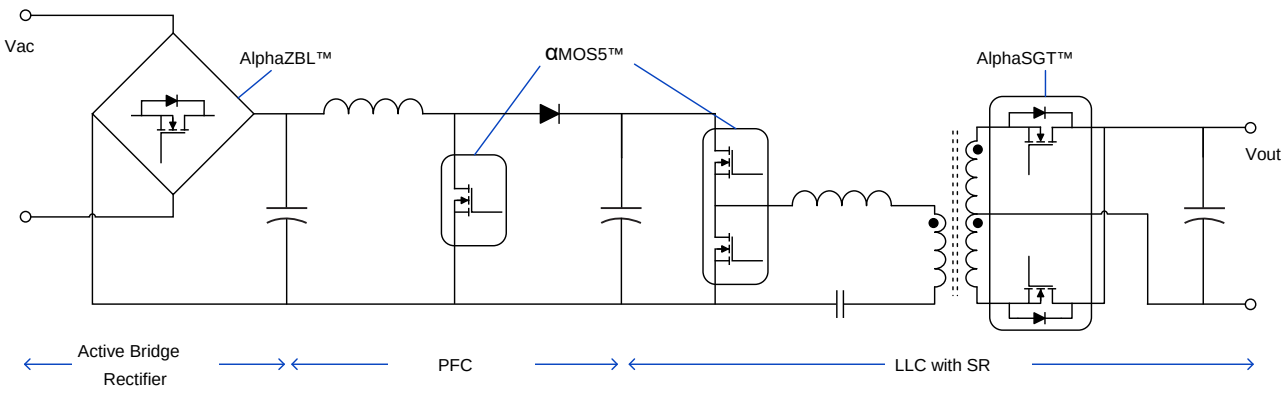

Figure 1. Circuit Diagram of AOS 300 W Gaming Adapter Solution

Table 1. Circuit Specification

Specification	Value
Input voltage	90Vac~264Vac
Input frequency	50/60 Hz
Output voltage and current	20 VDC / 15A
Output power	300 W

AlphaZBL™

Active Bridge Rectifier Stage

In a conventional PFC circuit, the bridge diode rectifier takes a large portion of system loss due to the typical 1 V forward voltage and two diodes in a conduct current path. Even if a well-designed PFC stage could achieve 98% efficiency, the loss of the bridge diode rectifier limits the overall efficiency of the power converter.

AOS AlphaZBL™ technique is a cost-effective solution that the self-powered IC, AOZ7200CI, can control the external N-channel MOSFET to replace the diode as active bridge rectification. The AlphaZBL™ board kit is implemented with the control IC, AOZ7200CI and the αMOS5™ MOSFET, AONV088A60, which has low $R_{DS(on)}$ and low V_F. See Figure 2 and Figure 3 below.

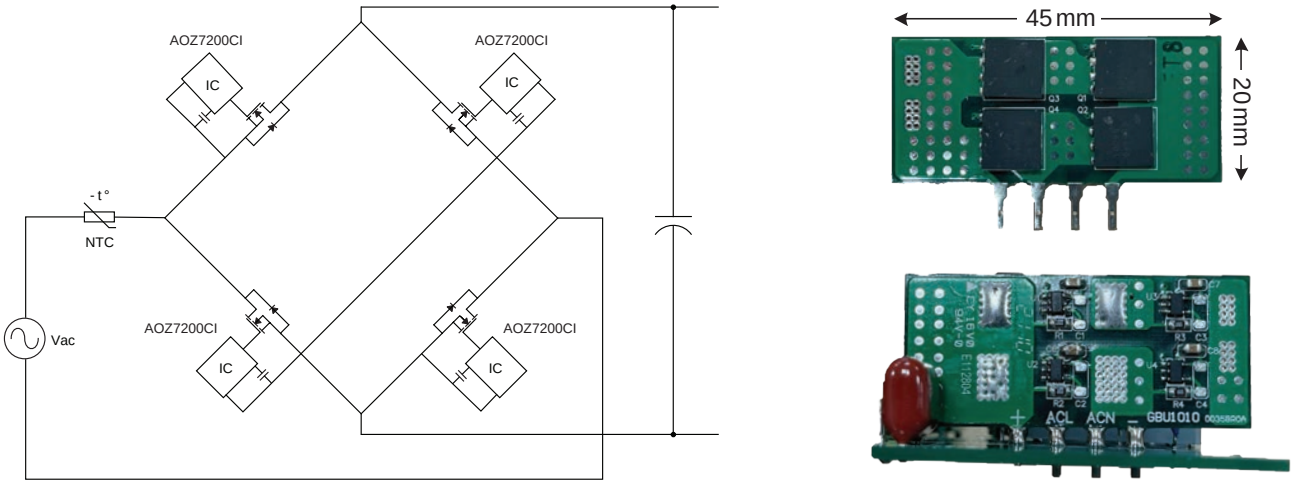

Figure 2. AlphaZBL™ Application Circuit and Board Kit

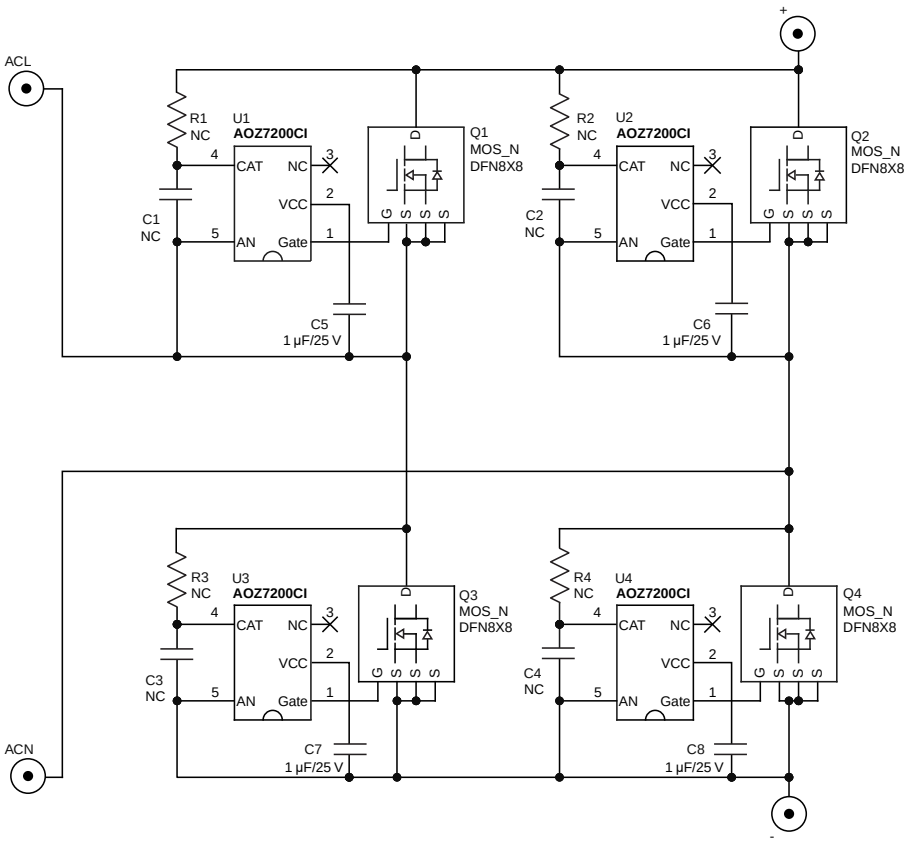

Figure 3. AlphaZBL™ Circuit Schematic

The power dissipation of the diode is:

$$P_{con.ZBL.diode} = V_F \times I_{avg.ZBL} + R_D \times I_{rms.ZBL}^{\ 2}$$

Where V_F and R_D are the forward voltage and the equivalent series resistance of the equivalent diode circuit.

The conduction loss of MOSFET is:

$$P_{con.ZBL.mosfet} = I_{rms.ZBL}^{\ 2} \times R_{DS(on)}$$

Typically, we can easily calculate the efficiency improvement of the active bridge rectifier from the above equations. However, the forward voltage and resistance of the diode change along with the temperature and current of the diode, and the on-resistance of MOSFET varies along with its junction temperature. As shown in Figure 4 and Figure 5.

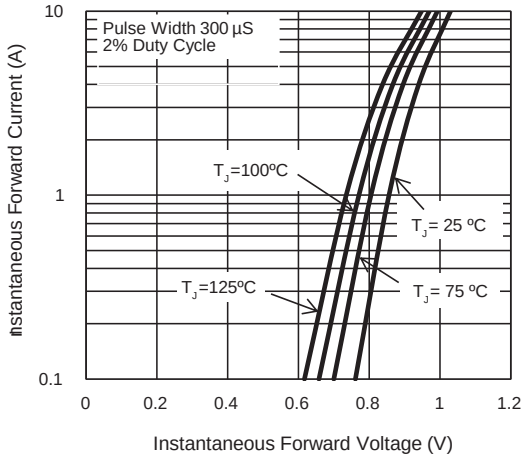

Figure 4. Typical Forward Characteristics (Ref. GB806 Datasheet)

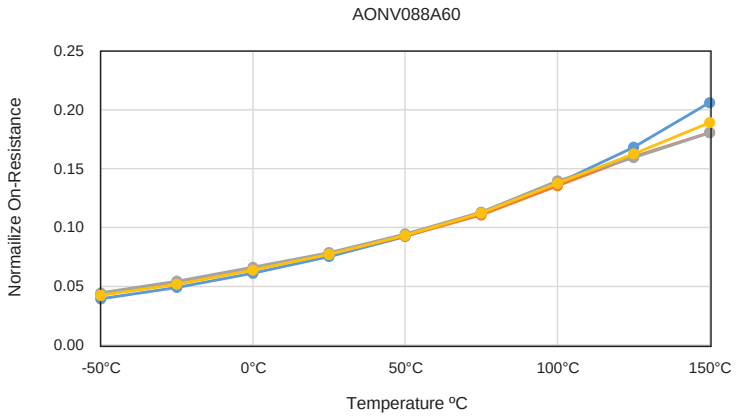

Figure 5. On-resistance vs. Junction Temperature

The power loss comparison is calculated as shown in Figure 6, assuming the same operating temperature. Because of the opposite temperature coefficient between diode and MOSFET, the high-temperature operating condition will degrade the benefit of efficiency improvement in active bridge rectification. Thus, the MOSFET selection for an active bridge rectifier is considered the smallest $R_{DS(on)}$ to ensure the smallest conduction loss and temperature rise. The switching loss of MOSFET can be ignored due to the low-frequency condition.

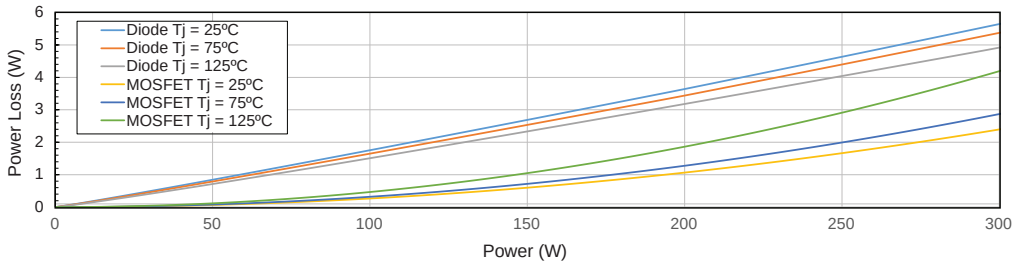

Figure 6. Power Loss Comparison Under the Same Junction Temperature

AONV088A60 with typical 75 mΩ on-resistance is used. A comparison between the AlphaZBL™ solution and conventional bridge diode rectifier was made. In Figure 7, the efficiency curves of the total supply show the AlphaZBL™ solution has better efficiency for the whole operation range. In addition, the thermal performance is good instead of a bridge diode rectifier (Figure 8). The heat sink is removed in the AlphaZBL™ board kit; hence, the volume of the power stage can be further reduced.

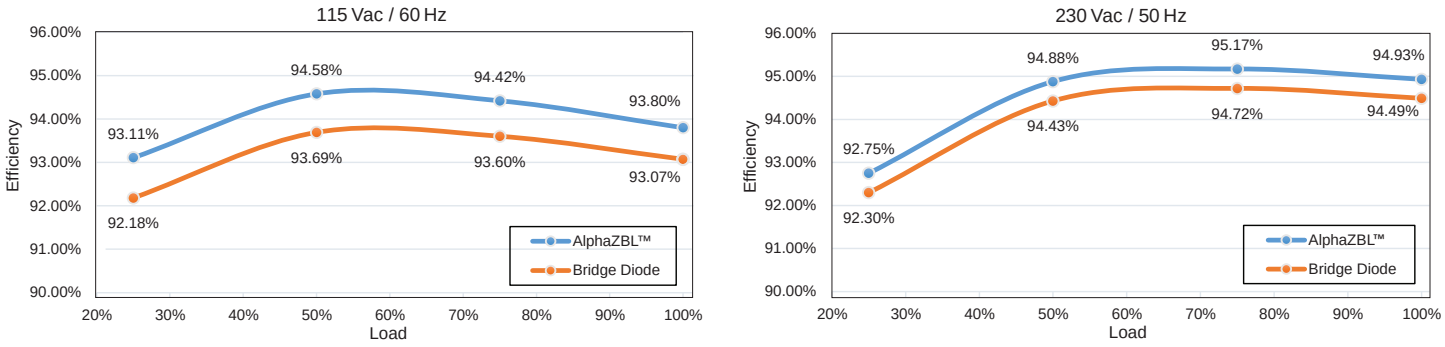

Figure 7. Adapter Efficiency Comparison by Replacing AlphaZBL™ and Bridge Diode Rectifier

Table 2. Efficiency Comparison Details

Input voltage	Parts	25% Load	50% Load	75% Load	100% Load	Avg
115 Vac/60 Hz	AlphaZBL™	93.11%	94.58%	94.42%	93.80%	93.98%
	Bridge diode	92.18%	93.69%	93.60%	93.07%	93.14%
230 Vac/50 Hz	AlphaZBL™	92.75%	94.88%	95.17%	94.93%	94.43%
	Bridge diode	92.30%	94.43%	94.72%	94.49%	93.98%

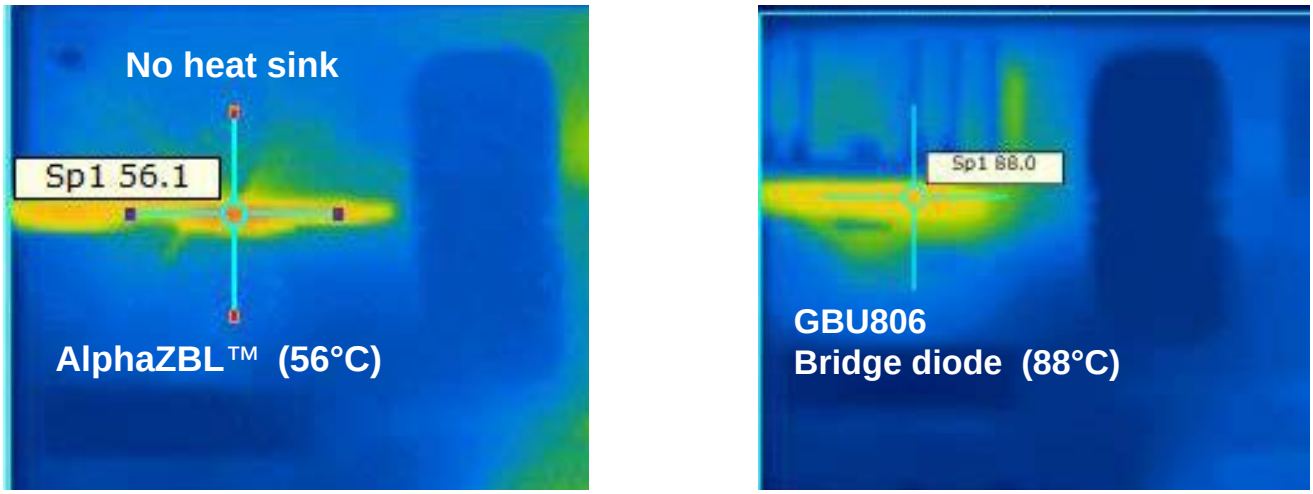

Figure 8. Thermal Performance at 115 Vac and Full Load

αMOS5™ MOSFET

PFC Stage

For 75~300 W applications, the BCM/QR/DCM boost PFC can achieve better efficiency and low cost than the CCM boost PFC. In addition, the valley switching or ZVS operation can reduce the turn-on switching loss of the boost switch. But the high ripple current makes the converter has a high peak current when turn-off hard switching and the conduction loss penalty of boost switch. Hence, the turn-off and conduction losses reduction will be significant considerations for high-efficiency design.

The circuit schematic of the BCM boost PFC with valley voltage switching operation is shown in Figure 9. The αMOS5™ MOSFETs, AONV110A60, are connected in parallel as the main switch of boost PFC. The design consideration of the boost PFC converter will not be discussed in this application note and will only describe the loss of MOSFET.

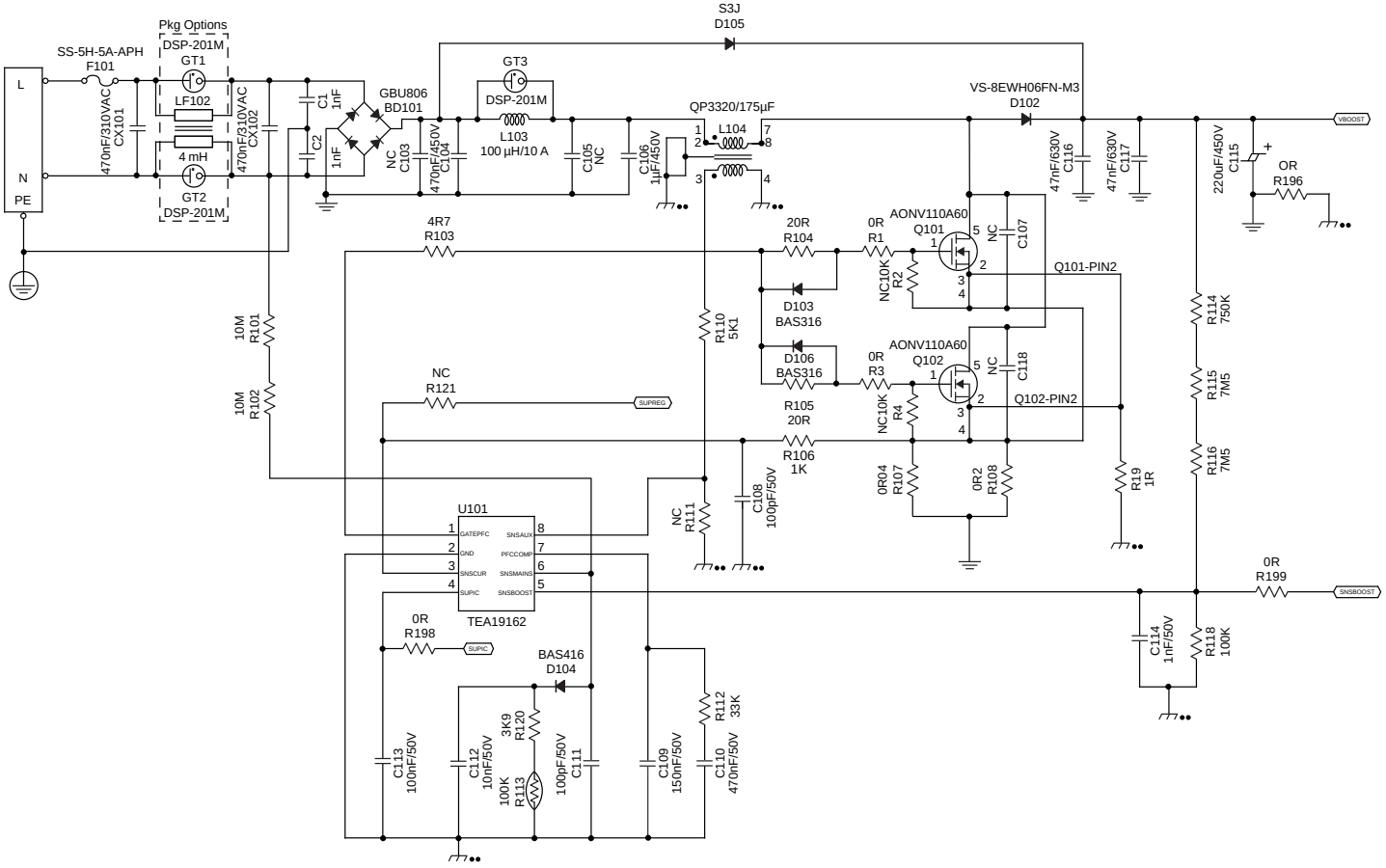

Figure 9. PFC Circuit schematic

The turn-off loss of MOSFET is:

$$P_{off.PFC.mos} = V_{O.PFC} \times I_{PFC.inpk.avg} \times t_{off.mos} \times f_{s.avg}$$

The average input peak current and the turn-off time are given as:

$$I_{PFC.inpk.avg} = \frac{4\sqrt{2} \times P_{O.PFC}}{\eta \times \pi \times V_{in.(ac)}}$$

$$t_{off.mos} \approx R_g \times C_{rss} \left(\frac{V_{ds} - V_{miller}}{V_{miller}} \right) + R_g \times C_{iss} \times ln \left(\frac{V_{miller}}{V_{th}} \right)$$

The average switching frequency and turn-on period are:

$$f_{s.avg} = \frac{1}{\pi}\int_0^{\pi}\frac{1}{T_{on.PFC}}\left(1-\frac{\sqrt{2}\times V_{in.(ac)}}{V_{O.PFC}}\sin\theta\right)d\theta$$

$$T_{on.PFC} = \frac{2\times P_{O.PFC}\times L_{PFC}}{\eta\times V_{in.(ac)}^{\ 2}}$$

In addition, the measured turn-off loss includes the energy used to charge C_{gd} and C_{ds}. Therefore, the high E_{OSS} can help to reduce the actual turn-off loss of switches.

$$E_{off} = E_{off(measured)} - E_{oss}$$

On the other hand, the actual turn-on loss needs to plus the measured loss and the energy used to discharge C_{gd} and C_{ds}. Thus, the low E_{OSS} at low voltage can help to reduce the actual turn-on loss when valley switching.

$$E_{on} = E_{on(measured)} + E_{oss}$$

Conduction loss of MOSFET is given as:

$$P_{cond.PFC.mos} = I_{rms.PFC.mos}^{\ 2}\times R_{DS(on)}$$

$$I_{rms.PFC.mos} = I_{PFC.inpk}\times\sqrt{\frac{1}{6}-\frac{4\sqrt{2}}{9\pi}\times\frac{V_{in.(ac)}}{V_{O.PFC(dc)}}}$$

$$I_{PFC.inpk} = \frac{2\sqrt{2}\times P_{O.PFC}}{\eta\times V_{in.(ac)}}$$

Where,

η = Efficiency of PFC converter

R_g = The sum of internal and external gate resistance

V_{miller} = Miller plateau of MOSFET

V_{th} = Gate threshold voltage of MOSFET

In the PFC stage, the αMOS5™, AONV110A60, is used and compared with the other two manufacturers' products.

Table 3. Parameters Comparison

Parts		AONV110A60		Competitor #1		Competitor #2	
BV_{DSS} (V)		600	V_{GS}=0V, I_D=250μA, T_j=25°C	600	V_{GS}=0V, I_D=1mA	600	V_{GS}=0V, I_D=1mA
$V_{GS(th)}$ (V)		3	V_{DS}=5V, I_D=250μA	3.5	V_{DS}=V_{GS}, I_D=0.41mA	4	V_{DS}=V_{GS}, I_D=250μA
$R_{DS(on).max}$ (mΩ)		110	V_{GS}=10V, I_D=19A	125	V_{GS}=10V, I_D=8.2A, T_j=25°C	137	V_{GS}=10V, I_D=10.5A
C_{iss} (pF)		4010	V_{GS}=0V, V_{DS}=100V, f=1MHz	1544	V_{GS}=0V, V_{DS}=400V, f=250kHz	1515	V_{GS}=0V, V_{DS}=100V, f=1MHz
C_{oss} (pF)		105		26		128	
C_{rss} (pF)		1.2		7		4.2	
R_g (Ω)		5.5	f=1MHz	7	f=1MHz, open drain	1.5	f=1MHz, I_D=0A
Q_{gs} (nC)		28	V_{DS}=480V, I_D=19A, V_{GS}=10V	8	V_{DD}=400V, I_D=8.2A, V_{GS}=0 to 10V	7.2	V_{DD}=480V, I_D=25A, V_{GS}=0 to 10V
Q_{gd} (nC)		24		11		16	
Q_g (nC)		78		36		33	
E_{oss}(#) (μJ)	V_{DS}=50V (@ turned-on)	1.28		1.33		2.84	
	V_{DS}=250V (@ turned-on)	4.0		2.4		5.4	
	V_{DS}=400V (@ turned-off)	7.7		3.89		8.23	
R_{thJC} (°C/W)		0.2		1.13		0.83	
R_{thJA} (°C/W)		40		35		45	

Note:
(#) measured results

It can be found that the αMOS5™ has a small on-resistance to reduce the conduction loss. The low E_{OSS} at low voltage can help to reduce the turn-on loss for valley voltage switching operation. The E_{OSS} at high voltage increases higher, resulting in the reduction of the turn-off loss. The AONV110A60 has the smallest junction-to-case thermal resistance that has better heat dissipation. These features make αMOS5™ suitable for zero/low voltage turn-on and high current turn-off applications.

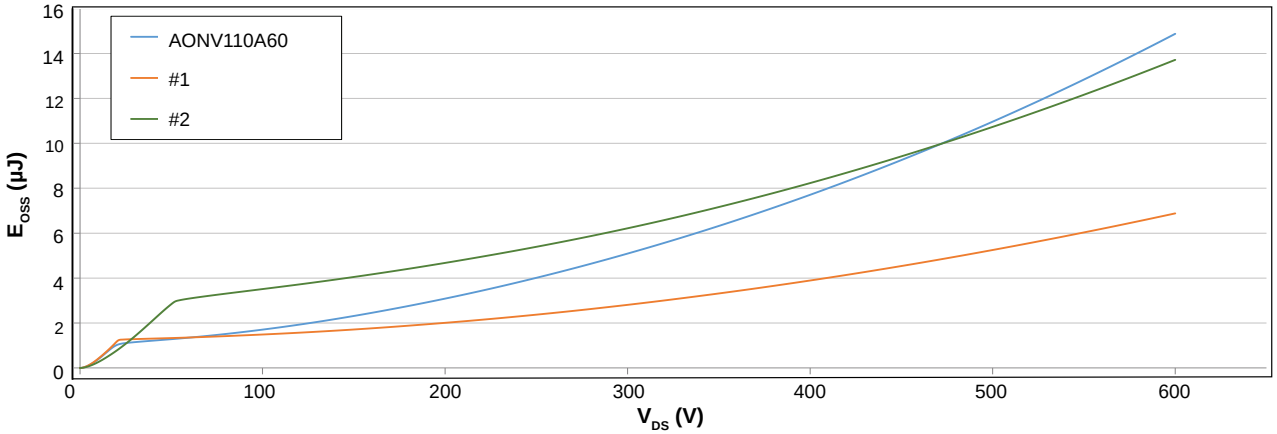

Figure 10. E_{OSS} Comparison

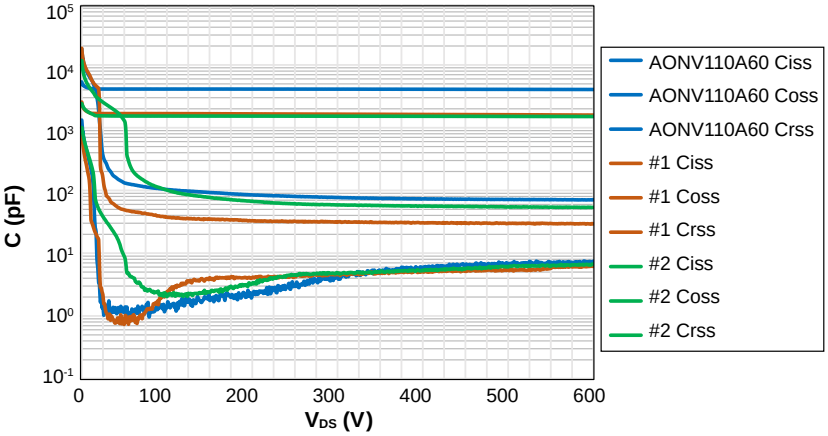

Figure 11. Capacitance Curve Comparison

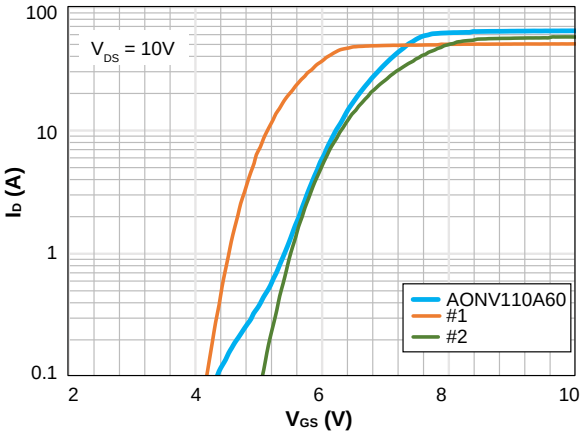

Figure 12. Transfer Characteristic

Figure 13 shows the turn-off waveforms, and Figure 14 shows the turn-on waveforms at different operating conditions. Because of large C_{OSS}, the AOS solution has lower dv/dt at both turn-on and turn-off operation. In Figure 14, Competitor #2 has a larger valley voltage at low-line 115 Vac condition because the C_{OSS} suddenly increased around 50 V (Figure 11). At high-line 230 Vac condition, the delayed turn-on occurred in the AOS solution due to larger C_{ISS} than others. However, the C_{OSS} characteristic helps to slow down the drain-source voltage charging, and the valley voltage has slightly increased at full load conditions.

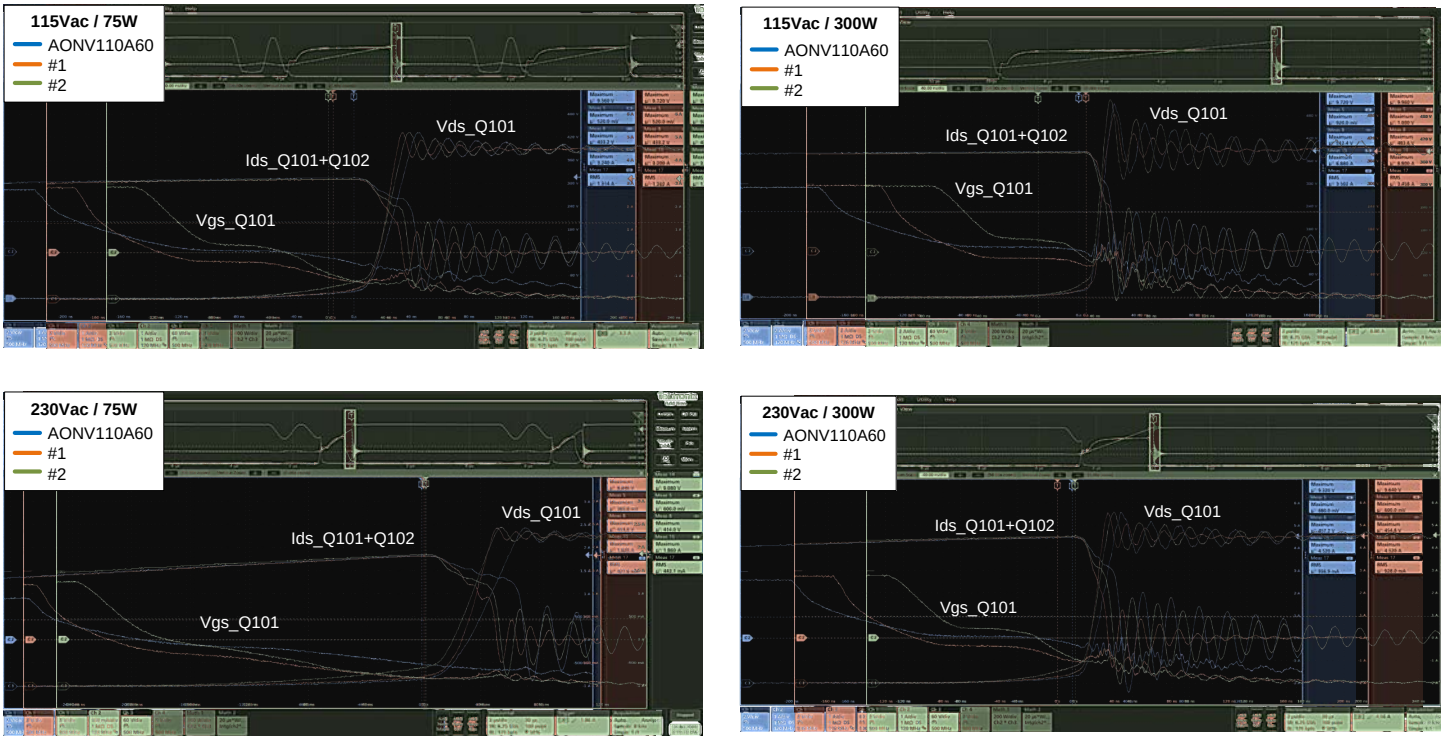

Figure 13. PFC MOSFET Turn-off Waveform

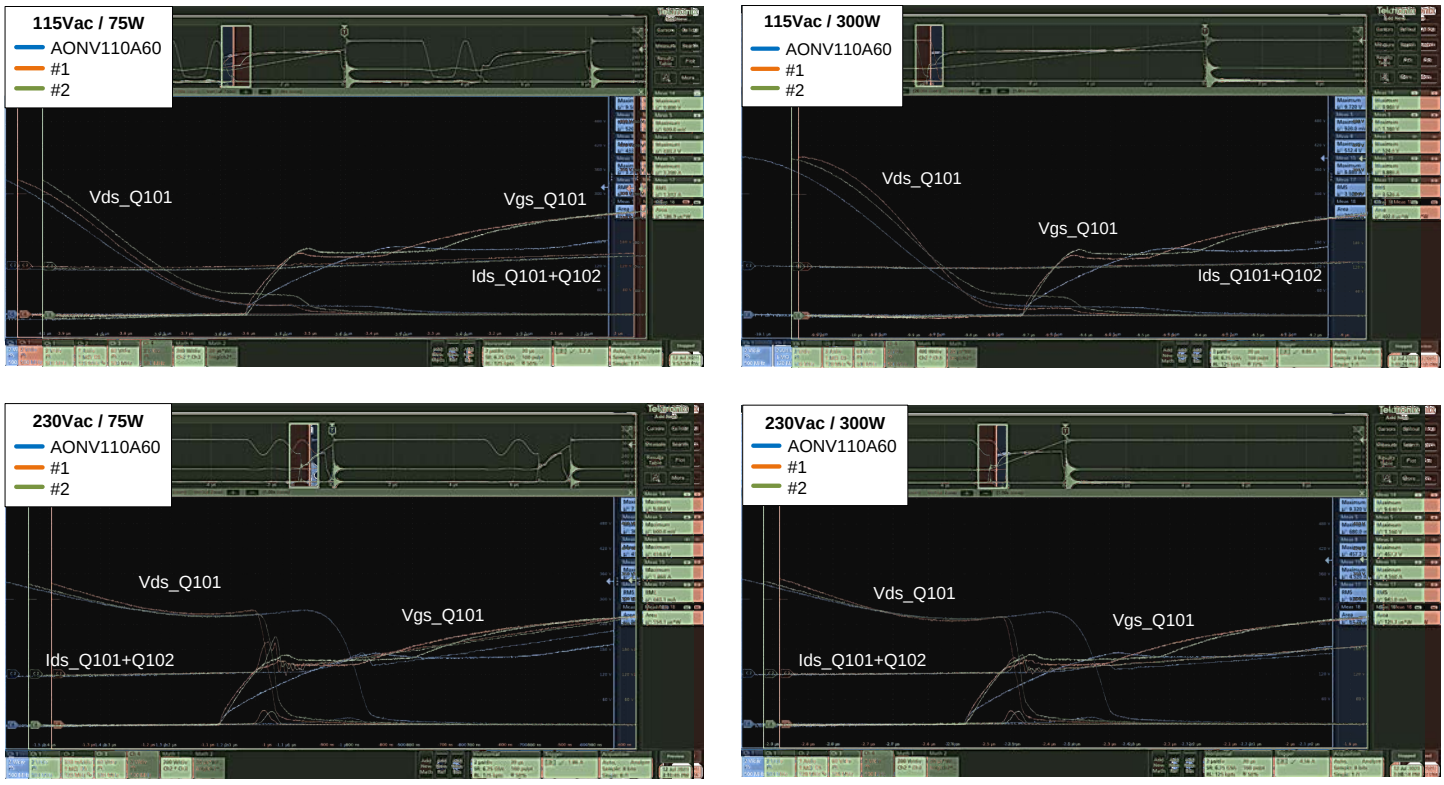

Figure 14. PFC MOSFET Turn-on Waveform

Figure 15 and Table 3 show the efficiency comparison between αMOS5TM and competitors #1, #2. The AOS solution has better thermal performance, as shown in Figure 16 and Figure 17.

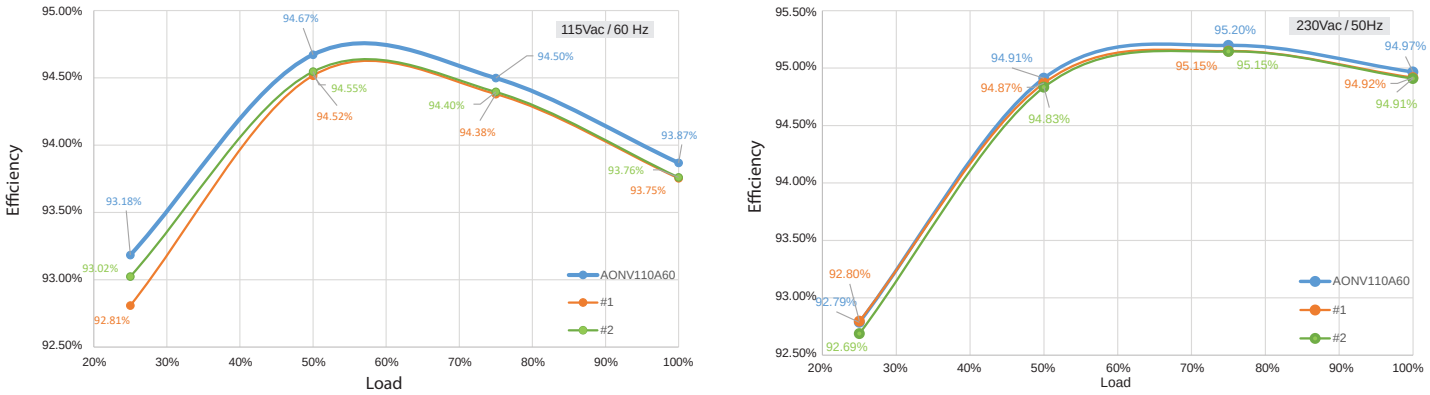

Figure 15. Adapter Efficiency Comparison by Replacing the Main Switch of Boost PFC

Table 4 Efficiency Comparison Details.

Input voltage	Parts	25% Load	50% Load	75% Load	100% Load	Avg
115 Vac/60 Hz	AONV110A60	93.18%	94.67%	94.50%	93.87%	94.06%
	#1	92.81%	94.52%	94.38%	93.75%	93.86%
	#2	93.02%	94.55%	94.40%	93.76%	93.93%
230 Vac/50 Hz	AONV110A60	92.79%	94.91%	95.20%	94.97%	94.47%
	#1	92.80%	94.87%	95.15%	94.92%	94.43%
	#2	92.69%	94.83%	95.15%	94.91%	93.39%

AONV110A60 **#1** **#2**

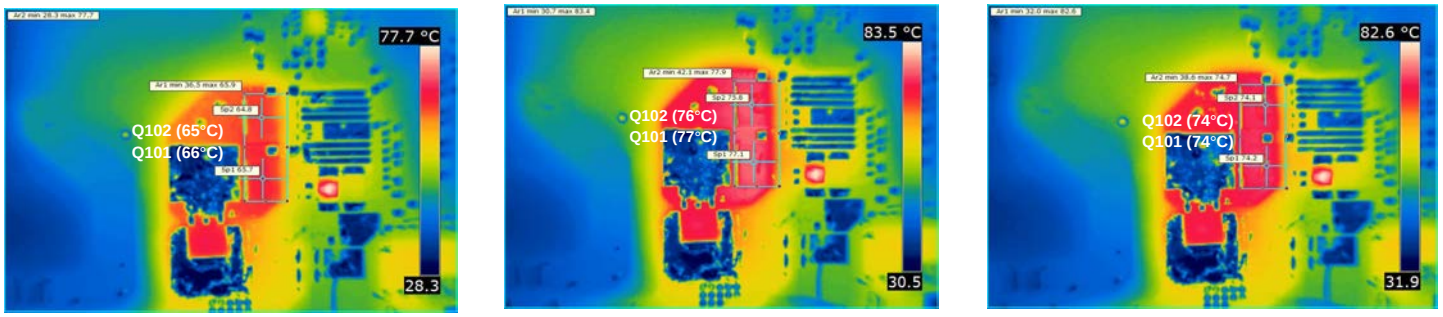

Figure 16. Thermal Performance at 115 Vac and Full Load

AONV110A60 **#1** **#2**

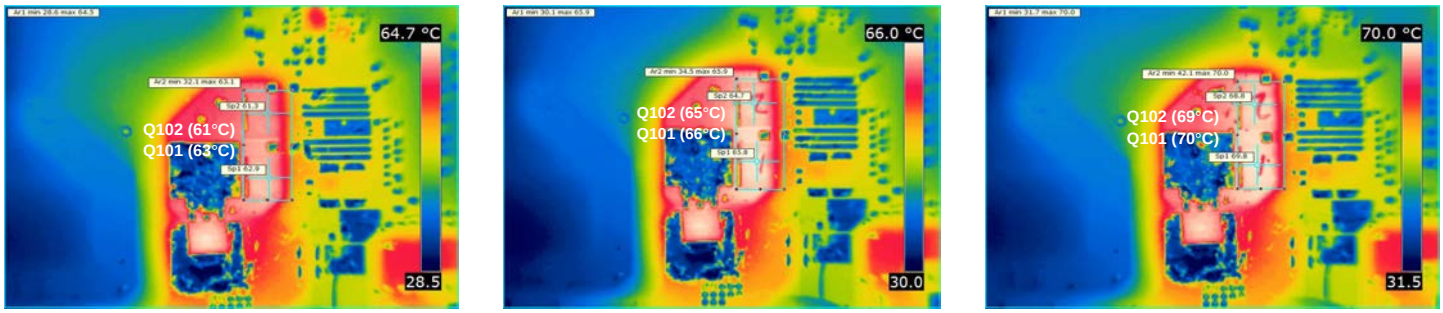

Figure 17. Thermal Performance at 230 Vac and Full Load

αMOS5™ MOSFET

Primary Switches of LLC Stage

After the PFC stage, a typical half-bridge LLC converter is connected to supply the output voltage. Zero voltage switching can be realized over the full load range, and synchronous rectification control can be used on the secondary side to improve converter efficiency. Thus, the turn-off and conduction losses dominate the loss of primary side switches. The design consideration of the LLC converter will not be discussed in this application note and will only describe the loss of MOSFET.

Typically, the high K value of the LLC converter design can help to reduce the RMS current of the switch due to the higher magnetizing inductance. However, the operating frequency range is increasing, which makes the design challenge of the magnetic component, and high L_m also limits the ZVS range at high-line conditions.

The ratio of magnetizing inductance and series-connected resonant inductance K is given as:

$$K = \frac{L_m}{L_r}$$

The recommended range is 3~7. Here, K=5 is chosen.

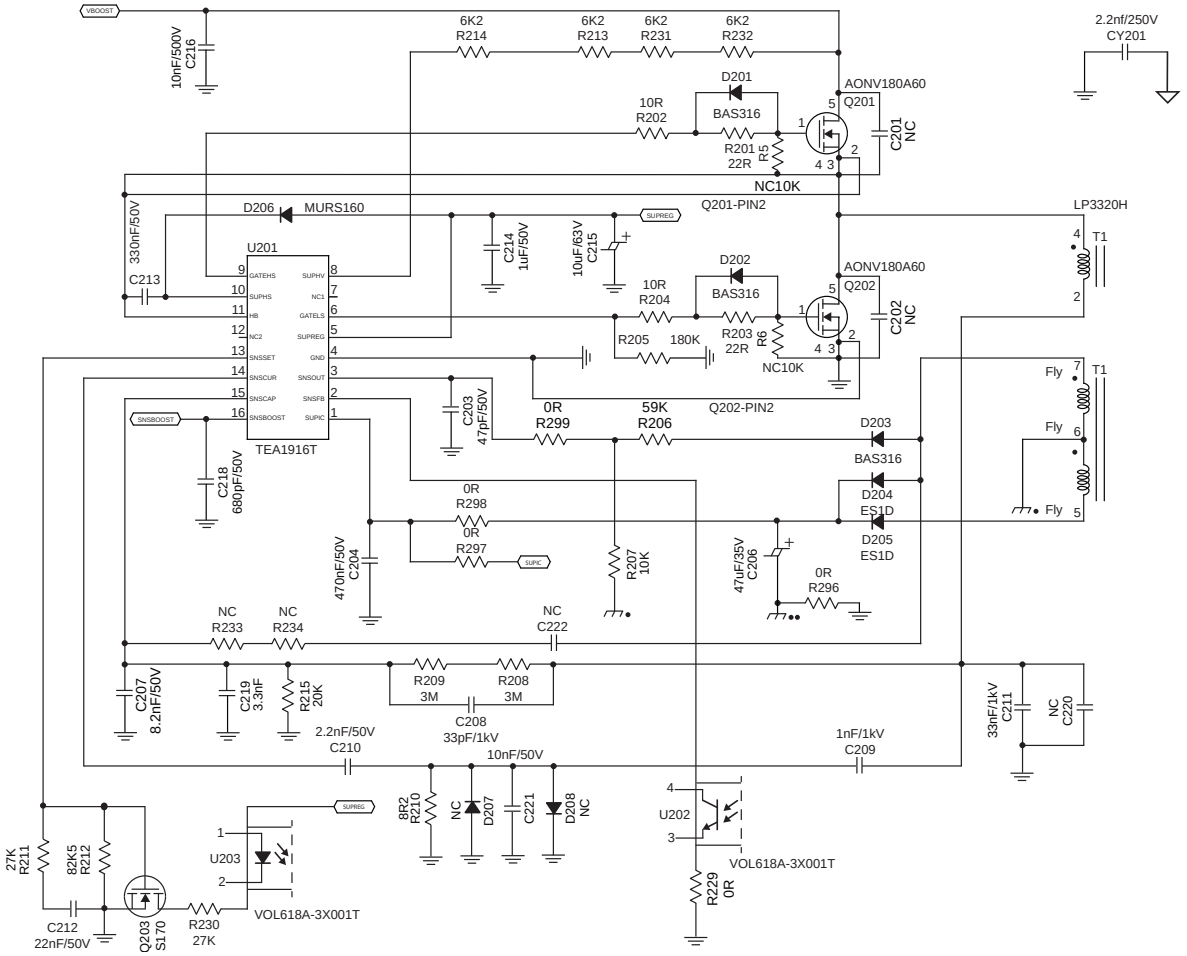

Figure 18. Circuit Schematic of Half-bridge LLC Primary Side

Conduction loss of MOSFET is:

$$P_{con.LLC.mos} = I_{rms.LLC.loss}^{2} \times R_{DS(on)}$$

$$I_{rms.LLC.mos} = \frac{1}{\eta \times 2} \times \sqrt{\left(\frac{V_{O.LLC\,(dc)} \times \pi}{R_{LOAD} \times 2n}\right)^2 + \left(\frac{n \times V_{O.LLC\,(dc)}}{2 \times L_m \times 2 \times f_r}\right)^2}$$

The design turns-ratio of the transformer is:

$$n = \frac{V_{in.max.LLC\,(dc)}}{2 \times V_{O.LLC\,(dc)}}$$

When the $f_s = f_r$, the turn-off switching loss of MOSFET is:

$$P_{off.LLC.mos} \approx \frac{1}{2} \times \frac{n \times V_{O.LLC\,(dc)}}{2 \times L_m \times 2 \times f_r} \times V_{O.PFC\,(dc)} \times t_{off.mos} \times f_s$$

$$t_{off.mos} \approx R_g \times C_{rss} \left(\frac{V_{ds} - V_{miller}}{V_{miller}}\right) + R_g \times C_{iss} \times ln\left(\frac{V_{miller}}{V_{th}}\right)$$

Design of ZVS:

$$\frac{1}{2} \times \left(L_m + L_r\right) \times I_{Lmpk}^{2} \geq \frac{1}{2} \times \left(2C_{eq}\right) \times V_{in.LLC}^{2}$$

Total gate driver loss is:

$$P_{driver} = 2 \times C_{iss@0V} \times V_g^{2} \times f_s$$

Where,

- η = Efficiency of PFC converter
- R_{Load} = Output load resistance
- L_m = Magnetizing inductance of the transforme
- L_r = Resonant inductance
- f_r = Frequency of resonant tank
- f_s = Switching frequency
- I_{Lmpk} = Peak current of magnetizing inductance
- C_{eq} = Equivalent capacitance of the parasitic capacitance and CDS of MOSFET
- R_g = The sum of internal and external gate resistance
- V_{miller} = Miller plateau of MOSFET
- V_{th} = Gate threshold voltage of MOSFET

In the LLC stage, the αMOS5™, AONV180A60, is used and compared with the other two manufacturers' products. The comparison includes:

Table 5. Parameters Comparison

Parts	AONV180A60		Competitor #1		Competitor #2	
BV_{DSS} (V)	600	I_D=250µA, V_{GS}=0V, T_j=25°C	600	I_D=1mA, V_{GS}=0V	600	I_D=10mA, V_{GS}=0V
$V_{GS(th)}$ (V)	3	V_{DS}=5V, I_D=250µA	3.5	V_{DS}=V_{GS}, I_D=0.28mA	3.7(max)	V_{DS}=10V, I_D=0.79mA
$R_{DS(on).max}$ (mΩ)	180	V_{GS}=10V, I_D=12A	185	V_{GS}=10V, I_D=5.6A, T_j=25°C	190	V_{GS}=10V, I_D=7.9A
C_{iss} (pF)	2340	V_{GS}=0V, V_{DS}=100V, f=1MHz	1081	V_{GS}=0V, V_{DS}=400V, f=250kHz	1350	V_{GS}=0V, V_{DS}=300V, f=1MHz
C_{oss} (pF)	62		19		35	
C_{rss} (pF)	1.3		5	Read from datasheet Figure when V_{GS}=0V, V_{DS}=400V, f=250kHz	4	
R_g (Ω)	5.4	f=1MHz	11	f=1MHz, open drain	6	f=1MHz, open drain
Q_{gs} (nC)	17	V_{GS}=10V, V_{DS}=480V, I_D=12A	6	V_{DD}=400V, I_D=5.6A, V_{GS}=0 to 10V	9	V_{DD}≈400V, I_D=15.8A V_{GS}=10V
Q_{gd} (nC)	14		8		16	
Q_g (nC)	46		25		38	
Q_{rr} (µC)	7.3	I_F=12A, dI/dt=100A/µs, V_{DS}=400V	1.3	V_R=400V, I_F=2A, dIF/dt=100A/µs	2.9	I_{DR}=7.9A, V_{GS}=0V -dIDR/dt=100A/µs
E_{oss} (µJ) (#) V_{DS}=400V @ turned-off	4.9		2.5		4.7	
R_{thJC} (°C/W)	0.31		1.53		0.9	
R_{thJA} (°C/W)	40		35		-	

Note:

(#) measured results

It can be found that the αMOS5™ has a small on-resistance to reduce the conduction loss. The high EOSS at high voltage helps to reduce the turn-off switching loss to improve the efficiency, especially when the converter is operated at the light-load condition. The AONV180A60 has the smallest junction-to-case thermal resistance that has better heat dissipation.

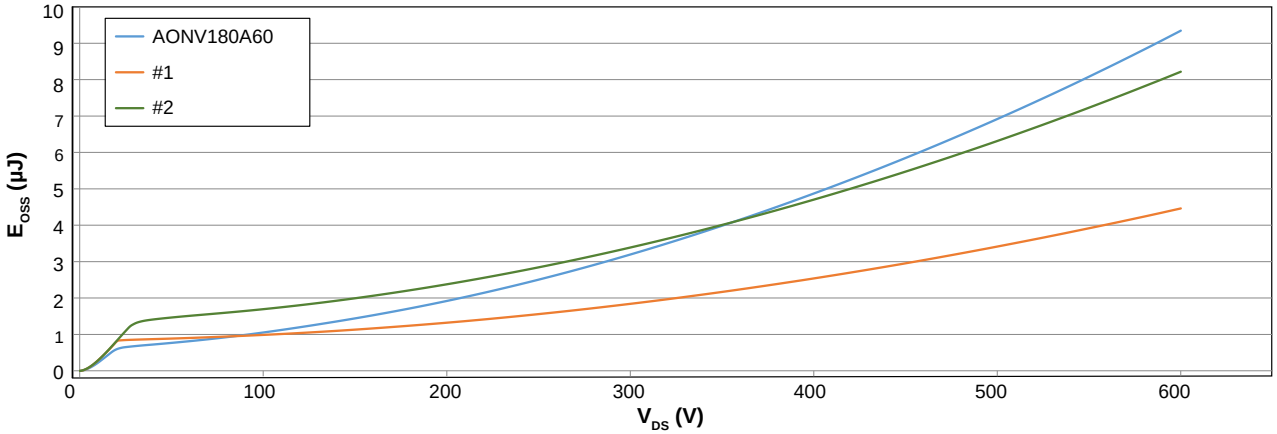

Figure 19. E_{OSS} Comparison

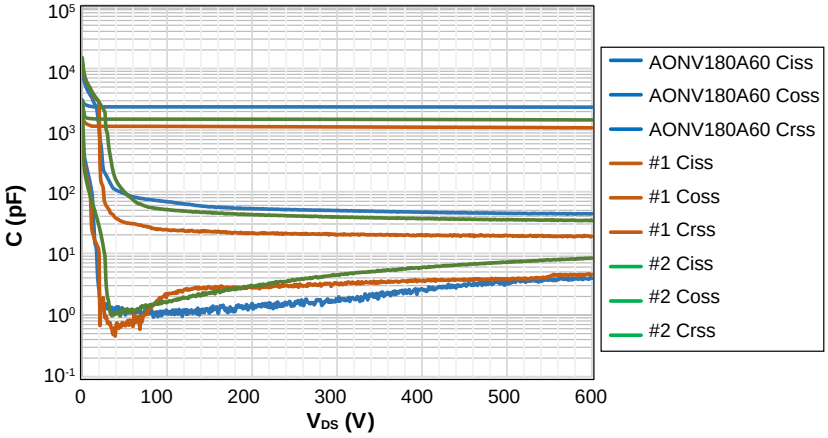

Figure 20. Capacitance Curve Comparison

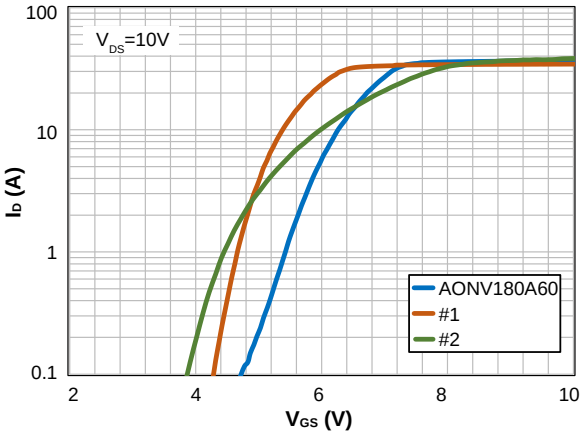

Figure 21. Transfer Characteristic

The MOSFET switching waveforms are demonstrated under 230 Vac only because the input voltage of LLC is regulated by the PFC stage. From Figure 22 and Figure 23, the AOS solution has a smaller dv/dt due to a larger COSS. Figure 24 and Table 6 show the adapter efficiency comparison. The AOS solution has around 0.1 ~ 0.2% improvement at light load. Also, it has the lowest temperature when the converter is operated at full load condition (Figure 25).

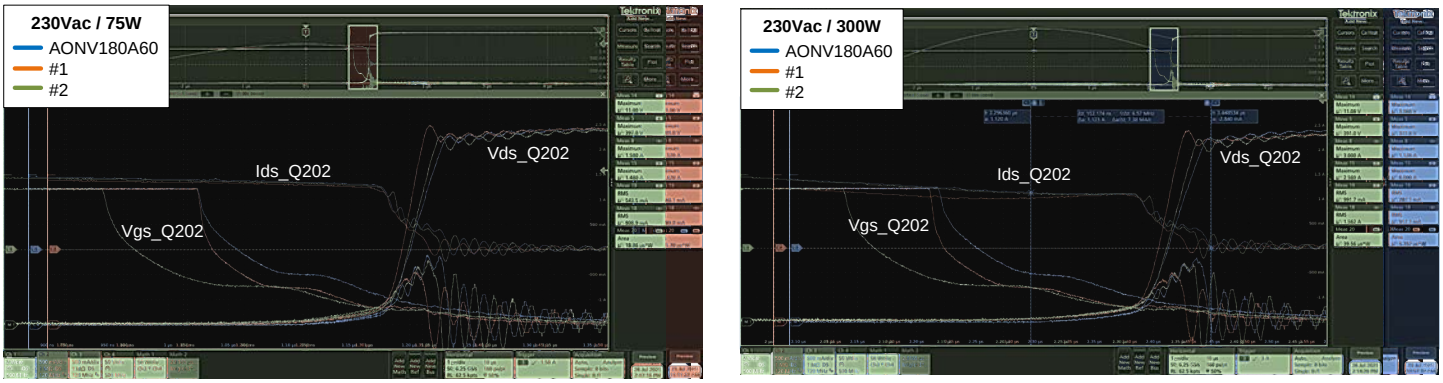

Figure 22. MOSFET Turn-off Waveform at 230 Vac Light Load and Full Load

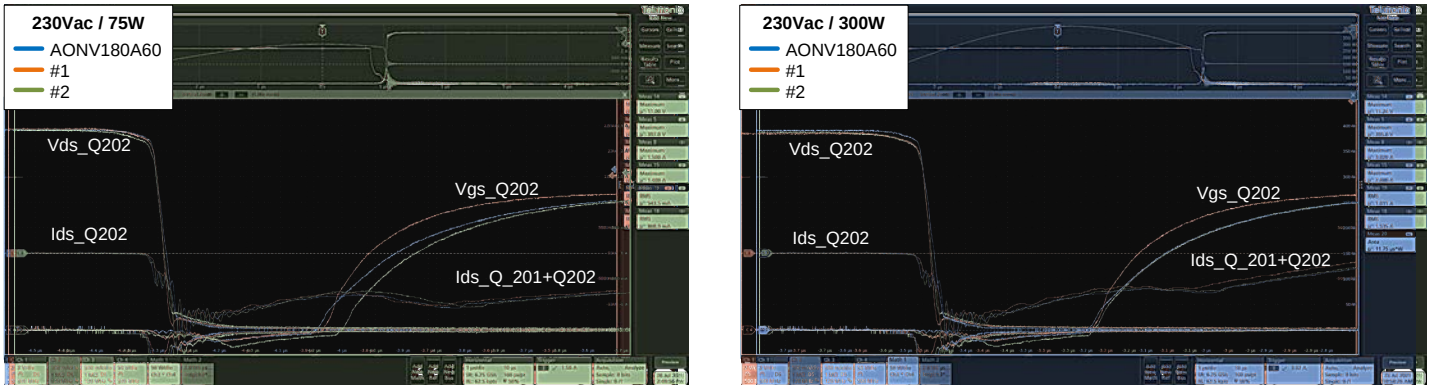

Figure 23. MOSFET Turn-on Waveform at 230 Vac Light Load and Full Load

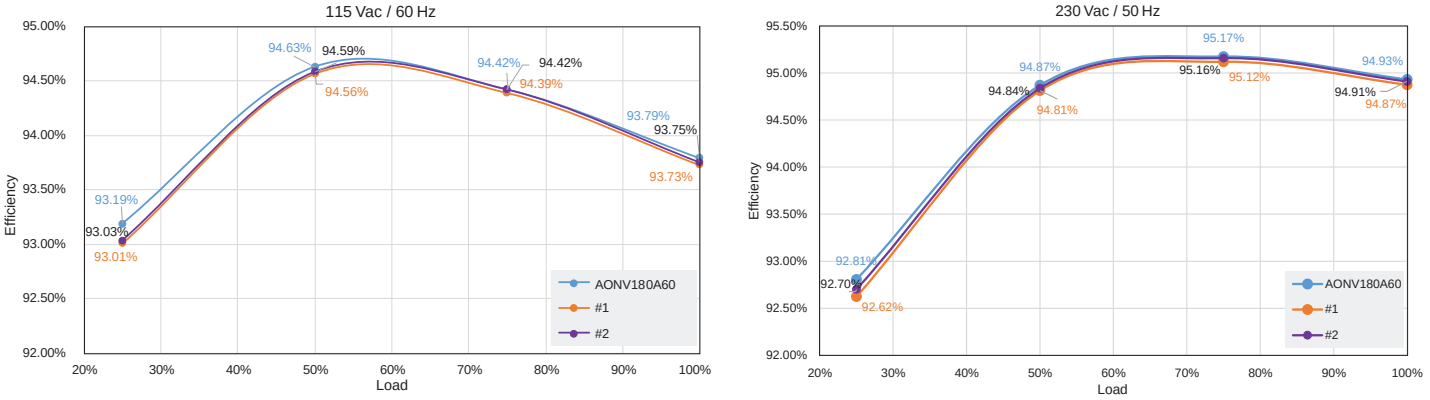

Figure 24. Adapter Efficiency Comparison by Replacing the Primary Side Switches of LLC

Table 6. Efficiency Comparison Details

Input voltage	Parts	25% Load	50% Load	75% Load	100% Load	Avg
115 Vac/60 Hz	AONV180A60	93.19%	94.63%	94.42%	93.79%	94.01%
	#1	93.01%	94.56%	94.39%	93.73%	93.92%
	#2	93.03%	94.59%	94.42%	93.75%	93.95%
230 Vac/50 Hz	AONV180A60	92.81%	94.87%	95.17%	94.93%	94.44%
	#1	92.62%	94.81%	95.12%	94.87%	94.36%
	#2	92.70%	94.84%	95.16%	94.91%	94.40%

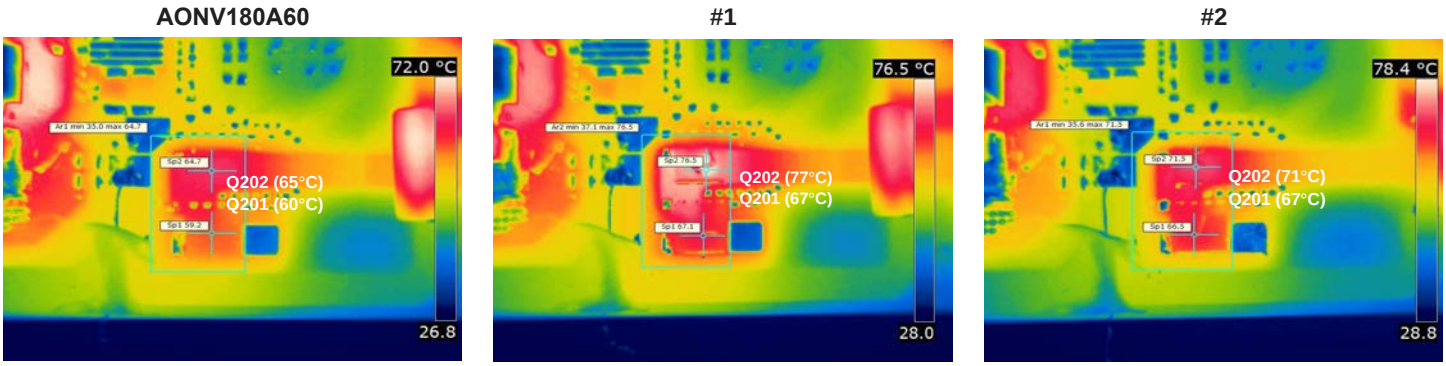

Figure 25. Thermal Performance at 230 Vac Full Load

AlphaSGT™ MOSFET

Secondary Self-synchronous Rectifier

The secondary side is a central-tapped rectifier with synchronous rectification (SR). The conduction loss caused by the on-resistance of MOSFET is much smaller than the voltage drops of diode rectification. One of the general control methods is detecting the drain-source voltage of MOSFET to control the turn-on/-off timing of the synchronous rectification. See Figure 26.

The control circuitry contains a blanking function to prevent an error trigger when the MOSFET turns on or off. Typically, the on-resistance of MOSFET is selected as small as possible to reduce the conduction loss. But the V_{DS} detection has become a challenge, especially in light load conditions. Thus, the on-resistance is recommended to be no lower than Vf_{wd}/I_{out}. In addition, the voltage of parasitic inductance and the decrease of the switching current cause V_{DS} to rise above the forward voltage drop (V_{fwd}) might trigger the switch to turn off prematurely and further increase the loss. The control circuitry will pull down the gate voltage level to increase the on-resistance of MOSFET, which eases the rise of V_{DS}. Furthermore, the lower gate voltage can reduce the driver loss and boost the turn-off speed.

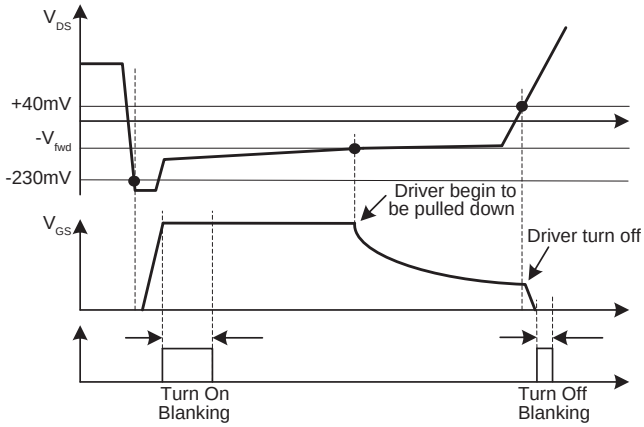

Figure 26. Turn-on/Turn-off Timing of SR (Ref. MP6924 datasheet)

Figure 27 shows the circuit diagram of the secondary side. Two MOSFETs are parallel-connected, and the performance is compared with the AONS66614 and the other two different manufacturers. Table 7 shows the parameters from the datasheet and measured results. From Table 7, the AlphaSGT$_{TM}$ has a small on-resistance. In addition, the on-resistance changes tremendously during a different gate-source voltage. The on-resistance will increase, followed by the lower gate-source voltage and the increasing drain-source current. It can be found that the AlphaSGT$_{TM}$ has the smallest on-resistance at the lowest gate-source voltage and highest drain-source current conditions, as shown in Table 7. In other words, the AONS66614 will have the smallest gate-source voltage when control circuitry pulls down the gate voltage to ease the rise of V_{DS}. Also, a lower thermal resistance than others.

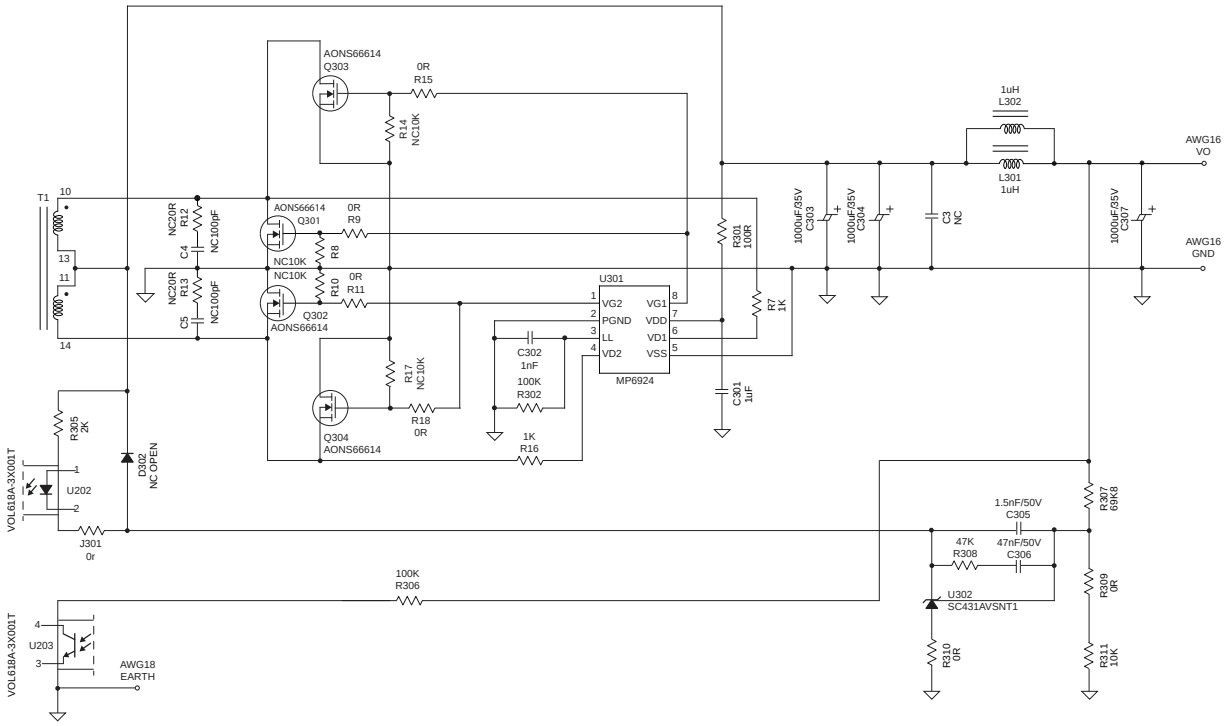

Figure 27. Circuit Schematic of Half-bridge LLC with Synchronous Rectifier on the Secondary Side

Table 7. Parameters Comparison

Parts	AONV180A60		Competitor #1		Competitor #2	
BV_{DSS} (V)	60	I_D=250μA, V_{GS}=0V	60	V_{GS}=0V, I_D=1mA	60	V_{GS}=0V, I_D=1mA
$V_{GS(th)}$ (V)	1.8	V_{DS}=V_{GS}, I_D=250μA	2.8	V_{DS}=V_{GS}, I_D=50μA	2.8	V_{DS}=V_{GS}, I_D=36μA
$R_{DS(on).max}$ (mΩ)	2.9	V_{GS}=10V, I_D=20A	2.8	V_{GS}=10V, I_D=50A	3.9	V_{GS}=10V, I_D=50A
	4.1	V_{GS}=4.5V, I_D=20A	4.2	V_{GS}=6V, I_D=12.5A	5.9	V_{GS}=6V, I_D=12.5A
C_{iss} (pF)	3310	V_{GS}=0V, V_{DS}=30V, f=1MHz	2700	V_{GS}=0V, V_{DS}=30V, f=1MHz	2000	V_{GS}=0V, V_{DS}=30V, f=1MHz
C_{oss} (pF)	745		660		490	
C_{rss} (pF)	30		28		22	
R_g (Ω)	1.1	f=1MHz	1.3	-	1.6	-
Q_{gd} (nC)	8.5	V_{DS}=30V, I_D=20A, V_{GS}=10V	7	V_{DD}=30V, I_D=50A, V_{GS}=0 to 10V	5	V_{DD}=30V, I_D=50A, V_{GS}=0 to 10V
Q_g (nC)	51		37		27	
Q_{rr} (μC)	73	I_F=20A, di/dt=500A/μs	29	V_R=30V, I_F=50A, diF/dt=100A/μs	28	V_R=30V, I_F=50A, diF/dt=100A/μs
E_{oss} (μJ) (#) V_{DS}=40V	0.81		0.66		0.51	
V_{SD}(V)	0.69	I_S=1A, V_{GS}=0V	0.88	V_{GS}=0V, I_F=50A, T_j=25°C	0.9	V_{GS}=0V, I_F=50A, T_j=25°C
R_{thJC} (°C/W)	1.3		0.9		1.1	
R_{thJA} (°C/W)	40		50		50	

Note: (#) measured results

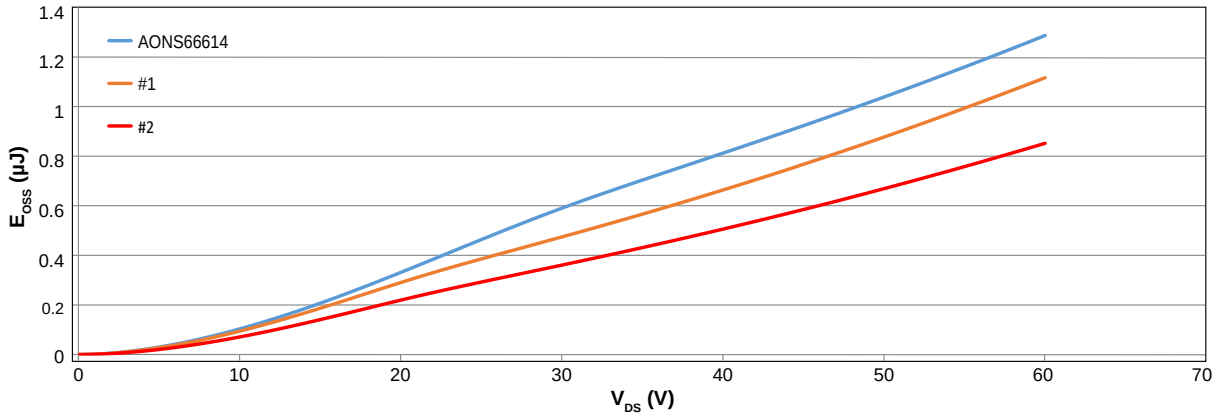

Figure 28. E_{OSS} Comparison

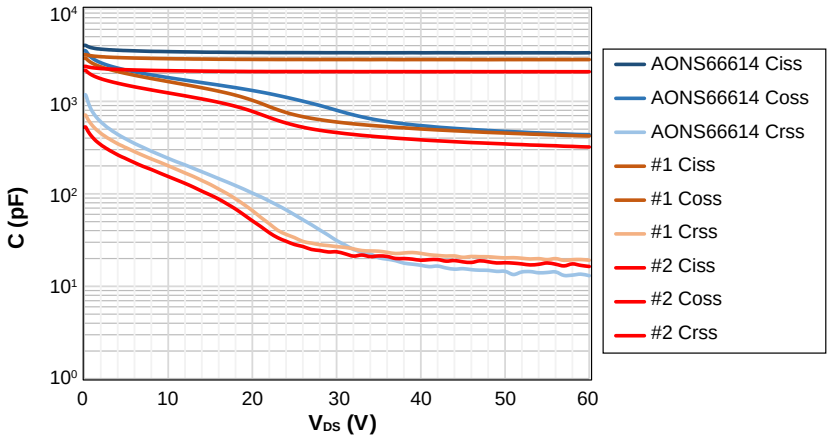

Figure 29. Capacitance Curve Comparison

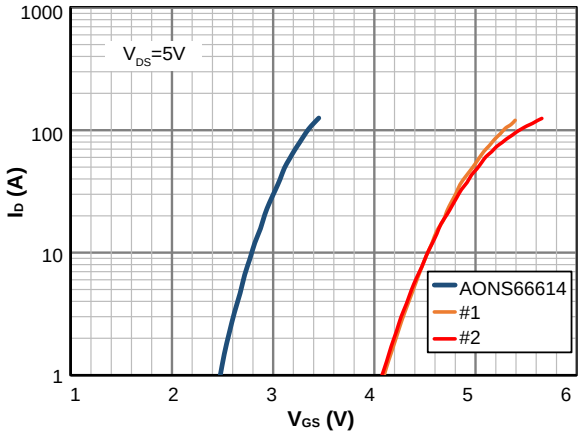

Figure 30. Transfer Characteristic

Figure 31 shows the MOSFET waveform under 230 Vac and 50% load conditions. It can be found that the AOS solution has a smaller gate-source voltage that can reduce the driver loss. Although the gate-source is regulated to a low level, the on-resistance still remains low resistance value (Table 7).

AONS66614 **#1** **#2**

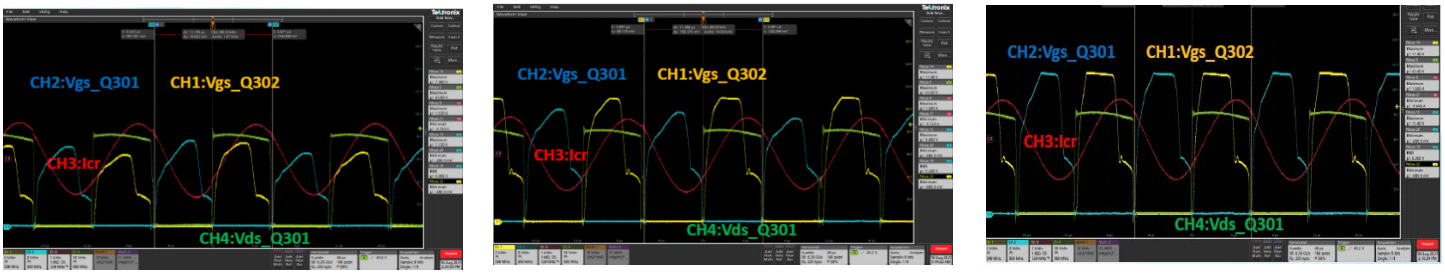

Figure 31. MOSFET Waveform at 230 Vac 50% Load

Figure 32 and Table 8 show the adapter efficiency comparison. The AOS solution has around 0.2% efficiency improvement at light load conditions. Also, the better thermal performance is shown in Figure 33.

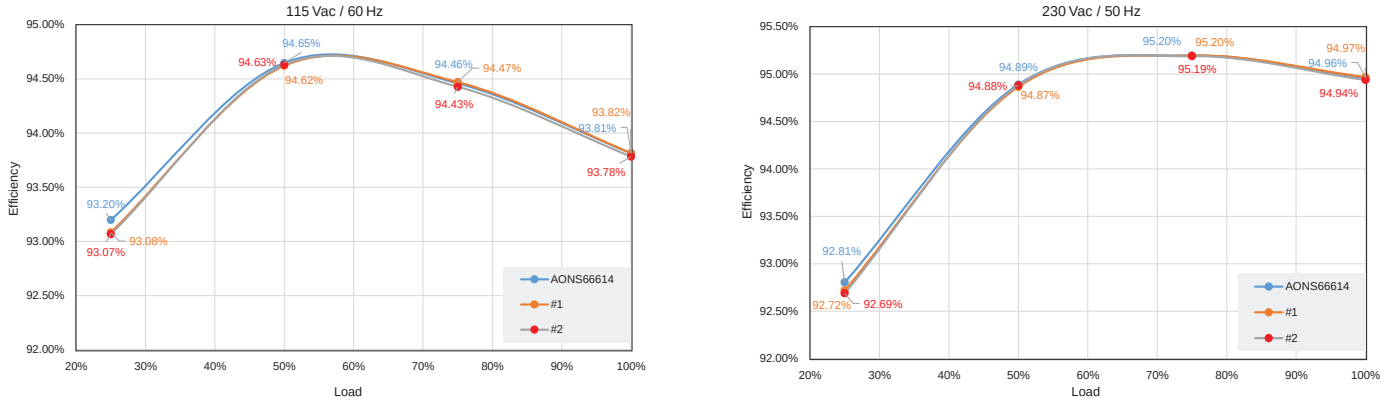

Figure 32. Adapter Efficiency Comparison by Replacing the Secondary Side Switches of LLC

Table 8. Efficiency Comparison Details

Input voltage	Parts	25% Load	50% Load	75% Load	100% Load	Avg
115 Vac/60 Hz	AONS66614	93.20%	94.65%	94.46%	93.81%	94.01%
	#1	93.08%	94.62%	94.47%	93.82%	94.00%
	#2	93.07%	94.63%	94.43%	93.78%	93.98%
230 Vac/50 Hz	AONS66614	92.81%	94.89%	95.20%	94.96%	94.46%
	#1	92.72%	94.81%	95.20%	94.97%	94.44%
	#2	92.69%	94.88%	95.19%	94.94%	94.42%

AONS66614 **#1** **#2**

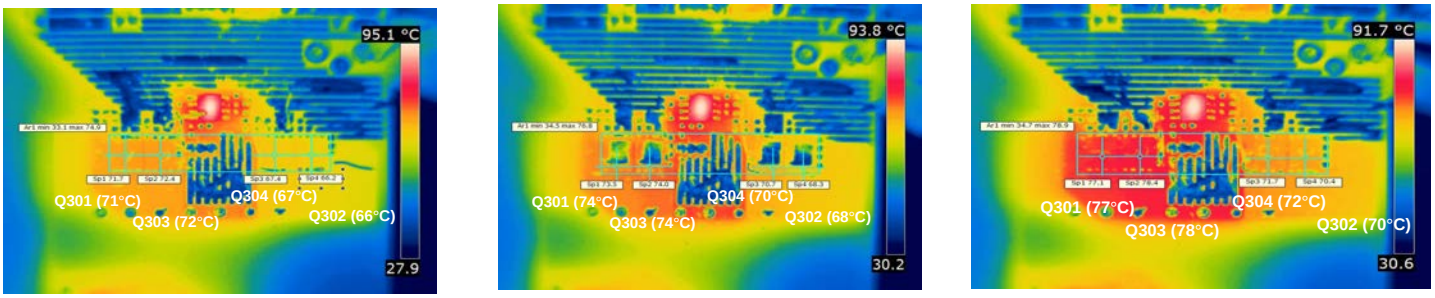

Figure 33. Thermal Performance at 230 Vac Full Load

Final Prototype

Table 9. Circuit Specification

Specification	Value	Type	Size
Input voltage	90 Vac ~ 264 Vac	Length	18.5 cm
Input frequency	50/60 Hz	Width	10 cm
Output voltage and current	20 VDC / 15A / 300 W	Height	2.5 cm
Average efficiency	94% at 115 Vac	Power density	0.649 W/cc

Finally, the prototype of the AOS solution evaluation board with universal AC input 90 Vac ~ 264 Vac and 20 VDC/15A output is demonstrated in this section. It has over 95.2% peak efficiency and 0.649 W/cc-power density with a low-cost 2-layer design. At present, a current consumer product, the Lenovo Slim 300 W AC adapter, has a 0.59 W/cc-power density, which is calculated at 20 x 10 x 2.54 cm. It could be noted that the AOS solution has the potential to provide better power density. The efficiency curves of the total supply and thermal performance of the AOS solution are shown below. (Figure 36 and Figure 37).

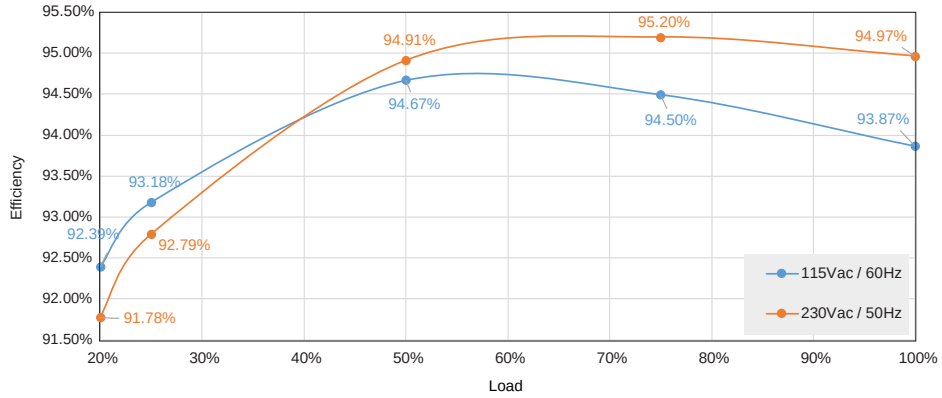

Figure 36. Efficiency of AOS Solution

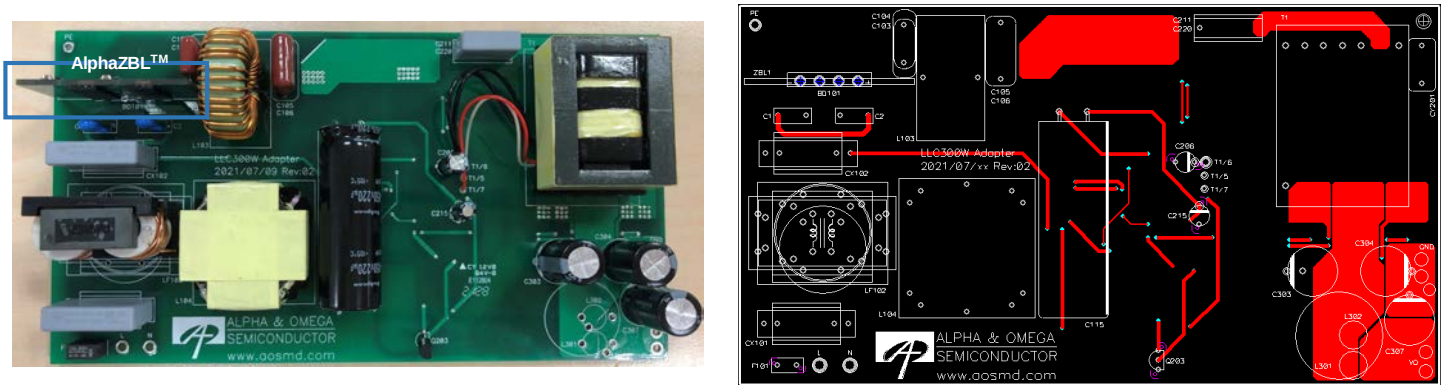

Figure 34. Evaluation Board Top View and Top Layer View

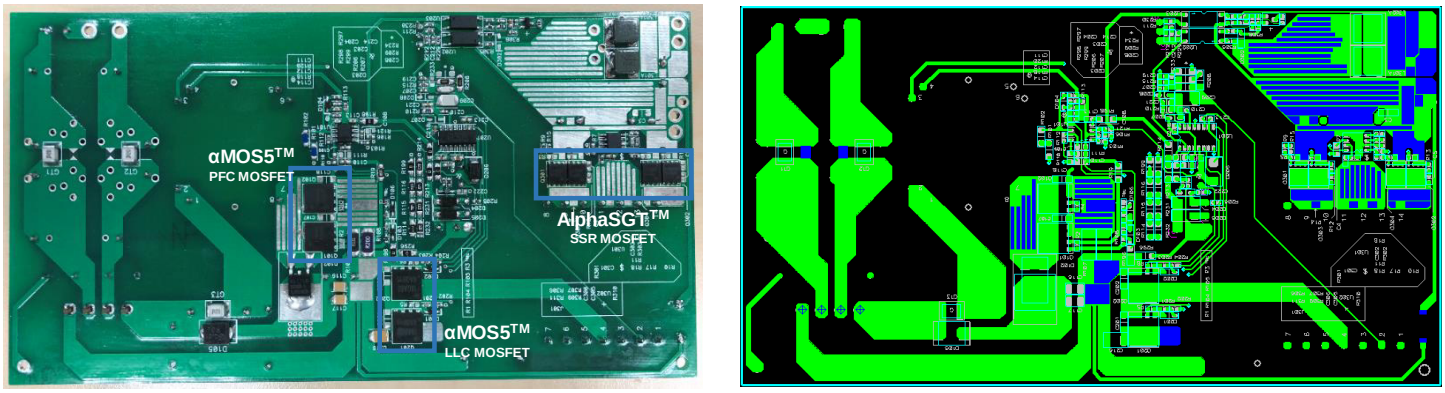

Figure 37. Evaluation Board Bottom View and Bottom Layer View

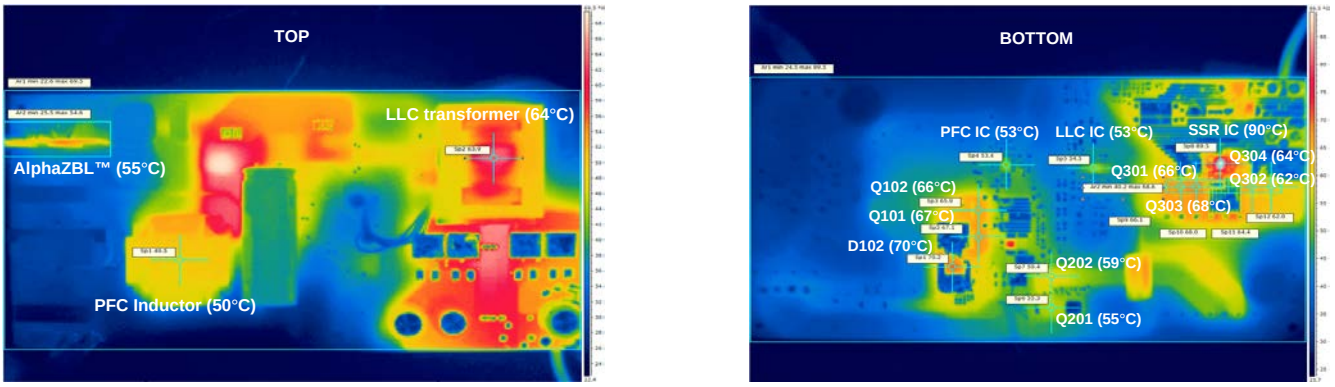

Figure 35. AOS Solution Thermal Performance at 115 Vac and Full Load

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