MOSFET Selection Guide for Telecom-Server Hot Swap Applications

Introduction

Hot swap circuits are predominately used in high-availability systems, such as servers, so that the operation will not be interrupted if there is a need to expand or repair the sub-circuits of the system, as in Figure 1 (a). The hot swapping often involves a large transient current (up to hundreds of amperes) to charge the output capacitors, which require a robust MOSFET with a large SOA capability during the linear operating mode. For discrete passive hot swap circuits, no controller is present to lower the overall cost. However, for high power and high redundancy critical telecom-server applications, usually, there is a need for hot swap controller to regulate the inrush transient current. It will not surpass the maximum allowable MOSFET limit to avoid possible system failure. After power-up, the hot swap controller will monitor the input current continuously for over-current and over-power protection. In telecom-server applications, the backplane terminal voltages dominate at 48V and 12V, and the controllers from Analog Devices are popular, as shown in Figure 1 (b). In this system, the 12V backplanes are made up of redundant power supplies connected to the parallel hot swap modules by the O-ring-FETs. MOSFET plays a key role in the hot swap applications; thus, this application note will evaluate the MOSFET behaviors among AOS and other competitors parts based on 12V ADM1278 hot swap circuits from ADI as in Figure 2.

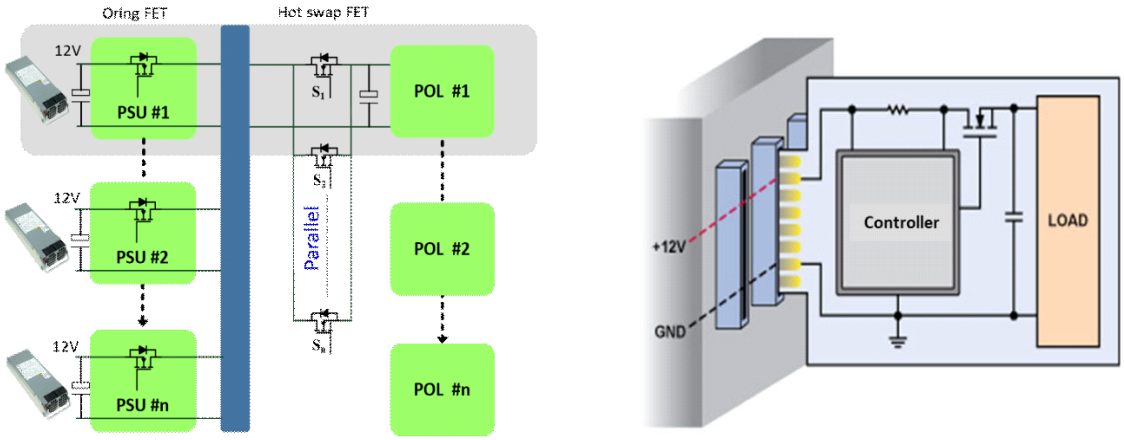


Figure 1. (a) Multi-module Telecom-server Hot Swap Applications
(b) 12V Hot Swap Active-controlled Module

Working Principle

Start-up Inrush Current

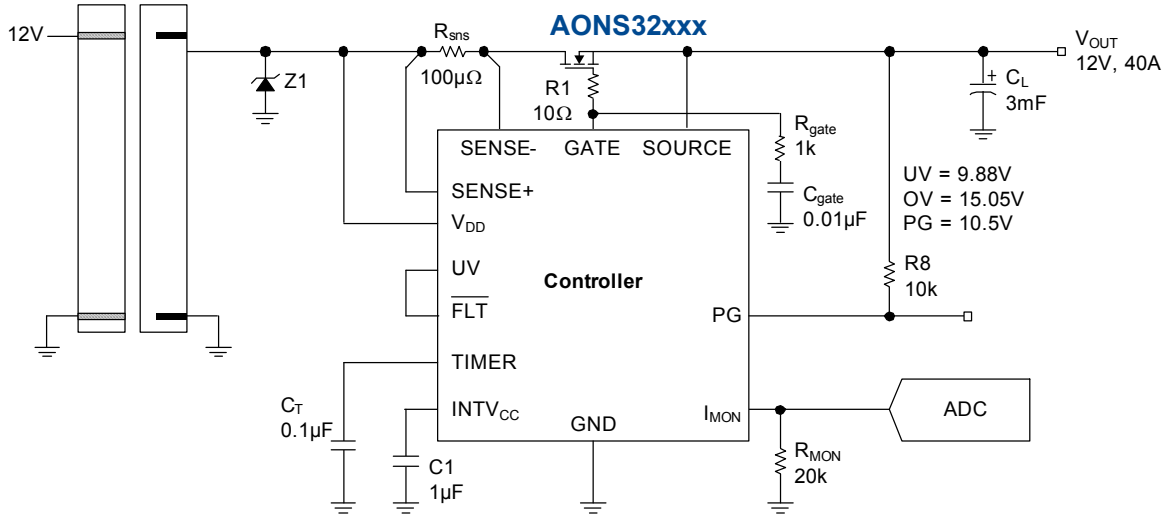


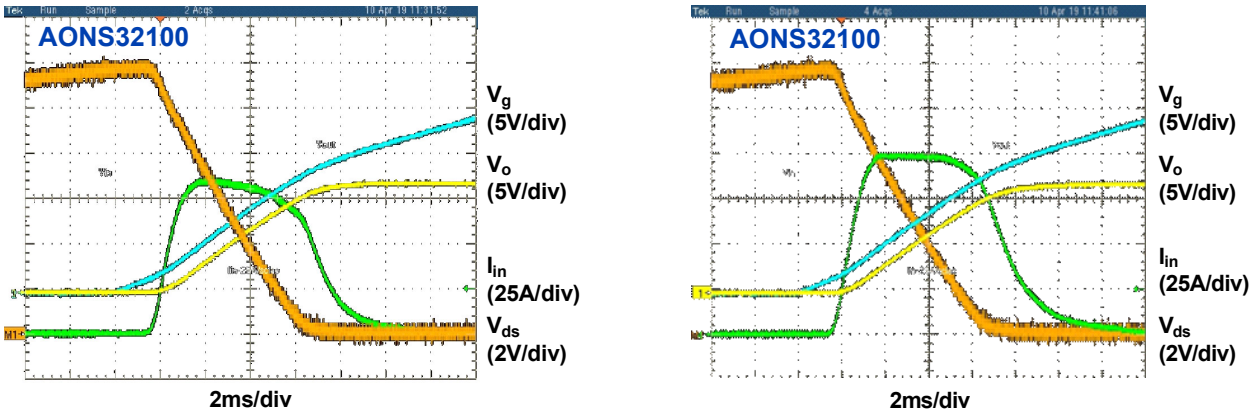
Figure 2. Hot Swap Circuit Schematic

When the hot swap module, as shown in Figure 2, is inserted into the 12V backplane, the controller GATE pin will source a constant 24uA I_g to the MOSFET gate as well as the shunt external R_{gate} and C_{gate}. After the GATE voltage reaches the MOSFET threshold VT, the I_g will only charge the external C_{gate} and MOSFET internal Crss because the voltage of Cgs across the GATE pin and the Vout node will remain constant. This is similar to the mille-plateau in the switching mode power supply. The inrush current I_{in} drawn by the output capacitor C_L can then be expressed as the equation (1,2): Where '*n*' stands for the number of MOSFET in parallel.

$$I_{in} = (I_g - nI_{gd})\frac{C_L}{C_{gate}} + I_{Load} \quad (1)$$

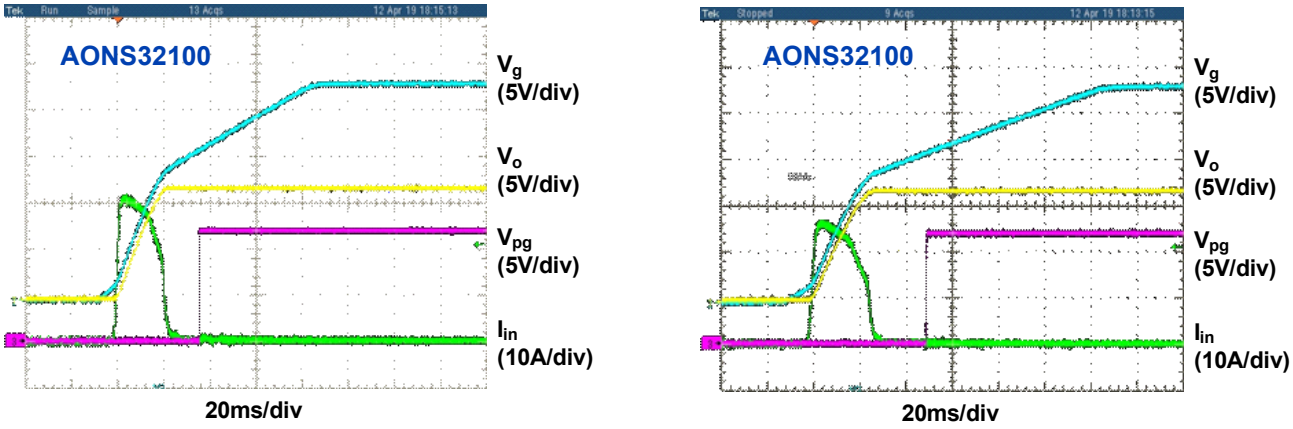
$$I_{gd} = \frac{dQ_{gd}}{dt} \quad (2)$$

Unlike in switching power supplies, where low Q_{gd} is preferred, in hot swap applications, larger Q_{gd} may benefit from lowering inrush current. On the other hand, the inrush current is also determined by the number of parallel MOSFETs, the value of the output capacitor C_L as well as the load current. The fewer parallel MOSFETs and the larger output capacitors will lead to larger inrush current stress on the MOSFET. Below are the test waveforms on AOS hot swap evaluation boards for different scenarios. Figure 3 shows that a larger C_L will draw a larger inrush current (green curve), while Figure 4 indicates that the increasing number of parallel MOSFETs will decrease the total inrush current (green curve).



(a) C_L = 50mF **(b) C_L = 65mF**

Figure 3. Comparison of Start-up Waveform with No Load and Different Output C_L

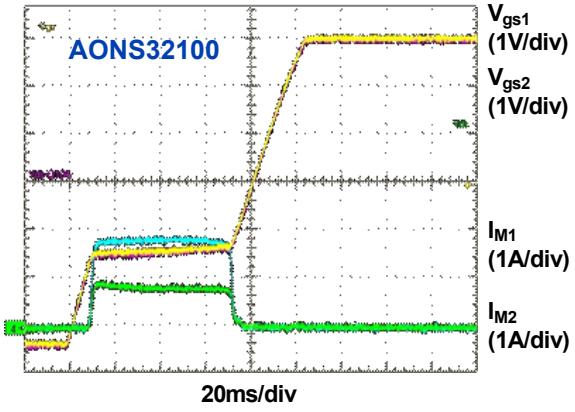


(a) n = 6 **(b) n = 10**

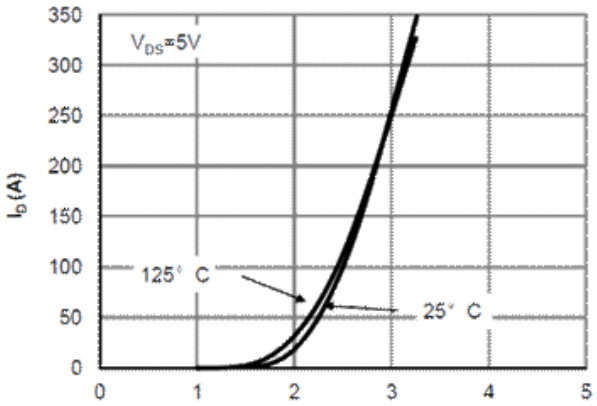
Figure 4. Comparison of Start-up Waveform with No Load, same C_L 50mF but Different Number of Parallel MOSFETs

VT Variation and Spirito-effect on Parallel Operations

There are inevitable VT variations even for MOSFETs yield from the same lot. As a result, in parallel operations, the lower VT MOSFET will conduct first, then the higher ones. In addition, the MOSFET exhibit a positive temperate coefficient on the transfer gain curve, as shown in Figure 5(b). These two physical attributes will contribute to the phenomenon shown in Figure 5(a) where the lower VT MOSFET will carry a larger current than the higher ones. Therefore, in reality, applications, the power designers should always consider the worst-case as if there is only one MOSFET in the loop.



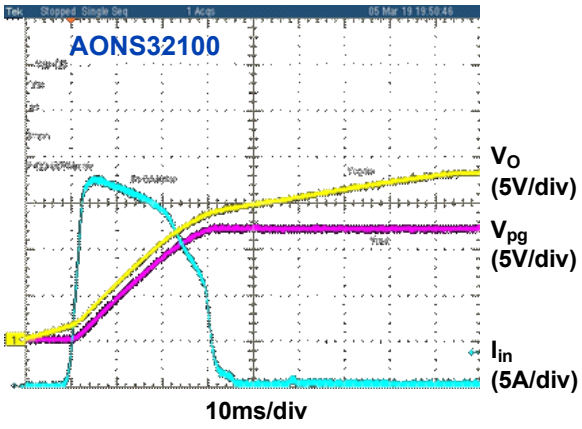
(a) Start-up Waveforms with Two Parallel MOSFETs



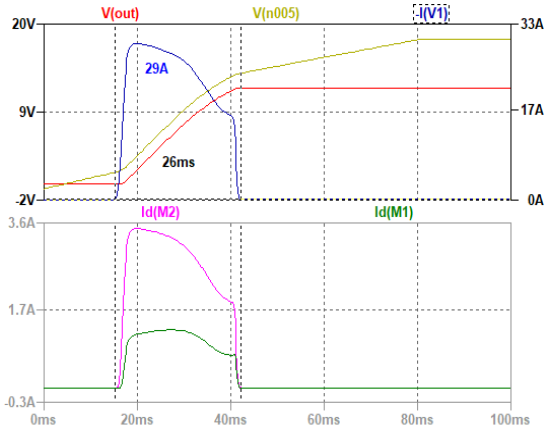
(b) Transfer Gain Curve

Figure 5. VT Variation and Spirito-effect on Parallel Operations

Simulation to Expedite the Design Process and to Save Cost



(a) Bench Start-up Waveforms



(b) Simulation Start-up Waveforms

Figure 6. Simulation and Bench Test Correlations

Simulation tools not only help to expedite the design process but save lots of trouble during the verification and debug phase. SPICE-based simulation software is a powerful switching power supply simulation tool, which includes every controller from ADI and other famous vendors. The MOSFETs from different vendors can easily be converted to the spice model and put into use. Figure 6 above shows a good correlation between the simulation and bench test of 10 parallel MOSFETs hot swap start-up waveforms. AOS generated MOS spice model behaves nearly identical performance as in the evaluation boards, where even the VT variation effect can be seen in Figure 6(b) lower chart.

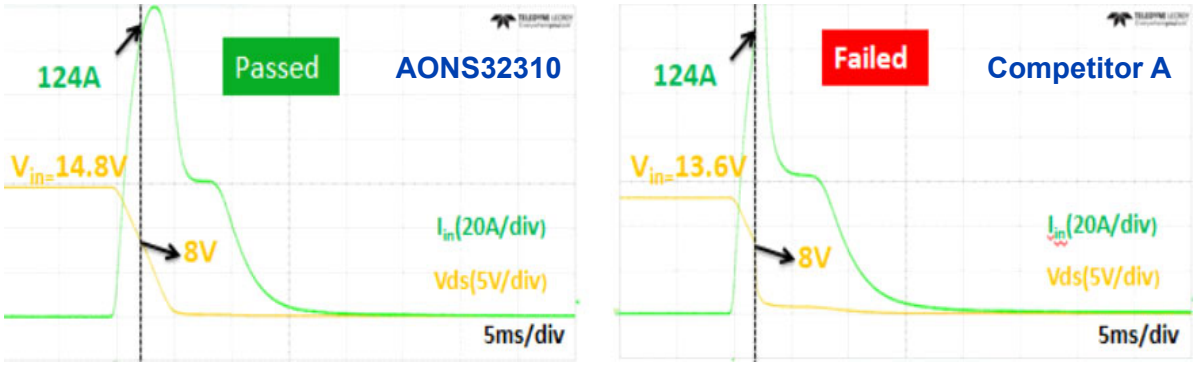
MOSFET Requirement

Telecom-server hot swap applications involve a large supply current during typical on conditions; therefore, a low Rdson MOSFET is most preferred. A large SOA is required to ensure the system's robustness during start-up and short-circuit conditions when MOSFETs are undergoing high voltage and current stress in linear operation mode. As discussed above, small VT variations and positive temperate coefficient of transfer gain are also favorable to mitigate the Spirito-effect.

AOS MOSFET Advantage over Competitors in Worst Cases

Table 1. Parameter Comparison

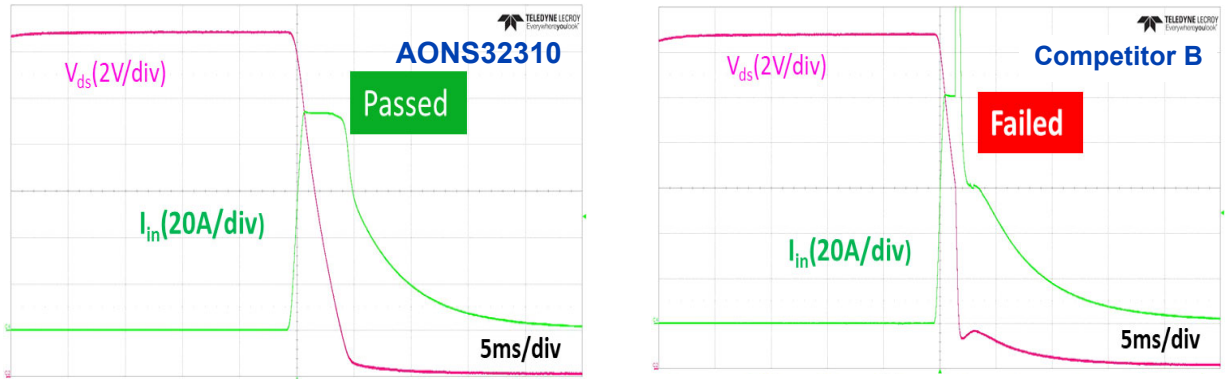
Device	V_{DS} (V)	I_D (A)	V_{TH} (V)	$R_{DS(ON)}$ (mΩ)	Ciss (pF)	Crss (pF)	Coss (pF)
AONS32310	30	390	1.8	0.8 / 1.05	15350	900	1430
Competitor A	30	298	2.2	NA / 0.9	9550	NA	NA
Competitor B	30	100	2.15	1.04 / 1.3	6227	619	1415
AONS32100	25	400	1.1	0.60 / 0.73	15200	1400	2000
Competitor C	25	300	1.7	0.57 / 0.72	8320	522	2982



(a) AONS32310 **(b) Competitor A**

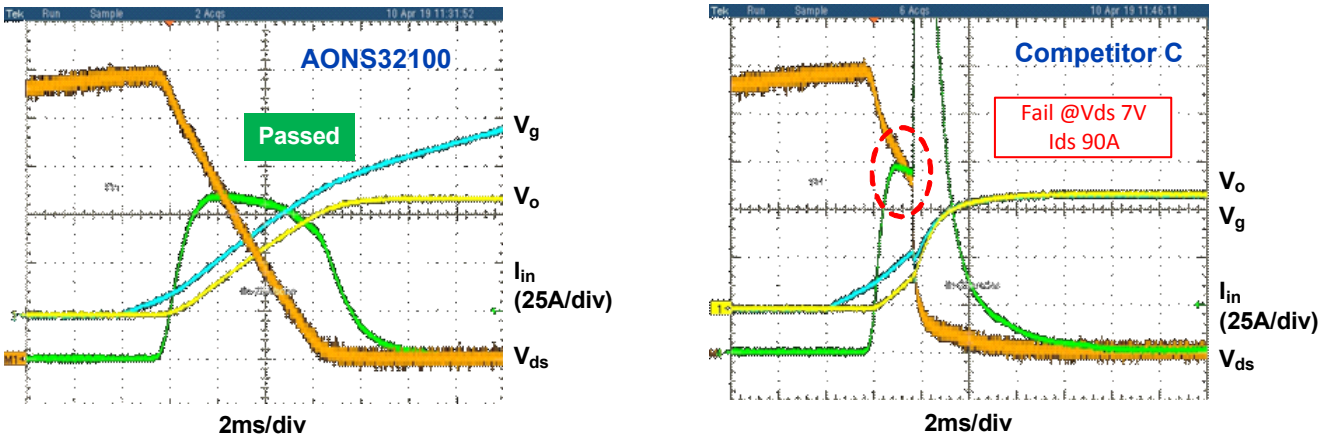
Figure 7. Comparison of Start-up Waveform with No Load, same 70mF C_L

Figure 7 shows that AONS32310 has a lower inrush current than the competitor because of relatively larger Crss. This can ease the inrush current limit settings of the system. Moreover, lower Rdson means higher efficiency when the output cap value and input voltage increases. All five AONS32310 parts sill worked well while all five of the competitor's parts failed.



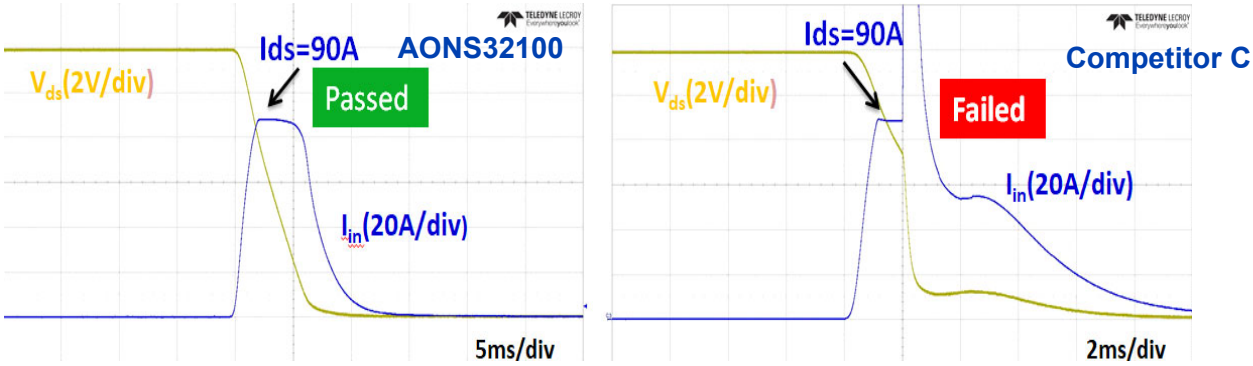
(a) AONS32310 (b) Competitor B

Figure 8. Comparison of Start-up Waveform with No Load, same 50mF C_L Inside the 100°C Chamber Environment



(a) AONS32100 (b) Competitor C

Figure 9. Comparison of Start-up Waveform with No Load, same as 50mF C_L



(a) AONS32100 (b) Competitor C

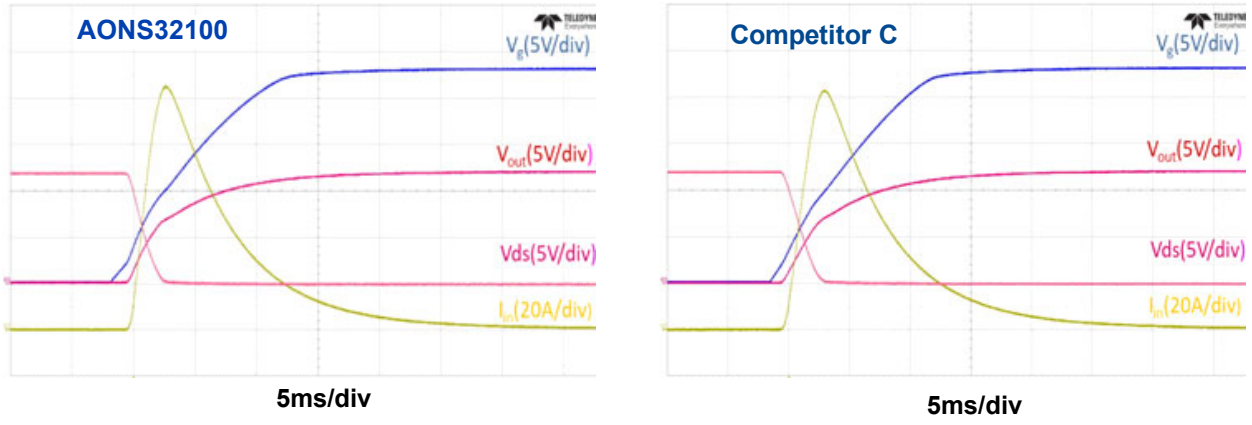
Figure 10. Comparison of Start-up Waveform with No Load, same 50mF C_L Inside the 100°C Chamber Environment

Figures 8-10 show additional worst-case start-ups using an apple to apple comparison of AOS parts with other major market competitors. In particular, Figures 8 and 10 show that AOS part still outperforms the competitors in the high-temperature environment scenarios.

These demonstrate AOS MOSFETs are in favor of hot swap applications compared to other competitors. Since the energy dissipated on the MOSFET is almost equal to the energy stored in the output C_L, AOS proposed to use the equation (3) below to demonstrate that, for example, the AONS32310 is 40% more robust than the competitor B in terms of SOA capability.

$$E_{dis} = \frac{1}{2} Vin^2 * C_L \quad (3)$$

On the other hand, if the same inrush current limit applies, the AONS32100 will exhibit almost identical start-up waveforms as the competitor C, where the system external C_{gate} and R_{gate} are removed (Figure 11). Thanks to the larger C_{iss} of AONS32100, this benefit will give cost savings to the BOM without sacrificing the system performances. Some customers have the concern that larger C_{iss} will delay the gate voltage build-up. However, in hot swap applications, as discussed before, the C_{iss} will not affect the gate voltage during the linear mode. After that, the MOSFET is already fully-on. Minor delay of gate voltage will not make a difference in the system efficiency and performance.



(a) AONS32100 without External C_{gate}

(b) Competitor C with 6.8nF C_{gate}

Figure 11. Comparison of Start-up No Load Waveform with and without External C_{gate}

Fault Conditions and Controller Protection

Even the best in class MOSFET cannot withstand the fault condition, such as output short for seconds. Therefore, the hot swap controller is required to shut down the MOSFET as soon as possible by sensing the current and voltage stress. The ADM1278 from Analog Devices is capable of both overcurrent and overpower protection. In an overpowering event, the controller will not turn off the MOSFET until the fault timer voltage hits the fault threshold 1V. The timer can be set according to the SOA of the MOSFET, which gives the designer the flexibility to choose the MOSFET that fits the system requirements and avoids the unnecessary shut down during the start-up and transient events. Figure 12 shows a series of OCP and OPP events based on the AOS evaluation board. It can be seen from the waveforms that the AONS32100 can withstand 42A/9V for more than 20ms in linear operation modes during short circuit fault in the worst-case scenario.

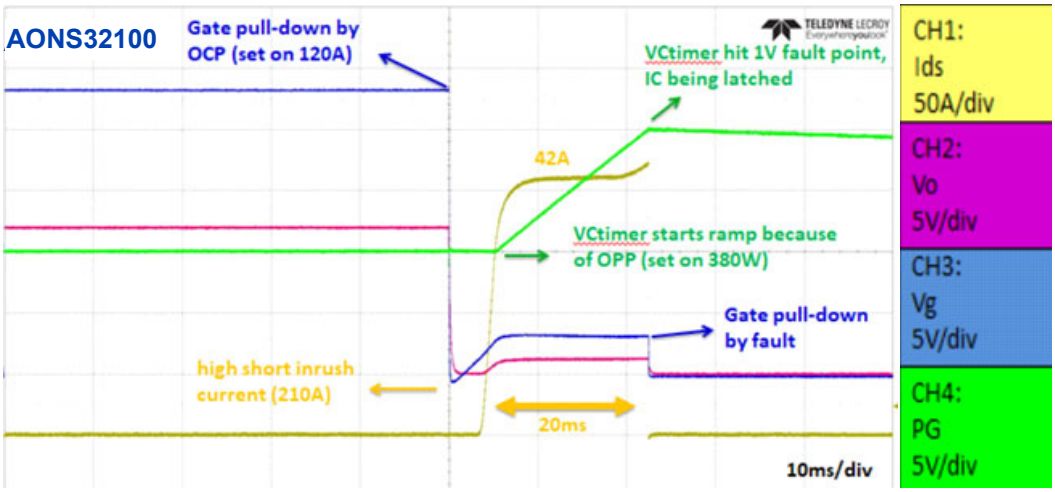


Figure 12. Short Circuit Conditions and Protections

Conclusion

This application introduces the theory and operations of the hot swap by both bench test and simulation results. Through a series of apple to apple comparisons of AOS MOSFETs with other major competitors, the conclusion can be made that the AOS MOSFETs demonstrate better robustness in terms of SOA capability. The lower R_{dson} and relatively higher Q_{gd}/C_{gd} also contribute to higher efficiency and lower the potential risk, and even a BOM save to the telecom-serer hot swap applications.

Reference

1) Wikipedia: https://en.wikipedia.org/wiki/Hot_swapping

2) 'Understanding Hot Swap: Example of Hot-Swap Circuit Design Process' - Analog Dialogue 42-05 May, (2008).

3) ADM1278 datasheet: Hot Swap Controller and Digital Power and Energy Monitor with PMBus Interface.

4) Advanced Power MOSFET Concept, B. Jayant Baliga, Springer.