

Extensive Applications of AOZ1905

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1. Introduction

AOZ1905 is a general purpose boost converter with integrated low-side NMOS. Its general application diagram is shown in Figure 1.

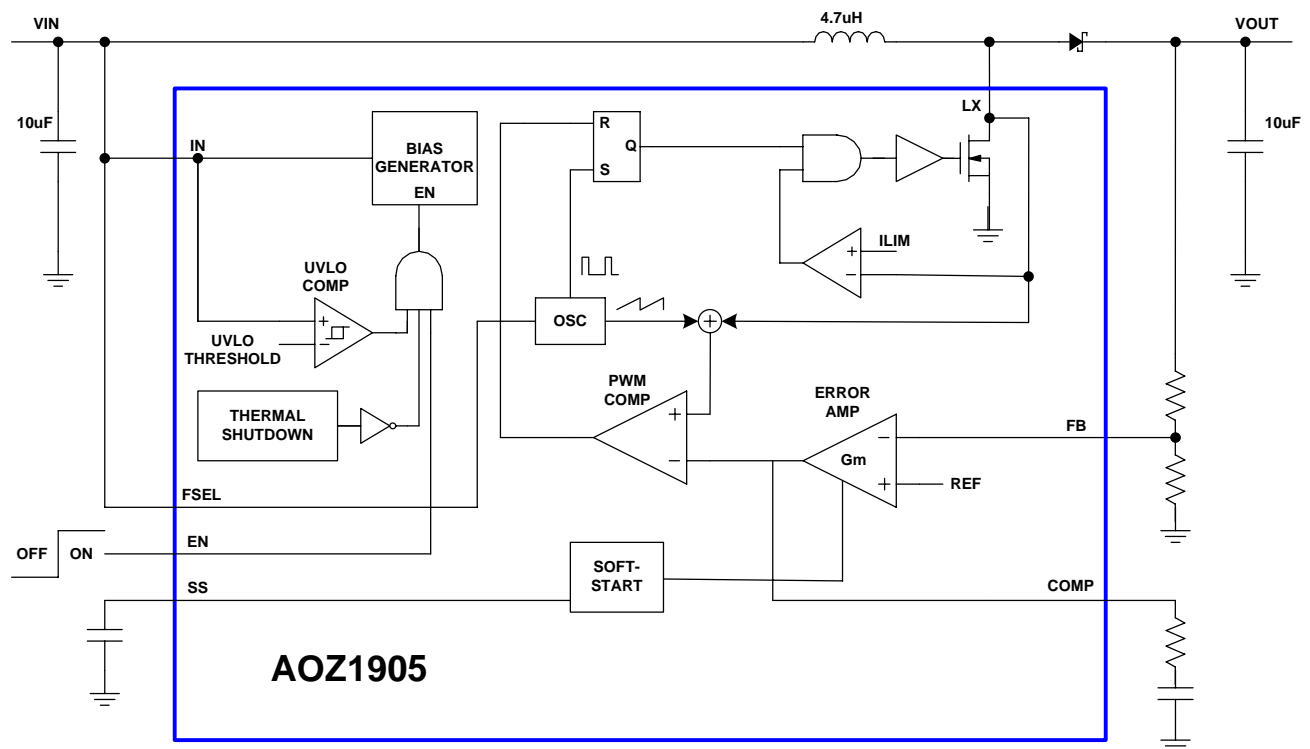


Figure 1: General application diagram

Its logic and driver circuits use low voltage silicon processes, and thus the maximum input voltage cannot exceed 6V. The power MOSFET and current sensing circuit use 30V silicon process; so the recommended maximum output voltage is 24V.

With minor external circuit modification, the AOZ1905 can be used in more applications:

- 1) Extended input voltage and output voltage such as boost $V_{in}=12V$ to $V_o=36V$
- 2) Multiple outputs including negative voltage (LCD source power solution)
- 3) Step-up or step-down input voltage using same circuit (Sepic circuit)

In this application note, the above applications are discussed.

2. Extended Input and Output Voltage (Input 12V to Output 36V)

Figure 2 shows the schematic of extended input voltage and output voltage with input voltage 12V and output voltage 36V as an example. Adding a Zener diode and current-limit resistor (Rz), the voltage seen by the IC is clamped to 5V by Zener diode, although the input voltage is 12V.

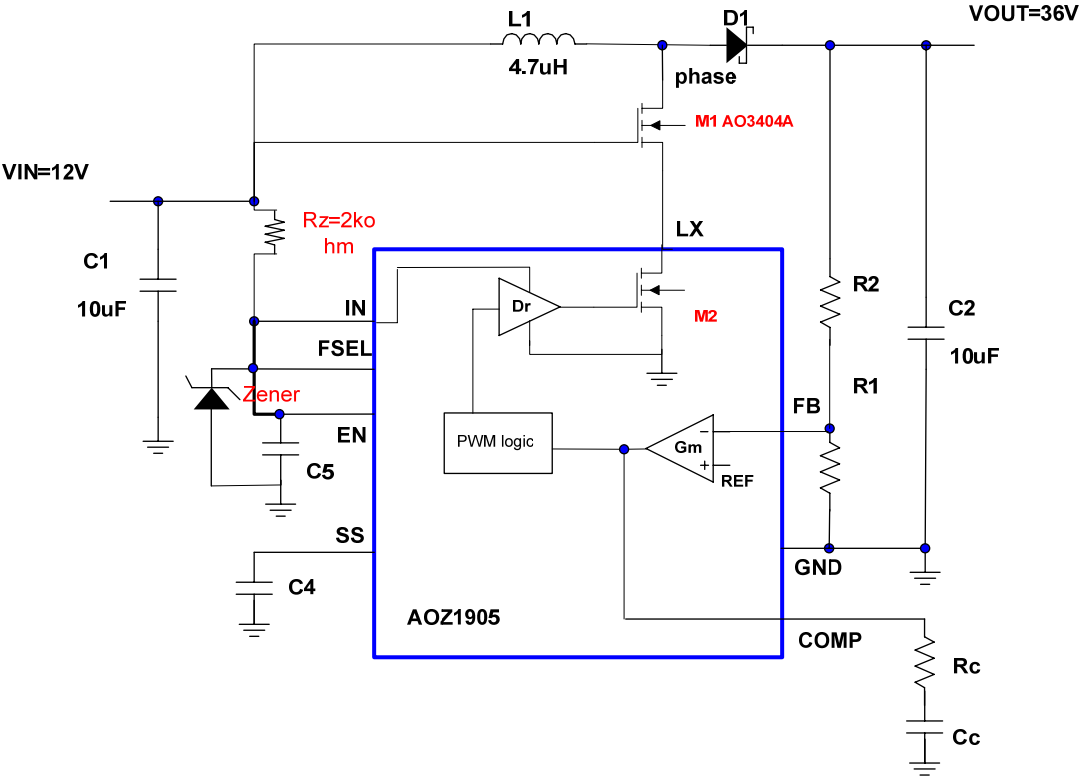


Figure 2: Schematic of extended input voltage and output voltage

A discrete NMOSFET with $V_{ds}=30V$, $V_{gs}=20V$ is connected on top of the internal integrated NMOS. AOZ1905 detects the FB: if FB higher than reference voltage, turns-off the M2; with M2 turning-off, the M1 is also turned off; at this time, V_{phase} equals to V_{out} , and the inductor voltage equal to $(V_{out}-V_{in})$. At each starting cycle, AOZ1905 turns-on the M2; with M2 turning-on, the M1 is also turned on; at this time, V_{phase} equals to zero; and the inductor voltage equals to V_{in} ; the defined D is the ratio of T_{on_M2} / T . According to inductor voltage-second balance principle: $V_{in} * D = (V_{out} - V_{in}) * (1 - D) \rightarrow V_o = V_{in} / (1 - D)$. It can be seen in Figure 3, the internal NMOS (M2) only needs to block 14V and the external NMOS (M1) only needs to block 24V; both of these voltages are within the safe operation range.

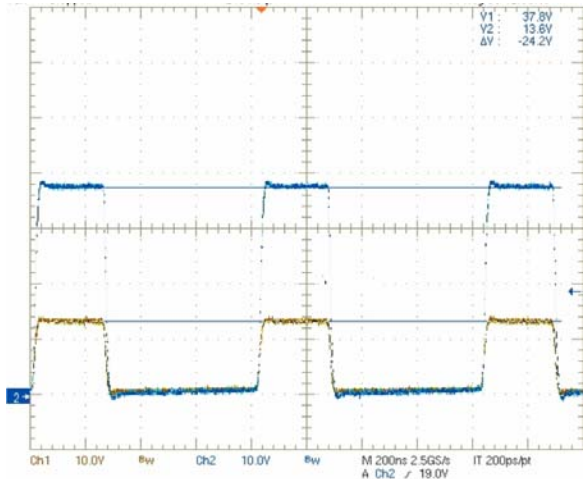


Figure 3: Waveform of LX and phase

3. Multiple Outputs including Negative Voltage (LCD Source Power Solution)

LCD panel needs several voltage rails to power source driver IC and gate driver IC. These rails include positive 26V, 9V and negative -9V. AOZ1905 with a few external components can provide the complete power solution for LCD. The schematic is shown in Figure 4. Basically, it regulates the 9V output, and uses the switching node (LX) to charge-pump the output to negative 9V and positive 26V.

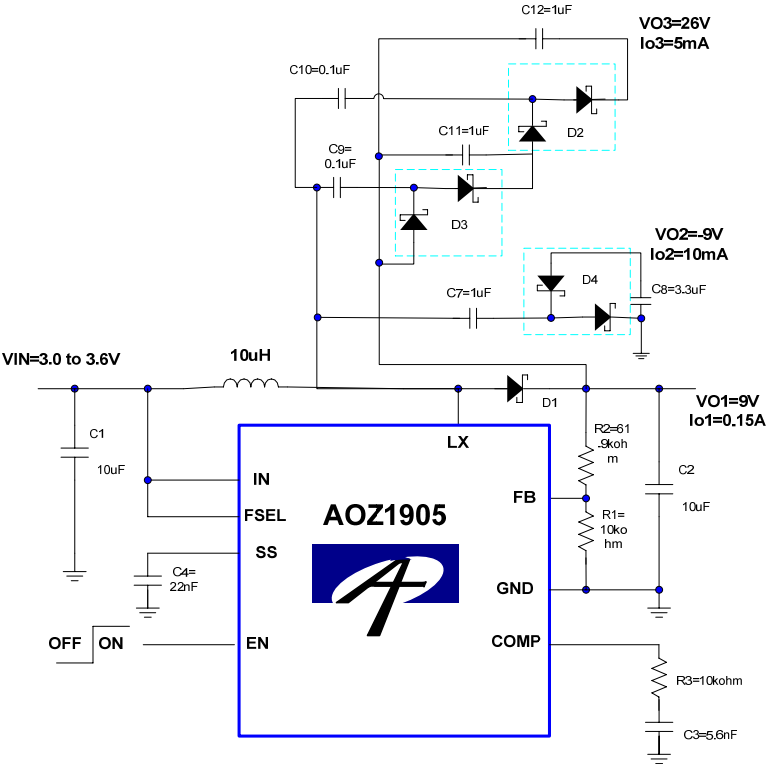


Figure 4: Multiple-output, low-profile TFT LCD power solution

4. Step-Up or Step-Down Input Voltage Using Sepsic Circuit

In many applications, the output voltage needs to be regulated constantly, despite of the variation of input voltage higher or lower than input voltage. One typical scenario is the portable power: A single-cell lithium ion battery can vary from 2.7V to 4.2V; the audio amplify needs solid 3.3V for proper operation. The AOZ1905 can be easily configured as Sepsic circuit to fulfill this function as shown in Figure 5.

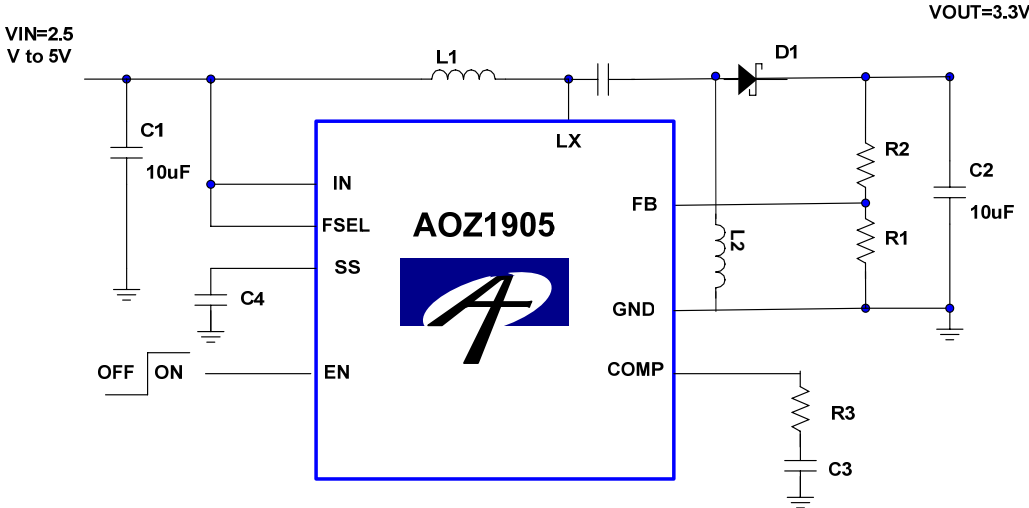


Figure 5: Sepsic circuit to step-up and step-down the voltage

The basic Sepsic circuit is shown in Figure 6. Since this Sepsic circuit is well known and the operational theory is widely published; only basic operation is explained below. During the switch off time, the current in L1 continues to flow through Cp, D1 and into Cout and the load recharging Cp ready for the next cycle. The current in L2 also flows into Cout and the load, ensuring that Cout is recharged ready for the next cycle. During this period the voltage across both L1 and L2 is equal to Vout. The voltage across Cp is equal to Vin and that the voltage on L2 is equal to Vout, in order for this to be true the voltage at the node of Cp and L1 must be Vin + Vout. The voltage across L1 is (Vin+Vout) – Vin = Vout. $D = Vout/(Vout + Vin)$.

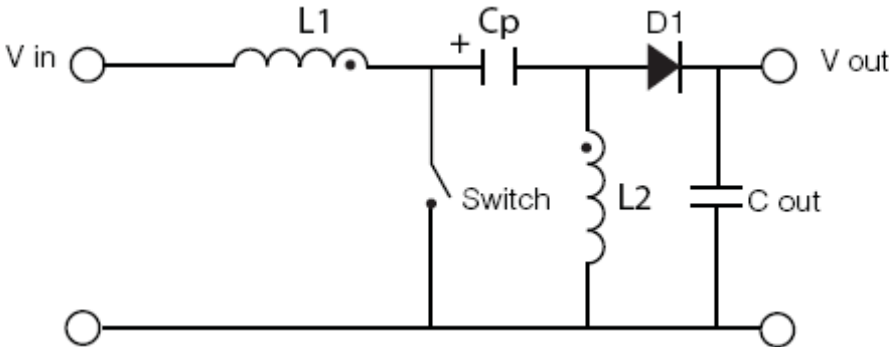


Figure 6: Basic Sepsic circuit

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