Design of Critical Conduction Mode (CRM) PFC Circuit with the AOZ7111

Introduction

This application note introduces the practical design procedure. It includes how to design the inductor, select the bulk capacitor, MOSFET, boost diode, current sense resistance, C_t capacitor, the control loop compensation network and so on. We implement a 395V, 160W, CRM PFC converter using the AOZ7111 to verify the design. The converter exhibits features such as high PF, low standby power dissipation, high efficiency, and a robust protection.

The AOZ7111 is a voltage mode active power factor correction controller designed for cost-effective boost PFC application that operates in critical conduction mode (CRM). Its voltage mode scheme does not need an AC input line-sensing network, which is usually necessary for a current mode CRM PFC controller. Also, it receives a ZCD signal pulse from the current sense resistor; therefore, ZCD auxiliary winding is not needed. The AOZ7111 is available in a SO-8 package.

It provides output over-voltage protection, over-current protection, open-feedback protection, and under-voltage lockout protection. The unique AC input fault detection circuit makes the system more robust during AC absent test. The additional OVP pin can be used to double check the output voltage if the feedback resistor gets damaged. The controller implements comprehensive safety features for robust designs.

Basic Principle of CRM PFC Converter

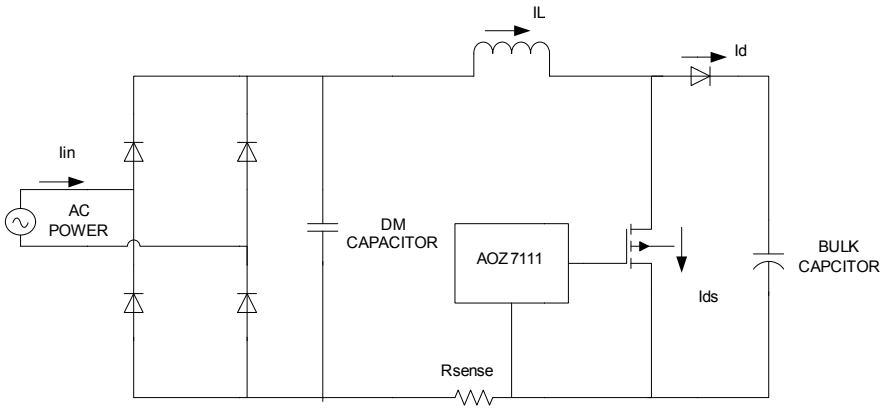


Figure 1. PFC Converter with AOZ7111

As shown in Figure 1, the PFC boost converter requires a coil, a diode and a power switch. In critical conduction mode, the inductor current I_L starts from zero up to peak current. If the turn-on time (t_{on}) is constant for a fixed time, the peak current will be proportional to the input voltage as shown in Figure 2. The averaged triangular current in each switching period is also proportional to the input voltage, thus the input current drawn from the source follows the input voltage waveform with very high accuracy.

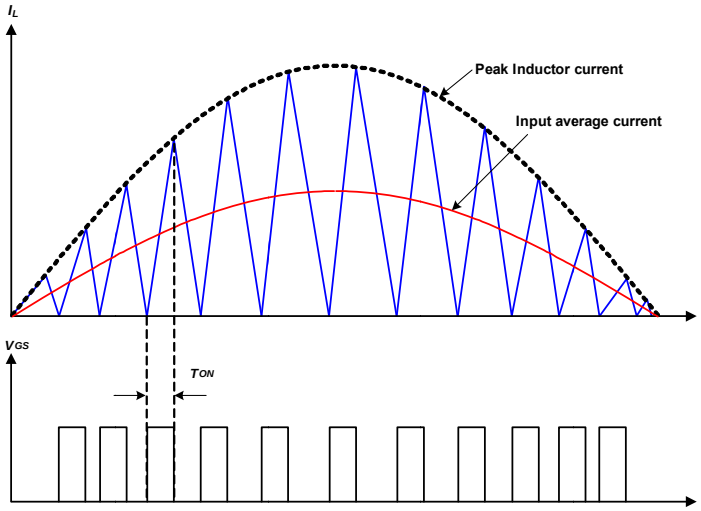


Figure 2. Waveforms of Inductor Current and Driver

Design Procedure

A 160W PFC application with universal input range is selected as a design example; it shows users the design procedure step by step.

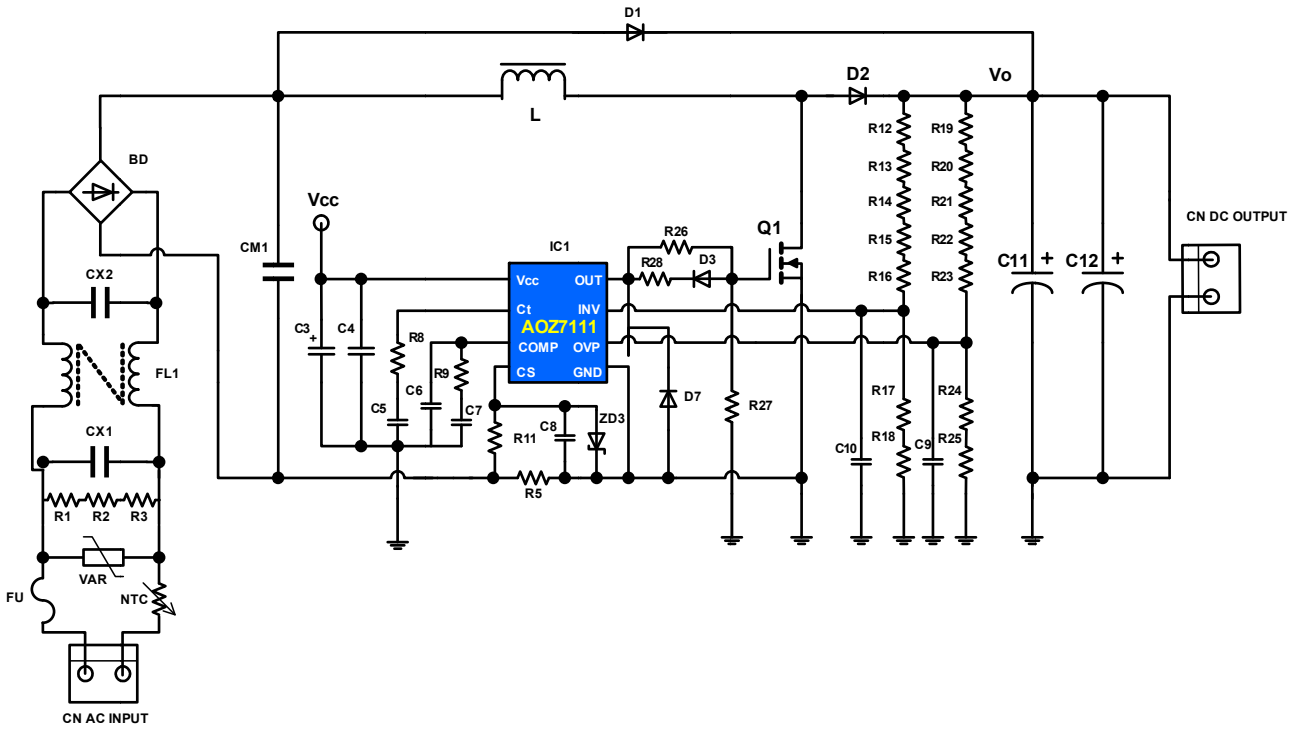


Figure 3. AOZ7111 Evaluation Board Schematic

STEP1-Define the Specification

The spec of the converter is shown in the table below.

Minimum Input Voltage	$V_{ac(min)}$ = 90V
Maximum Input Voltage	$V_{ac(max)}$ = 264V
Minimum Line Frequency	$f_{line(min)}$ = 47Hz
Maximum Line Frequency	$f_{line(max)}$ = 63Hz
Nominal Output Voltage	V_{out} = 395V
Output Ripple Voltage	$\Delta V_{out(ripple)}$ = 10V
Hold Up Time	t_{hold} = 20ms
Maximum Output Voltage	$V_{out(max)}$ = 440V
Minimum Switching Frequency	$f_{sw(min)}$ = 57kHz
Full Load Output Current	I_{out} = 0.405A
Full Load Output Power	P_{out} = 160W
Target Full Load Efficiency	η = 95%
Minimum Full Load Power Factor	PF = 0.95

STEP2-Power Stage Component Selection

1. Power Inductor Selection

The boost inductor value is determined by the output power and the minimum switching frequency. It is calculated by the equation below:

$$L = \frac{{V_{ac}}^2 \times \eta}{2 \times f_{sw(\min)} \times P_{out}} \times \left(1 - \frac{\sqrt[2]{2} \times V_{ac}}{V_{out}}\right) \qquad \text{(eq-1)}$$

Where L is the boost inductance.

The minimum frequency occurs at maximum input voltage ($V_{ac(max)}$ = *264V*) and full load condition as shown in Figure 4. According to eq-1, the inductor value is calculated as:

$$L = \frac{264^2 \times 0.95}{2 \times 60 \times 10^3 \times 160} \times \left(1 - \frac{\sqrt[2]{2} \times 264}{395}\right) = 189\,\mu H$$

We select the value as 200μH.

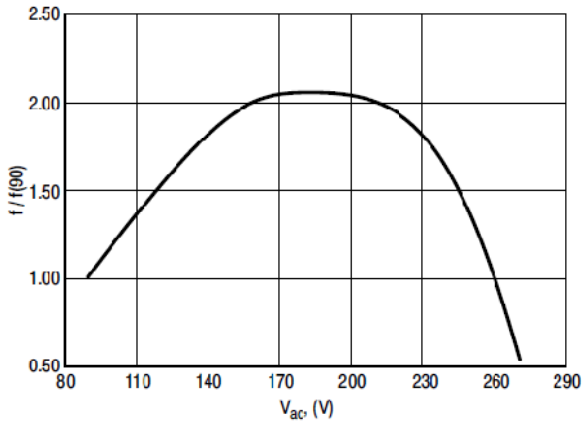


Figure 4. Switch Frequency vs. Input RMS Voltage (at sinusoid top)

At minimum input voltage and maximum output power, the inductor peak current reaches the maximum, which causes the greatest stress to the power components. The inductor peak current is calculated by:

$$I_{Lpk} = \frac{2 \times \sqrt[2]{2 \times P_{out}}}{V_{ac} \times \eta} = \frac{2 \times \sqrt[2]{2 \times 160}}{90 \times 0.95} = 5.29A \qquad \text{(eq-2)}$$

Assuming EER3019NA core is selected and setting B (max) as 0.23T, the primary winding should be:

$$N_{inductror} = \frac{I_{Lpk} \times L}{A_e \times B(\max)} = \frac{5.29 \times 200\mu H}{130.7mm^2 \times 0.21} = 39T_s \qquad \text{(eq-3)}$$

The number of turns of the boost inductor is determined as 39. Figure 5 shows the appearance of ER3019N core and bobbin (A_e = *130.7mm*^{2}, A_w = *81.8mm*^{2}). According to the typical B-H characteristics of ferrite core from SAMWHA (PL-7), the saturation flux density decreases as the temperature increases, so the high temperature characteristics should be considered (saturation flux *B (max) = 0.41mT @ 100deg*).

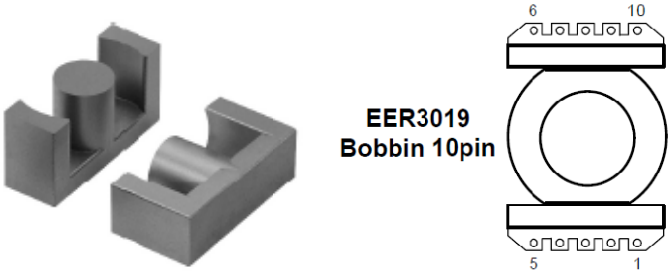


Figure 5. EER3019N Ferrite Specifications

When Φ0.10mm × 50 (litz wire) is used, the RMS current of inductor coil, current density and the window coefficient are:

$$I_{Lrms} = \frac{2 \times P_{out}}{\sqrt[2]{3 \times \eta \times V_{ac(\min)}}} = \frac{2 \times 160}{\sqrt[2]{3 \times 0.95 \times 90}} = 2.16A \qquad \text{(eq-4)}$$

$$I_{Ldensity} = \frac{2.16}{\pi \times \left(0.1/2\right)^2 \times 50} = 5.53\,A/mm^2 \qquad \text{(eq-5)}$$

$$A_{co} = \frac{\pi \times \left(0.1/2\right)^2 \times 50 \times N_p + \pi \times \left(0.3/2\right)^2 \times N_{aux}}{A_w} = \frac{15.31 + 0.35}{81.8} = 0.19$$

Figure 6 shows the winding of the inductor:

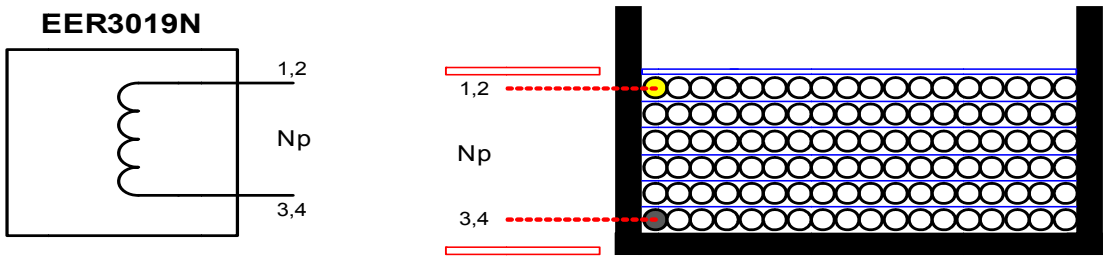


Figure 6. Winding the Inductor

Winding specification

	Pin	Diameter	Turns
Np	3,4 → 1,2	Φ0.10mm × 50 (litz wire)	39
Insulation tape		0.05mm	3

Test condition:

	Pin	Spec.	Test condition
Inductance	3,4 → 1,2	200μH (5%)	100KHz,1V

2. Bulk Capacitor Selection

According to the ripple specification of $10V_{p\text{-}p}$, the capacitor should be:

$$C_{bulk} = \frac{I_{out}}{2 \times \pi \times f_{line(\min)} \times \Delta V_{out(ripple)}} = \frac{0.405}{2 \times 3.14 \times 50 \times 10} = 129\mu F \qquad \text{(eq-6)}$$

According to the minimum allowable output voltage 315V ($0.8 \times V_{out}$) during one cycle line (20ms) drop-out, the capacitor should be:

$$C_{bulk} = \frac{P_{out} \times t_{hold}}{\frac{1}{2} \times V_{out}^2 - \frac{1}{2} \times V_{out(\min)}^2} = \frac{160 \times 20m}{\frac{1}{2} \times 395^2 - \frac{1}{2} \times 315^2} = 113\mu F \qquad \text{(eq-7)}$$

The output capacitor must be larger than 129μF, so the two electrical capacitor (68μ/450V) parallel are selected.

3. MOSFET and Output Diode Selection

To begin, we need to know the voltage stress of the MOSFET:

$$V_{ds(\max)} = V_{out(\max)} + V_{d(\max)} = 440 + 1.26 = 441.26V \qquad \text{(eq-8)}$$

Where $V_{ds(max)}$ is the maximum voltage stress of MOSFET.

The $V_{d(max)}$ is the maximum forward voltage drop of output diode. We can select AOS's AOTF11C60 MOSFET, its maximum $R_{ds(on)}$ is 0.4Ω, maximum C_{oss} (energy related) is 90pF at drain-source voltage is 480V, C_{ext} is zero. The output diode BYV29X is selected, $V_{f(max)}$ is 1.26V at 25°C, 8A.

The MOSFET and Output Diode RMS current are calculated as:

$$I_{ds(rms)} = I_{L(rms)} \times \sqrt{1 - \left(\frac{8 \times \sqrt[2]{2 \times V_{ac(\min)}}}{3 \times \pi \times V_{out}} \right)} = 2.16 \times \sqrt{1 - \left(\frac{8 \times \sqrt[2]{2 \times 90}}{3 \times \pi \times 395} \right)} = 1.84A \qquad \text{(eq-9)}$$

$$I_{d(ave)} = \frac{I_{out}}{\eta} = \frac{0.405}{0.95} = 0.426A \qquad \text{(eq-10)}$$

The MOSFET loss can be divided into three parts: conduction loss, turn-off loss, and turn-on loss.

Conduction loss can be obtained as:

$$P_{ds(con)} = I_{ds(rms)}^2 \times R_{ds(on)} = 1.84^2 \times 0.4 = 1.35W \qquad \text{(eq-11)}$$

Turn-off loss can be calculated as:

$$P_{ds(off)} = \frac{1}{2} \times V_{out} \times I_{in(rms)} \times t_{off} \times f_{sw(\min)} = \frac{1}{2} \times 395 \times 1.87 \times 50ns \times 57k = 1.05W \qquad \text{(eq-12)}$$

Where $I_{in(rms)}$ is the input RMS current, t_{off} is the turn-off time and $f_{sw(min)}$ is the minimum switch frequency.

Turn-on loss can be calculated as:

$$P_{ds(on)} = \frac{1}{2} \times (C_{oss} + C_{ext}) \times V_{out}^2 \times f_{sw(\min)} = \frac{1}{2} \times (90p) \times 395^2 \times 70 \times 1000 = 0.49W \qquad \text{(eq-13)}$$

C_{oss} is the output capacitance of the MOSFET. C_{ext} is an externally added capacitor at drain and source of MOSFET. The total loss of MOSFET is:

$$P_{ds(total)} = P_{ds(con)} + P_{ds(off)} + P_{ds(on)} = 2.89W \qquad \text{(eq-14)}$$

The power loss of the output diode is calculated as:

$$P_{d(loss)} = I_{d(ave)} \times V_{f(\max)} = 0.426 \times 1.26 = 0.54W \qquad \text{(eq-15)}$$

4. Current-Sense Resistor Selection and CS Circuit Design

The first role of R_{cs} is to set shut down mode over current protection level. According to the eq-2, the maximum inductor current is $I_{Lpk,}$ and sensing resistor is calculated as:

$$R_{cs} = \frac{V_{ocp1}}{I_{Lpk}} = \frac{0.7}{5.29} = 0.132\Omega \qquad \text{(eq-16)}$$

Choosing 0.1Ω as R_{cs}, power loss is calculated as:

$$P_{r(loss)} = I_{L(rms)}^2 \times R_{cs} = 2.16^2 \times 0.1W = 0.47W \qquad \text{(eq-17)}$$

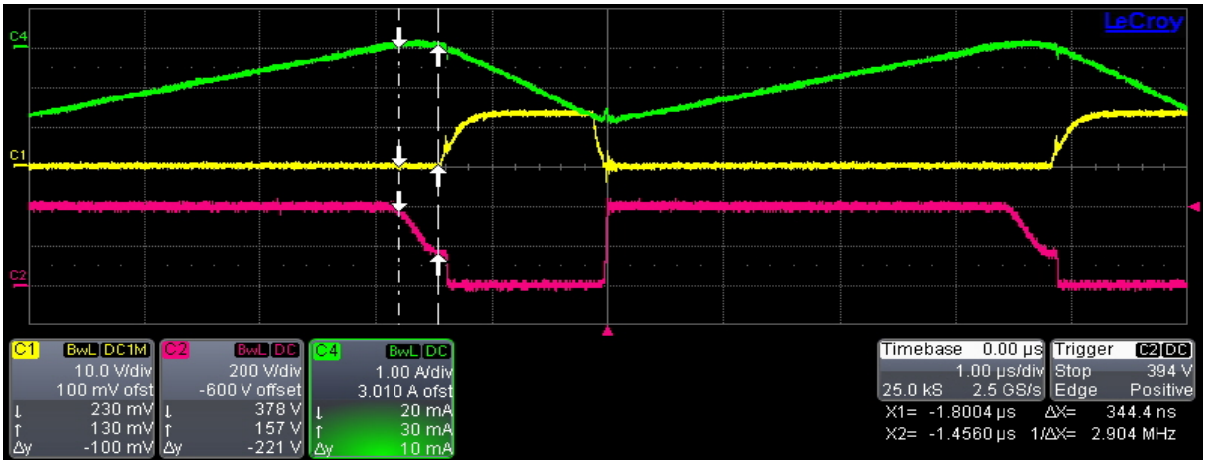
Recommended power rating of sensing resistor is 2W.

STEP3-The CS pin delay time constant selection

The second role of R_{cs} is detecting the zero current point of the boost inductor. The negative signal V_{cs} is applied to the current sense pin. When V_{cs} is higher than the threshold (-15mV), it means the inductor current is nearly zero. In order to minimize the constant turn-on time deterioration and turn-on loss, we should trigger the gate at the drain source voltage's valley point, which may need additional delay by the external resistor and capacitor. The required delay time is one-half of the resonant period; approximately:

$$R_{zcd} \times C_{zcd} + 650ns = \frac{2\pi \times \sqrt[2]{C_{eff} \times L}}{2} \qquad \text{(eq-18)}$$

Where C_{eff} is the effective capacitor shown at the MOSFET drain to source; C_{zcd} and R_{zcd} are the external capacitance and resistor at CS pin; "650ns" is the IC internal set delay time.



CH1: Driver Voltage – CH2: V_{ds} (MOSFET's Drain and Dource Voltage) – CH3: Inductor Current

Figure 7. Realistic CRM Waveforms with R_{zcd} and C_{zcd} @230V/Full Load

The time between both dotted lines is the delay time. We can select the appropriated R_{zcd} and C_{zcd} to achieve minimum drain voltage turn-on. These values are found experimentally.

STEP4-The C_t capacitor selection

When the PFC operates in critical conduction mode, a boost converter presents two phases. During the power switch conduction time, the current ramps-up from zero to the envelope level. At that moment, the power switch turns off and the current ramps-down to zero. The maximum on-time of the controller occurs when V_{comp} is at the maximum. The C_t capacitor is sized to ensure that the required on-time is reached at maximum output power and the minimum input voltage condition:

$$t_{on} = \frac{L \times I_{Lpk(\omega t)}}{\sqrt[2]{2}V_{ac} \times s_{in(\omega t)}} = \frac{L \times 2 \times \sqrt[2]{2} I_{in} \times s_{in(\omega t)}}{\sqrt[2]{2}V_{ac} \times s_{in(\omega t)}} = \frac{2 \times L \times I_{in}}{V_{ac}} = 2 \times L \times \frac{P_{out}}{\eta \times {V_{ac}}^2} \qquad \text{(eq-19)}$$

In regards to the AOZ7111; the on time was controlled with the capacitor connected to the Ct pin. A current source charges the C_t capacitor to a voltage ($V_{ct(off)}$) derived from COMP pin voltage.

$$t_{on} = \frac{C_t \times V_{ct(off)}}{I_{charger}} \qquad \text{(eq-20)}$$

$$V_{ct(off)} = V_{comp} - V_{ct(offset)} = \frac{2 \times P_{out} \times L \times I_{charger}}{\eta \times V_{ac}{}^2 \times C_t} \quad \text{(eq-21)}$$

From the datasheet of AOZ7111, we have: $V_{ct(max)}$ = *8V (typical);* $V_{ct(offset)}$ = *1V (typical),* $I_{charger}$ = *250μA (maximum)*, then:

$$C_{t(\min)} = \frac{2 \times P_{out} \times L \times I_{charger}}{\eta \times V_{ac}{}^2 \times (V_{comp} - V_{ct(offset)})} = \frac{2 \times 160 \times 200\mu \times 250\mu}{0.95 \times 90^2 \times 8V} = 260pF \quad \text{(eq-22)}$$

A value of 470p/50V provides sufficient margin.

STEP5-FB, OVP, and UVP Divider Resistors Selection

R_{fb1} and R_{fb2} form a resistor divider that scales down V_{out} before it is applied to the INV pin. The error amplifier adjusts the on-time of the drive to maintain the FB pin voltage equal to the error amplifier reference voltage (V_{ref}). The divider network bias current (I_{bias}) selection is the first step in the calculation. The divider network bias current is selected to optimize the trade-off of noise immunity and power dissipation. R_{fb1} is calculated as:

$$R_{fb1} = \frac{V_{out}}{I_{bias}} = \frac{395V}{80\mu A} = 4.9M\Omega \quad \text{(eq-23)}$$

A bias current of 80μA provides an acceptable trade-off of power dissipation to noise immunity. A series of five resistors of 1MΩ/0805 are selected.

$$R_{fb2} = \frac{V_{ref} \times R_{fb1}}{V_{out} - V_{ref}} = \frac{2.5V \times 5M}{395 - 2.5V} = 31.85k\Omega \quad \text{(eq-24)}$$

R_{fb2} is selected by a resistor of 30K/0805 and a resistor of 1.8K/0805 which are in series.

$$V_{out} = \frac{R_{fb1} + R_{fb2}}{R_{fb2}} \times V_{ref} = \frac{5M + 31.8k}{31.8k} \times 2.5 = 395.6V \quad \text{(eq-25)}$$

The AOZ7111 includes two integrated OVP circuits to prevent the output from exceeding a safe voltage. The first OVP circuit compares FB to the internal comparator's reference (V_{ref1} = *2.685V*) to determine if an OVP fault occurs.

$$V_{ovp1} = \frac{R_{out1} + R_{out2}}{R_{out2}} \times V_{ref1} = \frac{5M + 31.8k}{31.8k} \times 2.685 = 425V \quad \text{(eq-26)}$$

The second OVP circuit compares the external new resistor divider (R_{out3} and R_{out4}) applied to pin 4's reference (V_{ref2} = *2.75V*) to double check the output voltage. R_{ovp1} is the same as the R_{fb1}. The R_{ovp2} is reselected as 24.9k/0805 and 5.9k/0805 which are in series.

$$V_{ovp2} = \frac{R_{out3} + R_{out4}}{R_{out4}} \times V_{ref2} = \frac{5M + 30.8k}{30.8k} \times 2.75 = 449V \quad \text{(eq-27)}$$

STEP6-Compensation Network Selection

After designing the power components, we will help the user design the control loop compensation network. To find a compensation network, it is necessary to get the control loop model of this converter. This can be synthesized as shown in Figure 8.

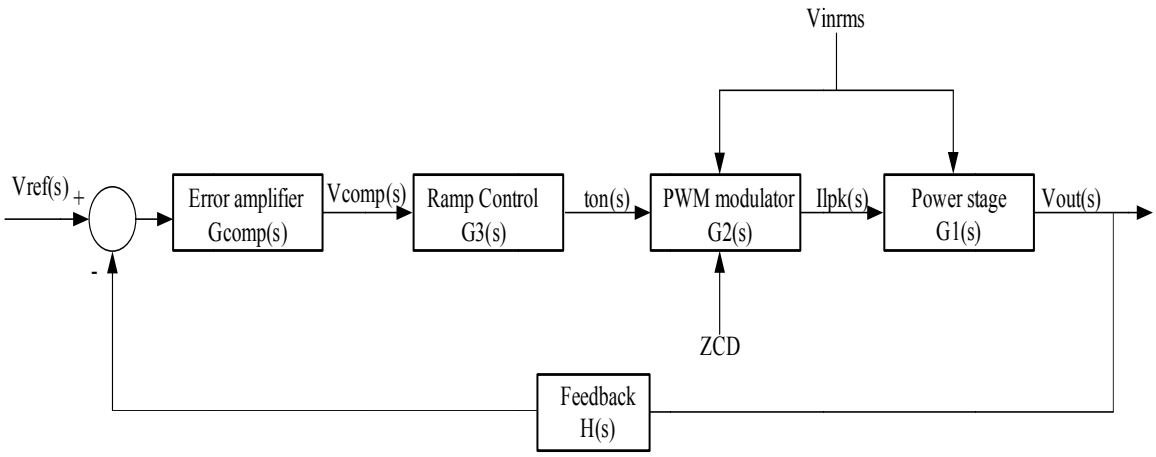


Figure 8. Control Loop of PFC

1. Power Stage

We assume that the control action takes place on the peak amplitude of various quantities inside the loop.

The first step is to determine the transfer function of power stage, defined as:

$$G_{1(s)} = \frac{dV_{out}}{dI_{Lpk}} = \frac{dV_{out}}{dI_{out}} \times \frac{dI_{out}}{dI_{Lpk}} \qquad \text{(eq-28)}$$

Where V_{out} is the DC output voltage, I_{Lpk} is the peak value of inductor current, I_{out} is DC output current.

The power stage can be modeled: a control current source (with shunt resistance R_e) that drives the output bulk capacitor C_o and the load resistance R_L *(= V_{out}/I_{out})*. The zero due to ESR associated with C_o is far from crossover frequency thus it is neglected.

The current source can be characterized with the following consideration: the low frequency component of the boost diode current is found by averaging the discharge portion of inductor current over a given switch cycle.

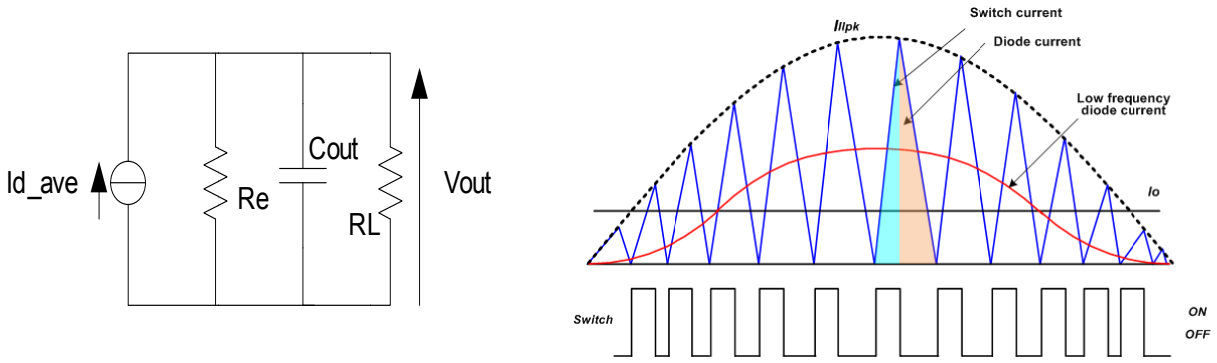


Figure 9. Power Stage Model and Boost PFC Current

The low frequency current averaged over a half-cycle yields the DC output current $I_{d(ave)}$:

$$I_{d(ave)} = \frac{1}{Ts} \times \int_0^{Ts} \left(\frac{1}{2} \times \frac{\sqrt[2]{2} \times V_{in} \times s_{in(\omega t)}}{V_{out}} \times I_{Lpk} \times s_{in(\omega t)} \right) dt = \frac{\sqrt[2]{2} \times V_{in}}{4 \times V_{out}} \times I_{Lpk} \qquad \text{(eq-29)}$$

Where I_{Lpk} is the peak inductor current at $\omega t = \pi / 2$. V_{in} is effective (RMS) input voltage.

Therefore, we can obtain the transfer function $G_{1(s)}$ of V_{out}-to-I_{Lpk}:

$$V_{out(s)} = I_{d(ave)(s)} \times \frac{\frac{1}{2} \times R_L}{1 + \frac{\frac{s}{2}}{R_L \times C_o}} = \frac{\sqrt[2]{2} \times V_{in}}{4 \times V_{out}} \times I_{Lpk(s)} \times \frac{\frac{1}{2} \times R_L}{1 + \frac{\frac{s}{2}}{R_L \times C_o}} \qquad \text{(eq-30)}$$

$$G_{1(s)} = \frac{V_{out(s)}}{I_{Lpk(s)}} = \frac{\sqrt[2]{2} \times V_{in}}{4 \times V_{out}} \times \frac{\frac{1}{2} \times R_L}{1 + \frac{\frac{s}{2}}{R_L \times C_o}} \qquad \text{(eq-31)}$$

The transfer function $G_{2(s)}$ of I_{Lpk}-to-t_{on} is:

$$G_{2(s)} = \frac{I_{Lpk(s)}}{t_{on(s)}} = \frac{\sqrt[2]{2} \times V_{in}}{L} \qquad \text{(eq-32)}$$

The transfer function $G_{3(s)}$ of t_{on}-to-V_{comp} is:

$$G_{3(s)} = \frac{t_{on(s)}}{V_{comp(s)}} = \frac{C_t}{I_{charger}} \qquad \text{(eq-33)}$$

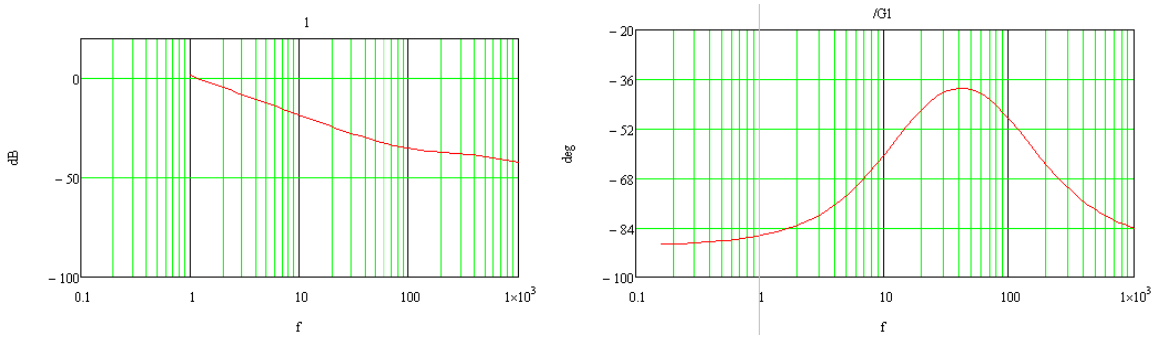
Finally, we can obtain the whole transfer function $G_{power(s)}$ of V_{out}-to-V_{comp}:

$$G_{power(s)} = \frac{V_{out(s)}}{V_{comp(s)}} = G_{1(s)} \times G_{2(s)} \times G_{3(s)} = \frac{C_t}{I_{charger}} \times \frac{{V_{in}}^2 \times R_L}{4 \times V_{out} \times L} \times \frac{1}{1 + \frac{s}{\omega p}} \qquad \text{(eq-34)}$$

Where C_t is 470pF, $I_{charger}$ is 200μA, V_{out} is 395V, R_L is full load (975Ω), C_o is 136μF, $\omega p = \frac{2}{RL \times Co}$.

$$G_{power(s)} = \frac{470 \times 10^{-12}}{200 \times^{-12}} \times \frac{230^2}{4 \times 395 \times 200 \times 10^{-6}} \times \frac{975}{1 + \frac{\frac{s}{2}}{975 \times 136 \times 10^{-6}}} \qquad \text{(eq-35)}$$

Calculated bode plot of transfer function $G_{power(s)}$:



2. Compensation E/A Transfer Function

The transfer function of E/A:

$$G_{comp(s)} = \frac{V_{comp(s)}}{V_{out(s)}} = G_o \times \frac{1}{s} \times \frac{1+\frac{s}{2\times\pi\times fcz}}{1+\frac{s}{2\times\pi\times fcp}} \quad \text{(eq-36)}$$

We can obtain that the zero is $fcz = \frac{1}{2\times\pi\times R1\times C1}$, the pole is $fcp = \frac{1}{2\times\pi\times R1\times\frac{C1\times C2}{C1+C2}}$, the DC gain is calculated as:

$$G_o = \frac{2.5}{V_{out}} \times G_m \times \frac{1}{C_1+C_2} \times \frac{\sqrt[2]{1+\left(\frac{fcr}{fz}\right)2}}{\sqrt[2]{1+\left(\frac{fcr}{fp}\right)2}} \quad \text{(eq-37)}$$

The G_m is the transconductance (100μS) of the E/A.

3. The Whole Open Loop Transfer Function

$$G_{whole(s)} = G_{power(s)} \times \frac{C_t}{I_{charger}} \times \frac{{V_{in}}^2}{4\times V_{out}\times L} \times \frac{R_L}{1+\frac{\frac{s}{2}}{R_L\times C_o}} \times G_o \times \frac{1}{s} \times \frac{1+\frac{s}{2\times\pi\times fz}}{1+\frac{s}{2\times\pi\times fp}} \quad \text{(eq-38)}$$

4. Feedback Network implementation

Desired crossover frequency:	fcr = 15Hz
Zero:	fcz = 14.6Hz
Pole:	fcp = 117Hz

We know that when $f = fcr$, the function $\left|G_{whole(j\omega)}\right|$ equals to 1, then $\left|G_{whole(j\omega)}\right| = 1, \omega = 2\times\pi\times fcr$, $\omega p = \frac{2}{RL\times C_o}$ we can obtain:

$$\left|G_{whole(j\omega)}\right| = \frac{C_t}{I_{charger}} \times \frac{{V_{in}}^2\times R_L}{4\times V_{out}\times L} \times \frac{1}{\sqrt[2]{1+\left(\frac{2\times\pi\times fcr}{\omega p}\right)^2}} \times \frac{1}{2\times\pi\times fc} \times G_o \times \frac{\sqrt[2]{1+\left(\frac{fcr}{fz}\right)^2}}{\sqrt[2]{1+\left(\frac{fcr}{fp}\right)^2}} = 1 \quad \text{(eq-39)}$$

We know $\left(\frac{2\times\pi\times fcr}{\omega p}\right)^2 \rangle\rangle 1, C1 \rangle\rangle C2, so \sqrt[2]{1+\left(\frac{2\times\pi\times fcr}{\omega p}\right)^2} \approx \frac{2\times\pi\times fcr}{\omega p}, \frac{1}{C1+C2} \approx \frac{1}{C1}$ substitute the numerical values, we can obtain as:

$$\left|G_{whole(j\omega)}\right| \approx 2.38\times10^{-6} \times \frac{230^2}{2\times395\times200\times10^{-6}\times68\times2\times10^{-6}} \times \frac{1}{(2\times\pi\times fcr)^2} \times \sqrt[2]{2} \times \frac{2.5}{395} \times \frac{115\times10^{-6}}{C1} \quad \text{(eq-40)}$$

Series compensation capacitor:

$$C_1 \approx 2.35\times10^{-6} \times \frac{230^2}{2\times395\times200\times10^{-6}\times68\times2\times10^{-6}} \times \frac{1}{(2\times\pi\times fcr_{(real)})^2} \times \frac{2.5\times115\times10^{-6}}{395} = 362nF \quad \text{(eq-41)}$$

0.33μF/50V is selected.

Series compensation resistor:

$$R_1 = \frac{1}{2\times\pi\times C_1\times f_{cz(real)}} = \frac{1}{2\times 3.14\times 0.33\times 10^{-6}\times 15} = 32.1K \qquad \text{(eq-42)}$$

33K/0805 is selected.

Parallel compensation capacitor:

$$C_{ps} = C_p \,//\, C_s = \frac{1}{2\times\pi\times R_s\times f_{cp}} = \frac{1}{2\times 3.14\times 33\times 10^3\times 117} = 41nF \qquad \text{(eq-43)}$$

$$C_p = \frac{C_s\times C_{ps}}{C_s - C_{ps}} = \frac{0.33\mu F\times 41nF}{0.33\mu F - 41nF} = 46.8nF \qquad \text{(eq-44)}$$

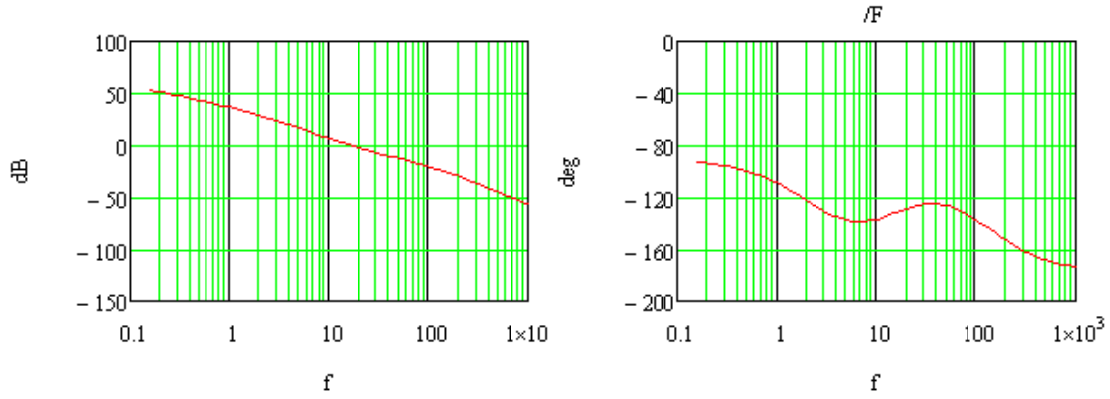
47nF/50V is selected.

5. Calculated Overall Loop Bode Plot

$$G_{whole(s)} = G_{power(s)}\times G_{comp(s)} = \frac{C_t}{I_{charger}}\times\frac{{V_{in}}^2}{4\times V_{out}\times L}\times\frac{R_L}{1+\frac{\frac{s}{2}}{R_L\times C_o}}\times G_o\times\frac{1}{s}\times\frac{1+\frac{s}{2\times\pi\times fz}}{1+\frac{s}{2\times\pi\times fp}}$$

(eq-45)

Calculated bode plot:



Cross frequency: $f_{cr(real)} = \left|root\left(\left|G_{whole(2\pi f)}\right| - 1, f\right)\right| = 15.944Hz$ (eq-46)

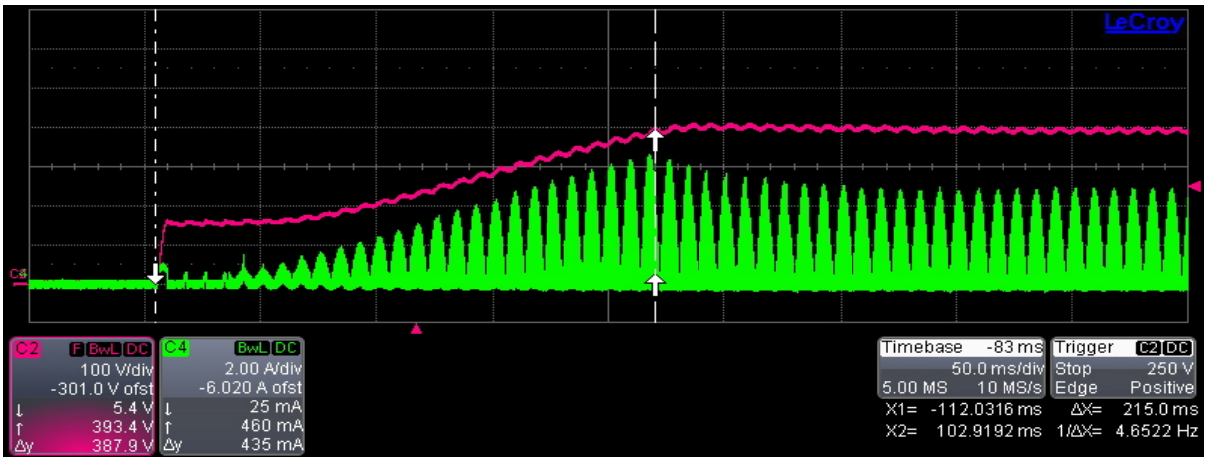
Phase Margin: $\Phi = 180 + 180\times\frac{1}{\pi}\times\arg\left(G_{whole(2\pi fcr)}\right) = 48.36\,\text{deg}$ (eq-47)

Appendix1 Experimental Verification

The table is the experimental results of the converter.

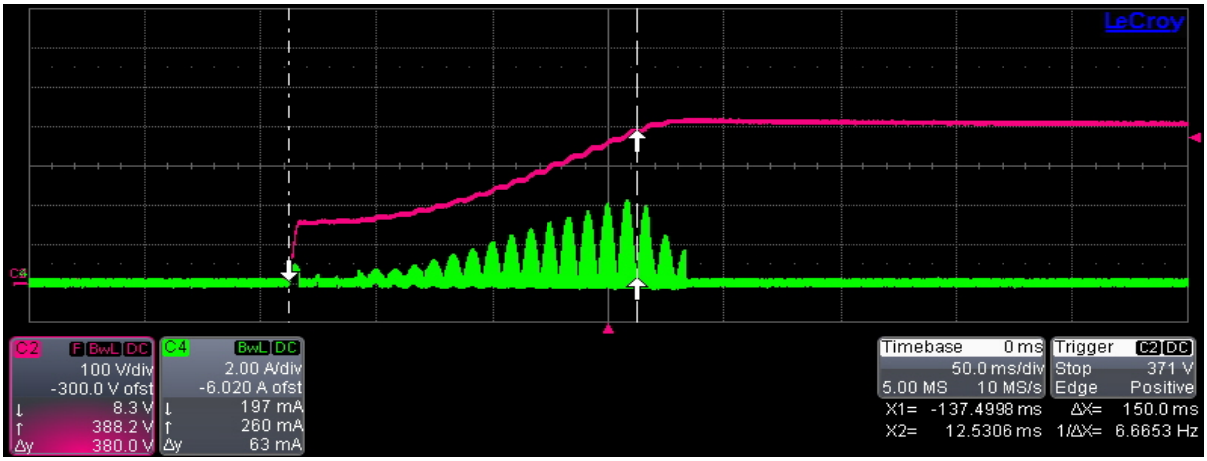
Vin	Pout(W)	Pin(W)	η (%)	PF	THD
90V_{ac}	80	84.4	94.8	0.994	11.5
	160	169.5	94.4	0.997	7.1
115V_{ac}	80	83.5	95.8	0.991	13.5
	160	166.6	96.0	0.996	8.3
230V_{ac}	80	82.63	96.8	0.945	24.8
	160	163.1	98.1	0.977	11.9
264V_{ac}	80	82.62	96.8	0.900	42.5
	160	162.9	98.2	0.950	23.3

Start-up waveforms of output voltage: Figures 10 and 11 show the start-up time for 115V_{ac} full load and no load. The inductor current increases smoothly due to keep in the closed loop soft-start.



CH2: DC Output Voltage – CH4: Inductor Current

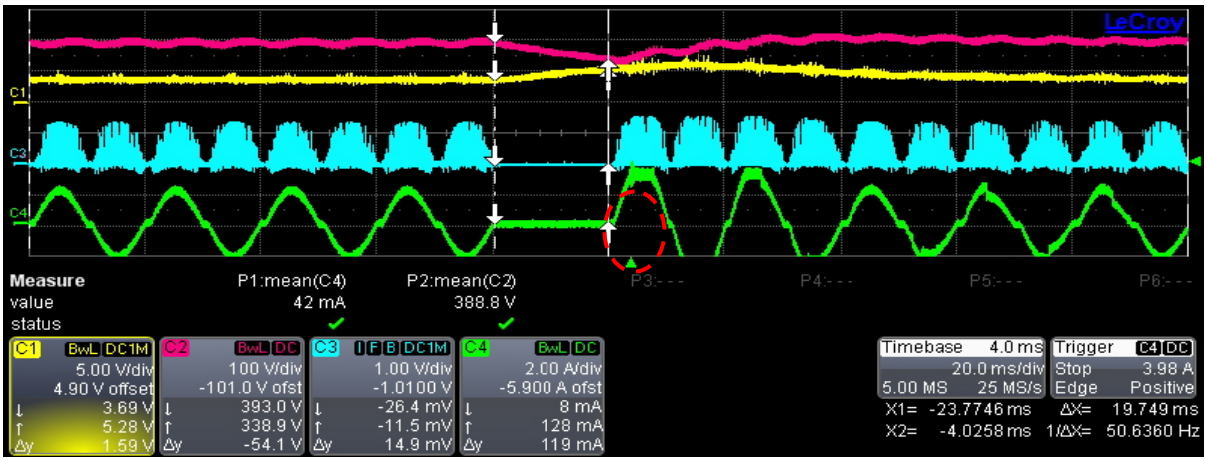
Figure 10. Start-Up Waveform of V_{out} at 115V_{ac} Full Load



CH2: DC Output Voltage – CH4: Inductor Current

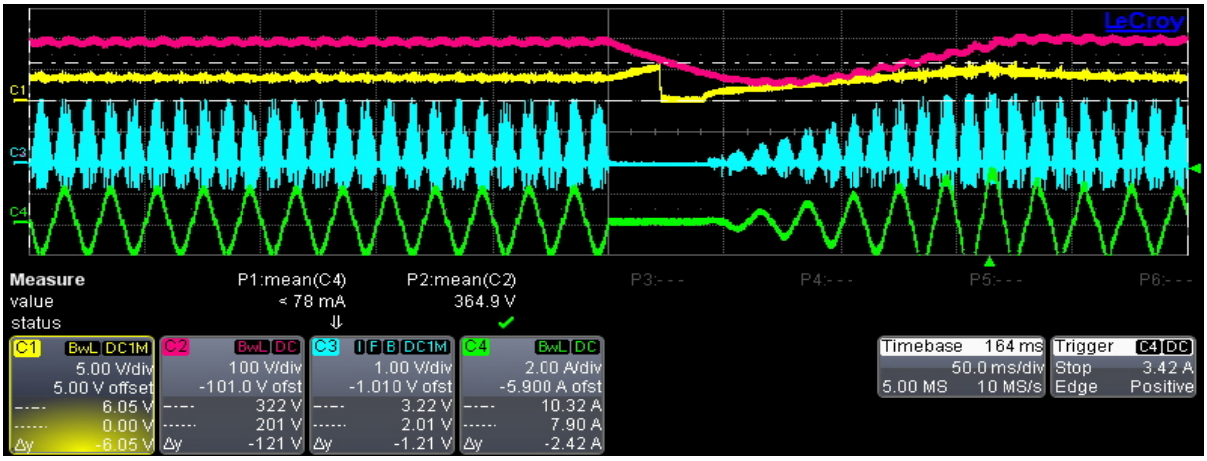
Figure 11. Start-Up Waveform of V_{out} at 115V_{ac} No Load

Figures 12 and 13 show the output voltage response when the AC input is omitted for 20ms and 40ms. As Figure 12 observed that V_{comp} increased when the AC input is absent for 20ms, the peak inductor current is limited cycle-by-cycle by OCP comparator. But when the AC input is absent for over 20ms, the V_{comp} is reduced to zero rapidly and restarts smoothly when AC is applied again as Figure 13 shown.



CH1: V_{comp} – CH2: DC Output Voltage – CH3: Sense Resistor Voltage – CH4: AC Input Current

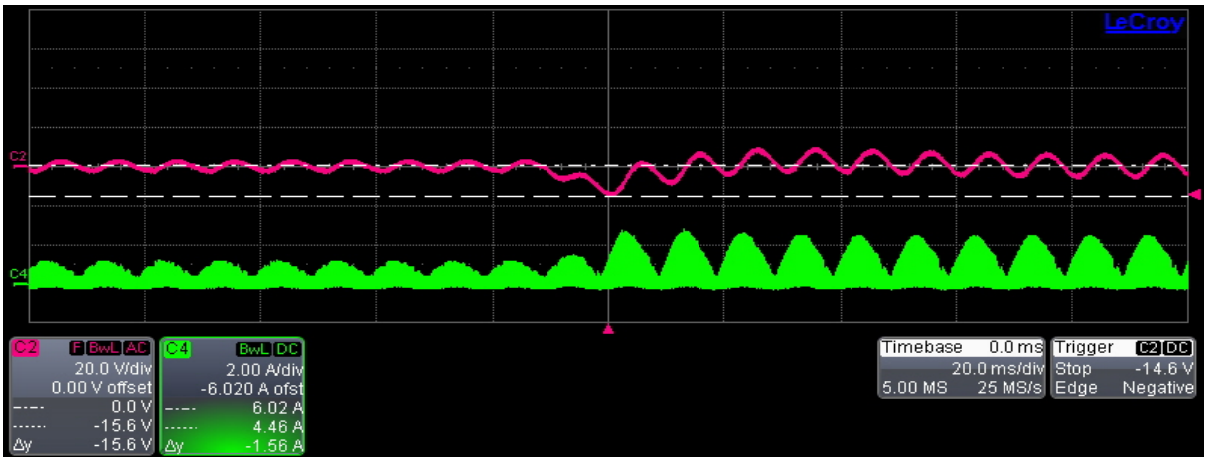
Figure 12. AC-Absent for 20ms Detection Operation



CH1: V_{comp}p – CH2: DC Output Voltage – CH3: Sense Resistor Voltage – CH4: AC Input Current

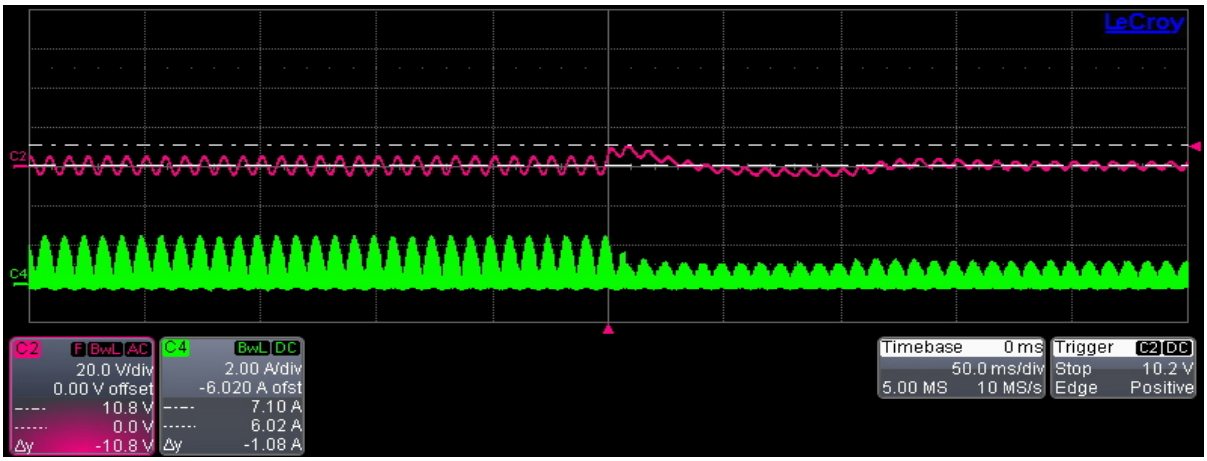
Figure 13. AC-Absent for 40ms Detection Operation

Figures 14 and 15 show the output response and inductor current for 115V_{ac} full load and 115V_{ac} no load.



CH2: DC Output Voltage – CH4: Inductor Current

Figure 14. Output Response of Dynamic Load (60W—160W@230V_{ac})



CH2: DC Output Voltage – CH4: Inductor Current

Figure 15. Output Response of Dynamic Load (160W—60W@230V_{ac})

Loop gain. The frequency response is measured at four conditions. Figure 16 shows that at 264V_{ac} input voltage the crossover frequency is 20.44Hz and the phase margin is 57.0deg. Figure 17 show 230V_{ac} input voltage, the crossover frequency is 18.44Hz and the phase margin is 54.7deg. Figure 18 show 115V_{ac} input voltage, the crossover frequency is 6.91Hz and the phase margin is 52.7deg. Figure 19 show 90V_{ac} input voltage, the crossover frequency is 5.2Hz and the phase margin is 52.1deg.

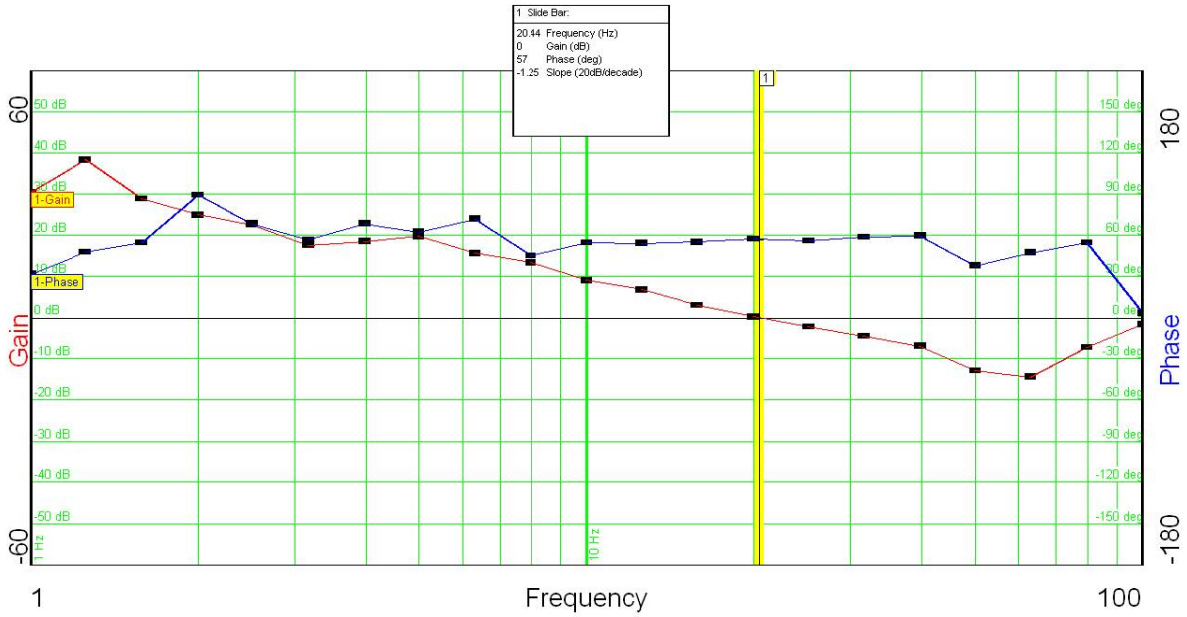


Figure 16. Phase Margin @264V_{ac}-50Hz Full Load

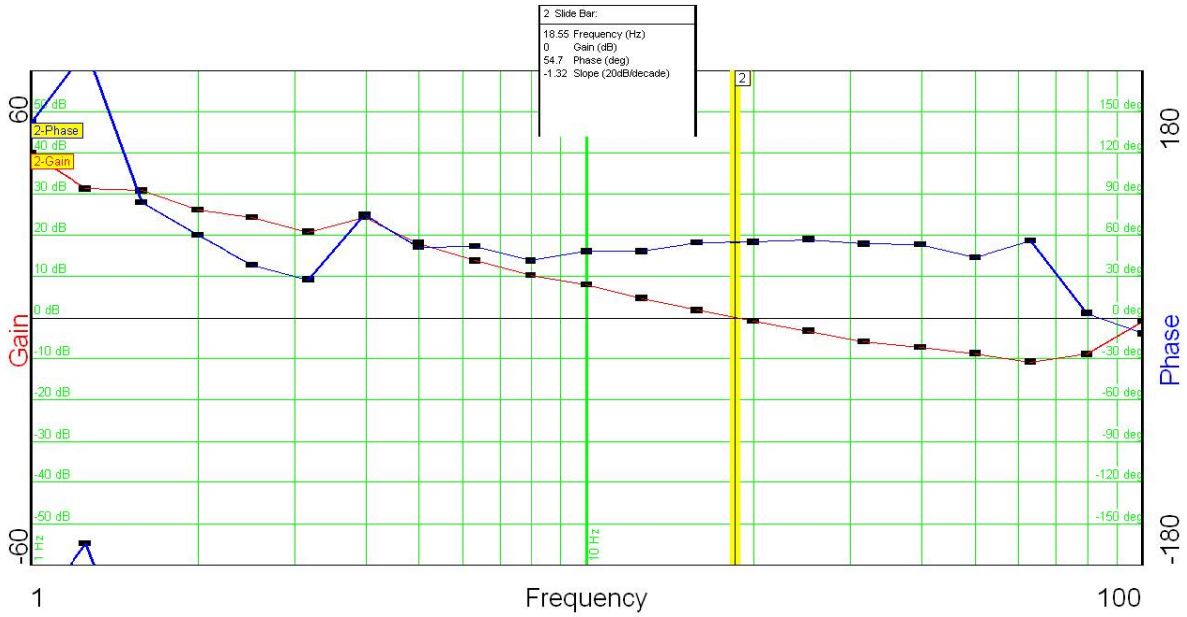


Figure 17. Phase Margin @230V_{ac}-50Hz Full Load

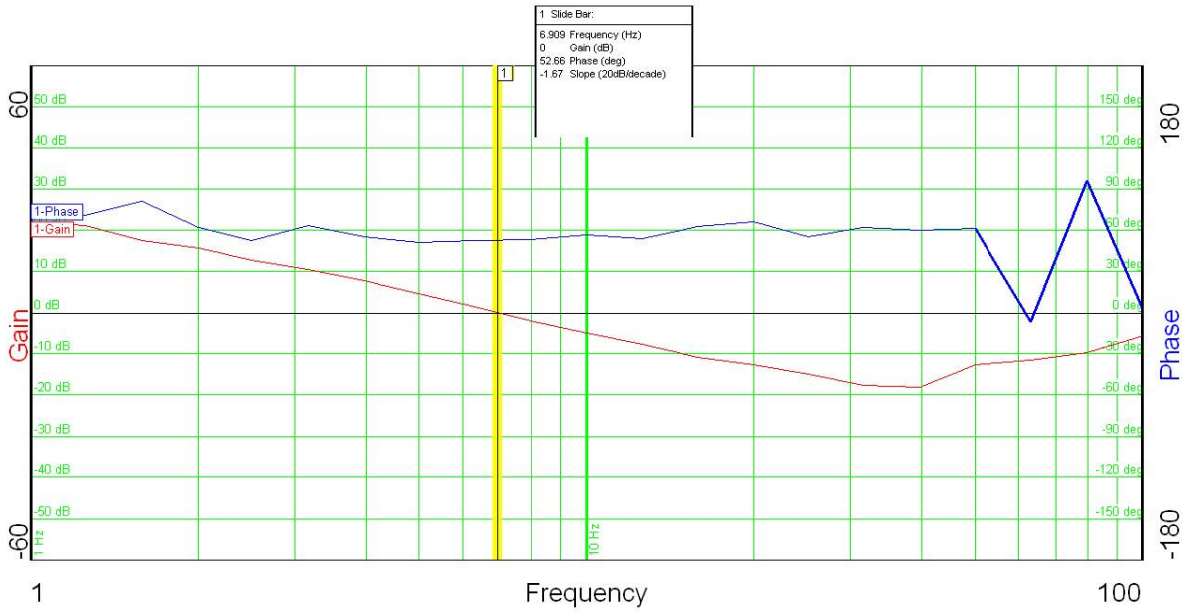


Figure 18. Phase Margin @115V_{ac}-50Hz Full Load

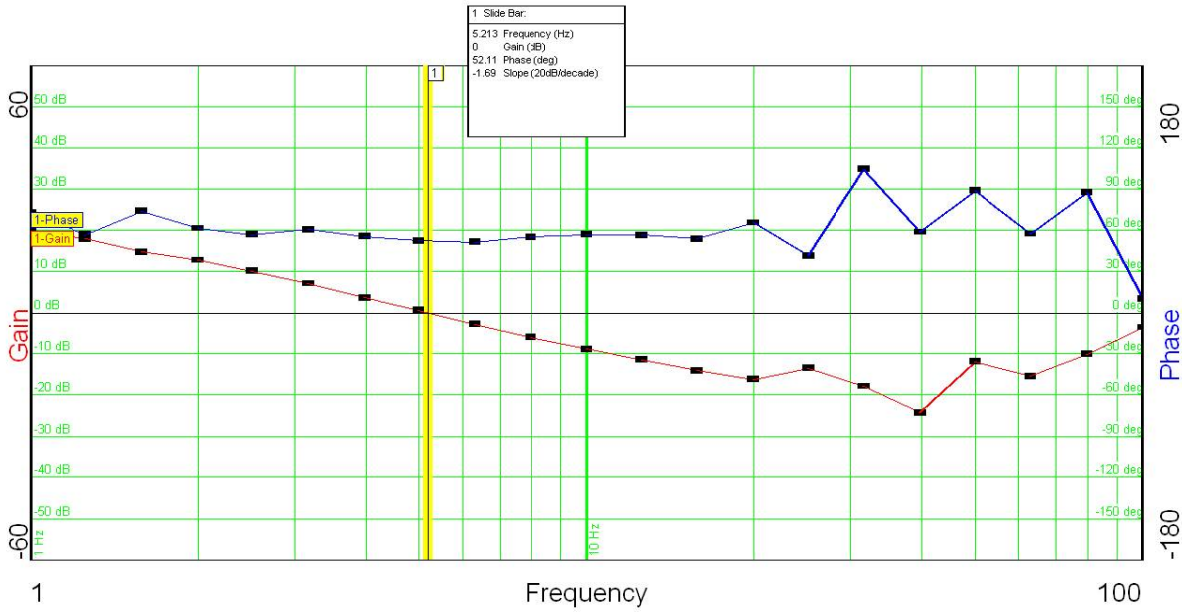


Figure 19. Phase Margin @90V_{ac}-50Hz Full Load

Appendix 2: PCB LAYOUT

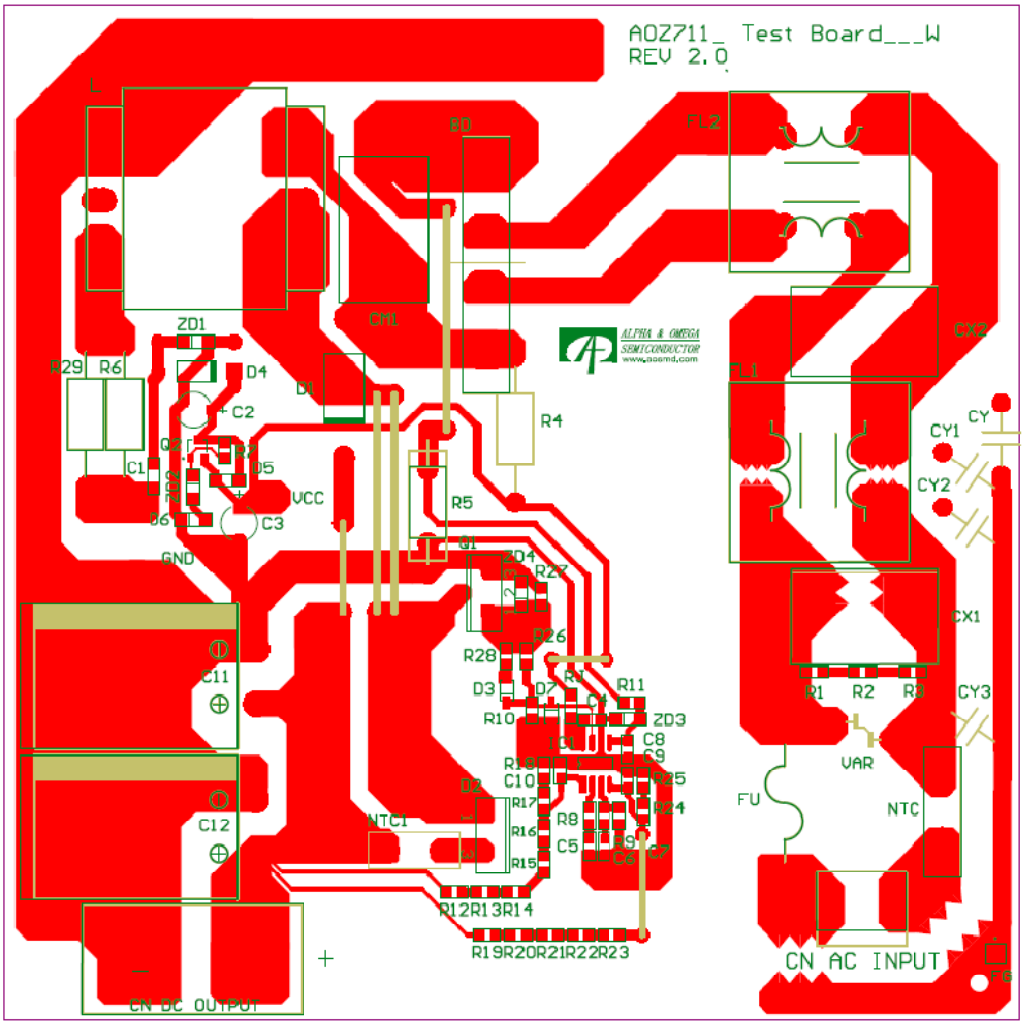


Figure 20. Recommended PCB Layout

PCB Layout Guide

The following points are good PCB layout guild-line for a PFC stage.

1. To keep the IC GND pin as clean as possible, the power stage ground and the signal ground must be separated. Then both grounds are connected by a separated signal line. At the same time, the signal ground end of this line should be connect to the end of current sense resistor which is connected to power ground as shown in Figure 20. Figure 21 shows that if the signal ground end connects directly to the power stage ground, the CS pin is easily interrupted. Figure 22 shows, the inductor current ramp-up to a higher level and becomes distorted since the signal ground is interrupted by noise and the IC cannot detect the zero current signal.

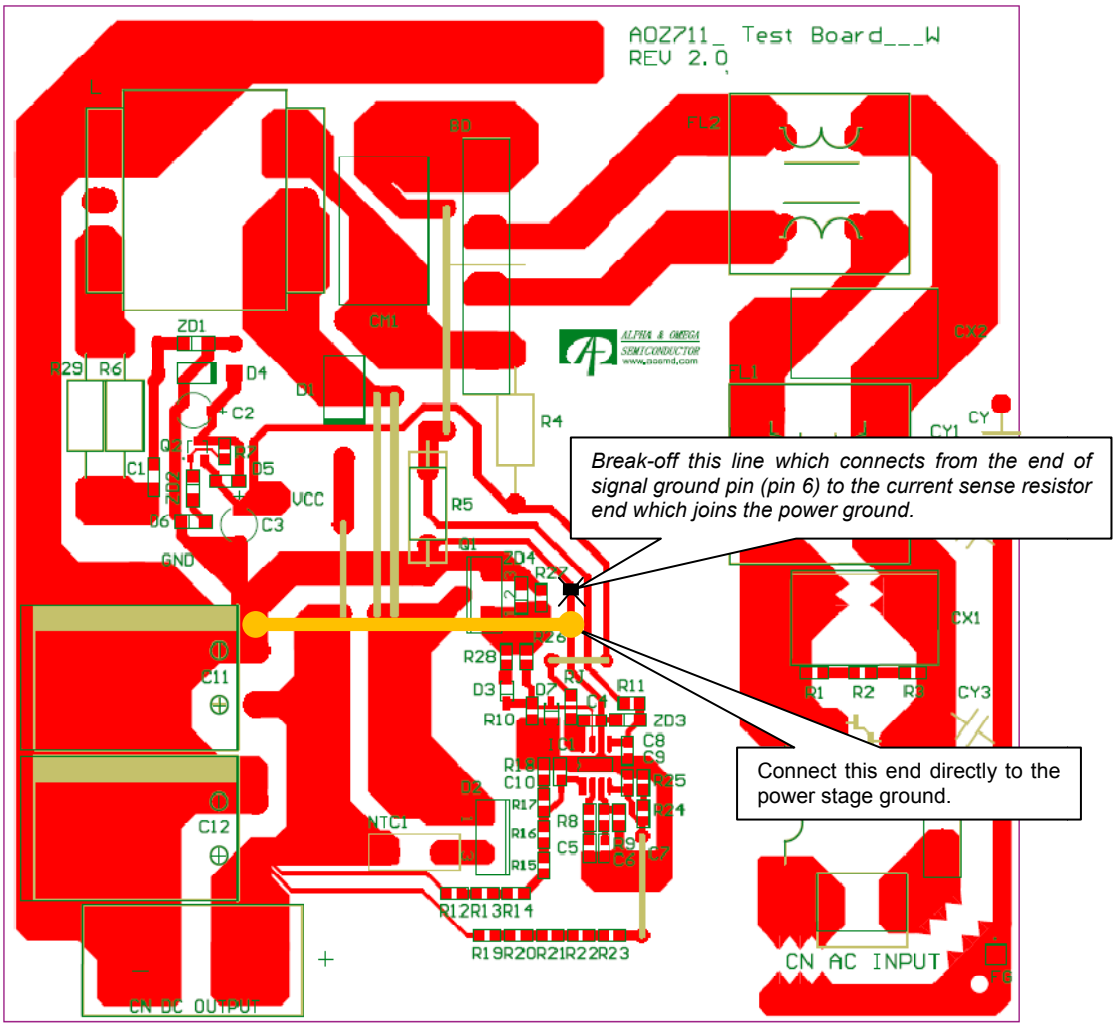
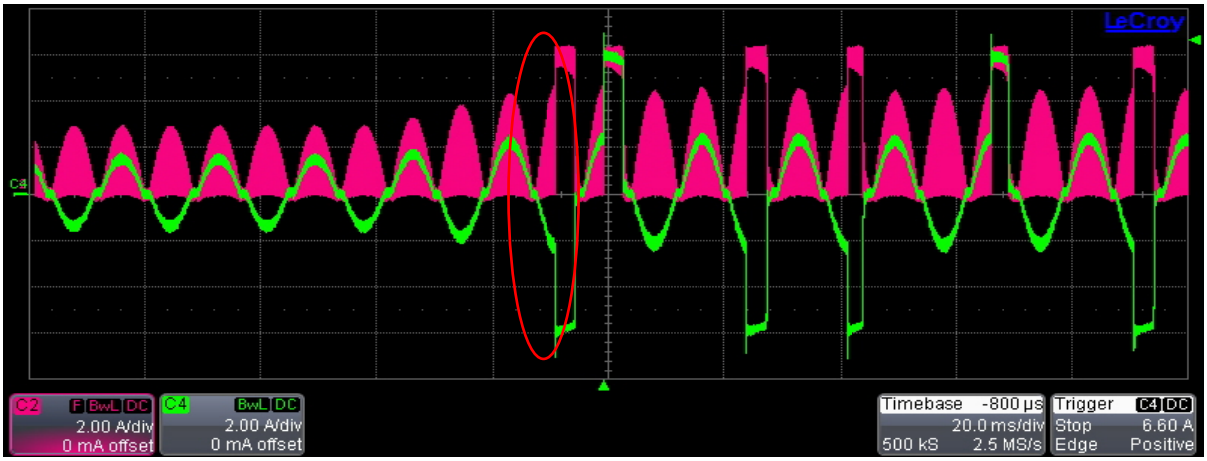


Figure 21. Bad Layout (*The Signal Ground Connects Directly to Power Ground*)



CH2: Inductor Current – CH4: Input Current

Figure 22. Interrupted Input Current Waveform and Inductor Current

2. The PFC MOSFET gate drive loop path should be minimized
3. Minimize the trace length to INV pin. Since the feedback node is high impedance, the trace from the output resistor divider to INV pin should be as short as possible.
4. Switching current sense (CS pin) is very important for the stable operation of PFC stage. Normally, a RC filter is recommended to reduce the noise applied to CS pin.
5. The V_{cc} decoupling capacitor C_{vcc} needs to be placed as closed as possible to IC V_{cc} and GND pin.

Appendix 2: BILL OF MATERIALS (BOM)

Ref Designation	Value	Description	Package	Manufacturer
FU	5A/250V	Fuse, 5A/250V		
NTC	SCK-044K	NTC, SCK-044K		
VAR	10D-471	VAR, 10D-471		
CX1	0.22μ/275VAC	X CAP, 0.22μF/275VAC		
FL1	25mH	Common mode EMI filter, 25mH		
CX2	0.33μF/275VAC	X CAP, 0.33μF/275VAC		
BD	D15XB60	AC Bridge rectifier, D15XB60		
CM1	0.68μF/630V	DM filter cap, 0.68μF/630V		
L	200μH	PFC chock, 200μH	EER3019	
Q1	AOT11CF60	AOT11CF60	TO-220F	AOS
D2	BYV29X	PFC boost diode, BYV29X	TO-220F	NXP
C11,C12	68μF/450V	Bulk cap, KMF 450V/68μF		Samyoung
R5	0.1Ω/5W	Rense resistor, 0.1Ω/5W		
D1	1N5408	Diode, 1N5408	DO-241	
R12~R16, R19~R23	1MΩ	Thick Film Res, 1%	1206	
R17	27KΩ	Thick Film Res, 1%	0603	
R18	4.22KΩ	Thick Film Res, 1%	0603	
R24	27KΩ	Thick Film Res, 1%	0603	
R25	3.9KΩ	Thick Film Res, 1%	0603	
C10	1nF/50V	Ceramic Cap, 50V, X5R/X7R	0603	
C9	10nF/50V	Ceramic Cap, 50V, X5R/X7R	0603	
R11	240Ω	Thick Film Res, 1%	0603	
C8	100pF/50V	Ceramic Cap, 50V, X5R/X7R	0603	
R27	10KΩ	Thick Film Res, 1%	0603	
R26	10Ω	Thick Film Res, 1%	0603	
R28	2.4Ω	Thick Film Res, 1%	0603	
D3,D7	LL4148			
ZD3(optional)	3.9V Zener	3.9V Zener 0.5W		
R8	0Ω	Thick Film Res, 1%	0603	
C5	470pF/50V	Ceramic Cap, 50V, X5R/X7R	0603	
C6	0.22uF/50V	Ceramic Cap, 50V, X5R/X7R	0603	
C7	47nF/50V	Ceramic Cap, 50V, X5R/X7R	0603	
R9	10KΩ	Thick Film Res, 1%	0603	
C4	0.1μF/50V	Ceramic Cap, 50V, X5R/X7R	0603	
C3	22μF/50V	EC Cap, 50V	5*11	
IC1	AOZ7111	CRM PFC Controller	SO-8	AOS

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