Design Procedure using AOZ1361DI

Introduction

The AOZ1361DI is a high-side load switch intended for applications that require circuit protection. The device operates from voltages between 4.5V and 28V. The internal current limiting circuit protects the input supply voltage from large load current. The current limit can be set with an external resistor. The device employs internal soft-start circuitry to control inrush current due to highly capacitive loads associated with hot-plug events. The AOZ1361DI is available in a 10-pin 4mm x 4mm DFN package.

This application note briefly discusses the design procedure using AOZ1361DI, and will focus on how to set the current limit point and select the soft-start capacitor.

Typical Application

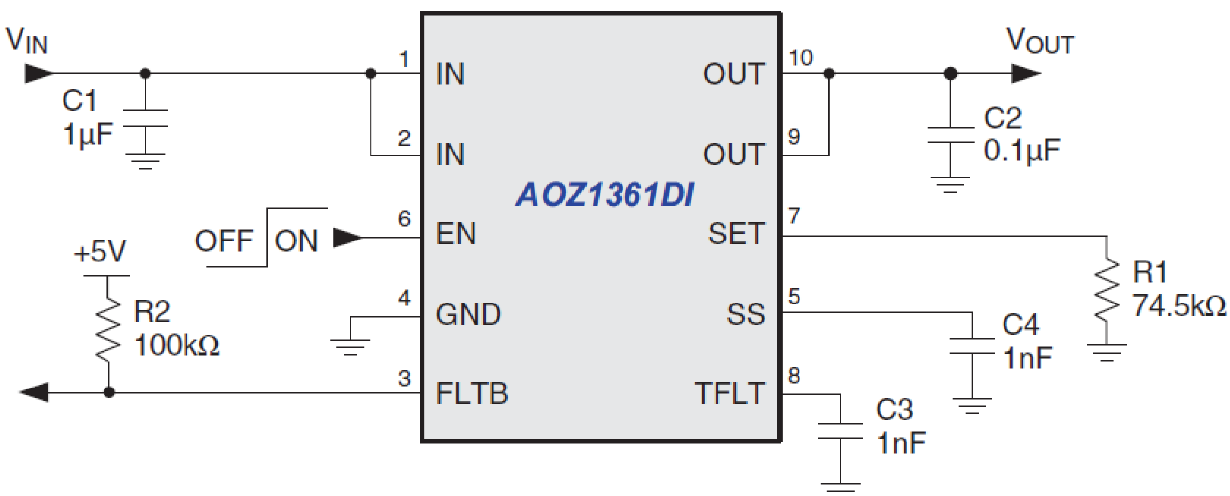

Figure 1. Typical Application of AOZ1361DI

As shown in Figure 1, the current limit can be set by the resistor R1 between SET pin and GND, and the soft start time can be set by the cap C4 between SS pin to GND.

Design Procedure

Input Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input and provides the instantaneous current needed each time the switch turns on and to limit input voltage drop. Also, it is to prevent high-frequency noise on the power line from passing through the output of the power side. The choice of the input capacitor is based on its ripple current and voltage ratings rather than its capacitor value. The input capacitor should be located as close to the VIN pin as possible. A 1µF ceramic cap is recommended. However, higher capacitor values further reduce the voltage drop at the input.

Output Capacitor Selection

The output capacitor acts in a similar way. A small 0.1µF capacitor prevents high-frequency noise from going into the system. Also, the output capacitor has to supply enough current for a large load that it may encounter during system transients. This bulk capacitor must be large enough to supply fast transient load in order to prevent the output from dropping.

Current Limit Setting

Design Example: VIN=12V, Io=2A, Co=100µF

The current limit should be higher than the Io; meanwhile, we have to consider the power dissipation which happened under the over current or short conditions, which can be calculated by the equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LIMT}$$

For this case, we set I_{LIM} to 50% higher than Io, and thus, R_{SET}=61kohm to set I_{LIM}=3A according to Figure 2.

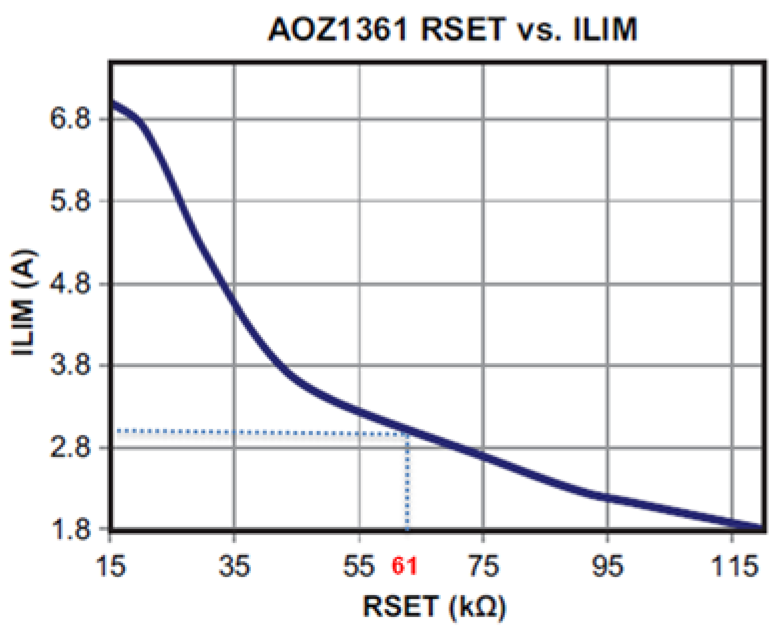

Figure 2. Current Limit vs. R_{SET} (VIN=12V)

Soft-Start Time Calculation:

To avoid any start-up issue, the minimum soft-start time can be calculated as below:

$$Ton\_\min = \frac{k_{factor} \times Co \times VIN}{I_{LIM}}$$

Where k_{factor} is the experience factor to cover the additional load during the start-up, output capacitor variation and etc.

Usually k_{factor} equal to 2 can guarantee the load switching start-up.

Then,

$$Ton\_\min = \frac{2 \times 100uF \times 12V}{3A} = 800us$$

Soft-Start Capacitor Calculation:

The slew rate control circuitry applies a voltage on the gate of the PMOS switch in a manner such that the output voltage and current are ramped up linearly until they reach a steady-state load current level. The slew rate can be adjusted by an external capacitor connected to the SS pin to ground. The slew rate rise time, Ton, can be set using the following equation:

$$Ton = \frac{Css \times VIN}{30uA}$$

For the example case, since

$Ton\_\min = \frac{2 \times 100uF \times 12V}{3A} = 800us$, the minimum Css can be calculated by below equation:

$$Css\_\min = \frac{Ton\_\min \times 30uA}{VIN} = \frac{800us \times 30uA}{12V} = 2nF$$

TFLT

TFLT is a fault delay pin, and its delay time is adjustable by a capacitor connected from TFLT to GND. The delay time can be calculated by:

$$T_{TLFT}(us) = 600(us/nF) \times C_{TFLT}(nF)$$

Summary:

For the application VIN=12V, Io=2A, Co=100μF, we can set R_{SET}=61kohm, Css=2nF.

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