



General Description

- Trench Power AlphaSGT2™ technology
- Low $R_{DS(ON)}$ and optimized switching performance
- RoHS 2.0 and Halogen-Free Compliant

Applications

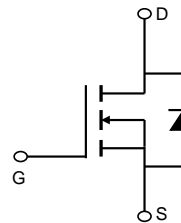
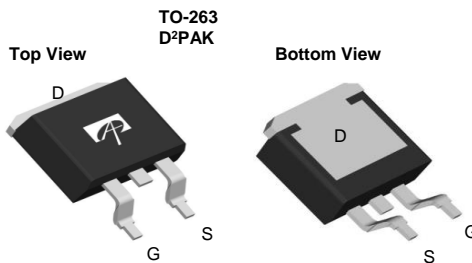
- Industrial Application
- Telecom and Server Power Supply

Product Summary

V_{DS}	80V
I_D (at $V_{GS}=10V$)	140A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 2.7m Ω
$R_{DS(ON)}$ (at $V_{GS}=8V$)	< 3m Ω

100% UIS Tested
100% Rg Tested

Max $T_j=175^\circ C$



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOB66811L	TO-263	Tape & Reel	800

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	$T_C=25^\circ C$	140	A
	$T_C=100^\circ C$	140	
Pulsed Drain Current ^C	I_{DM}	530	
Continuous Drain Current	$T_A=25^\circ C$	44	A
	$T_A=70^\circ C$	37	
Avalanche Current ^C	I_{AS}	75	A
Avalanche energy $L=0.1mH$ ^C	E_{AS}	281	mJ
Power Dissipation ^B	$T_C=25^\circ C$	310	W
	$T_C=100^\circ C$	155	
Power Dissipation ^A	$T_A=25^\circ C$	10	W
	$T_A=70^\circ C$	7	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	12	15	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	50	
Maximum Junction-to-Case	$R_{\theta JC}$	0.4	0.48	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	80			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.6	3.2	3.8	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		2.2 3.3	2.7 4	mΩ
		V _{GS} =8V, I _D =20A		2.4	3	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		90		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current ^G				140	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =40V, f=1MHz		5750		pF
C _{oss}	Output Capacitance			1580		pF
C _{rss}	Reverse Transfer Capacitance			30		pF
R _g	Gate resistance	f=1MHz	0.5	1.0	1.5	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =40V, I _D =20A		77	110	nC
Q _{gs}	Gate Source Charge			21		nC
Q _{gd}	Gate Drain Charge			15		nC
Q _{oss}	Output Charge	V _{GS} =0V, V _{DS} =40V		112		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =40V, R _L =2.0Ω, R _{GEN} =3Ω		19		ns
t _r	Turn-On Rise Time			7		ns
t _{D(off)}	Turn-Off DelayTime			45		ns
t _f	Turn-Off Fall Time			10		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		35		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		175		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 175° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=175° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO MAKE CHANGES TO PRODUCT SPECIFICATIONS WITHOUT NOTICE. IT IS THE RESPONSIBILITY OF THE CUSTOMER TO EVALUATE SUITABILITY OF THE PRODUCT FOR THEIR INTENDED APPLICATION. CUSTOMER SHALL COMPLY WITH APPLICABLE LEGAL REQUIREMENTS, INCLUDING ALL APPLICABLE EXPORT CONTROL RULES, REGULATIONS AND LIMITATIONS.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:

http://www.aosmd.com/terms_and_conditions_of_sale

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

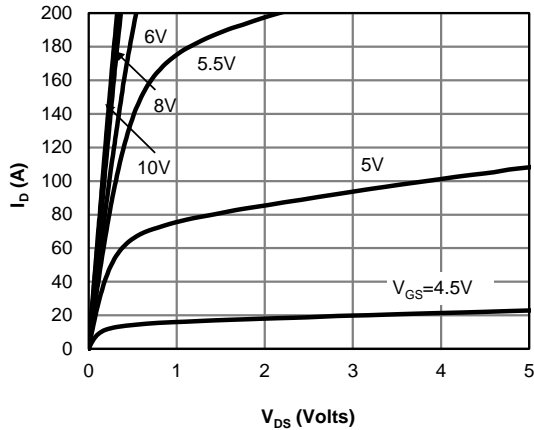


Figure 1: On-Region Characteristics (Note E)

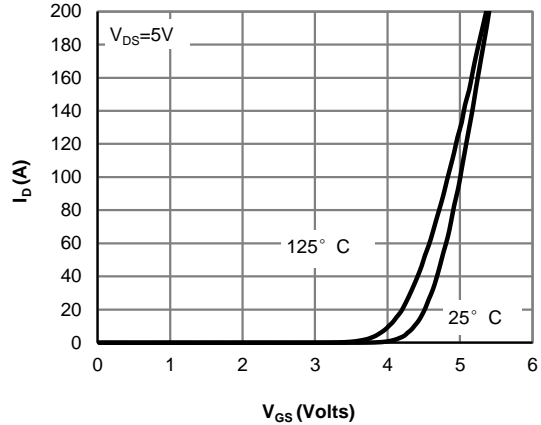


Figure 2: Transfer Characteristics (Note E)

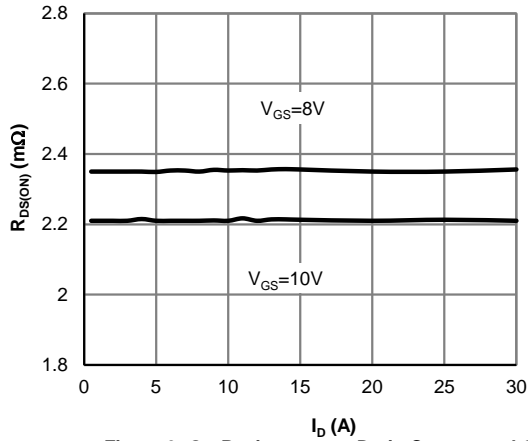


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

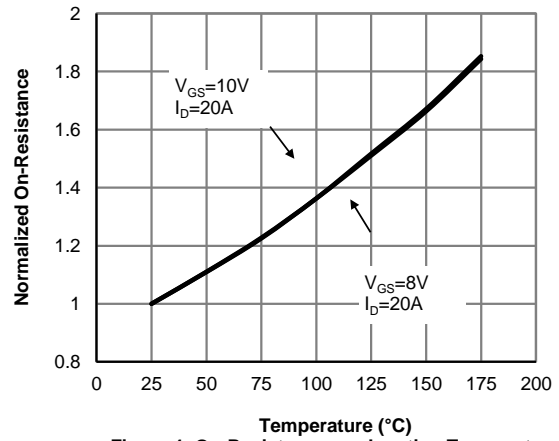


Figure 4: On-Resistance vs. Junction Temperature (Note E)

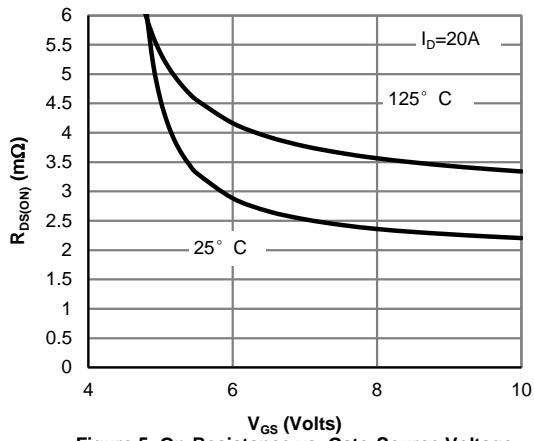


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

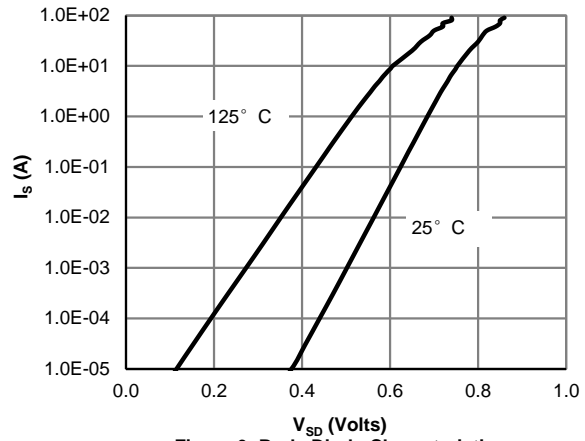


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

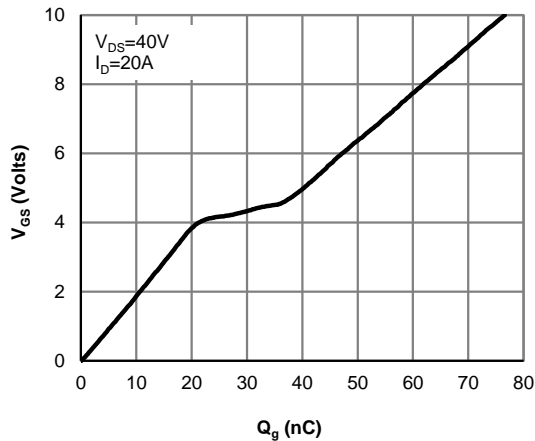


Figure 7: Gate-Charge Characteristics

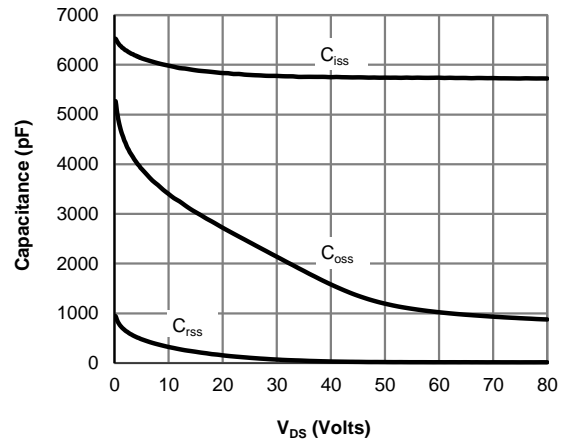


Figure 8: Capacitance Characteristics

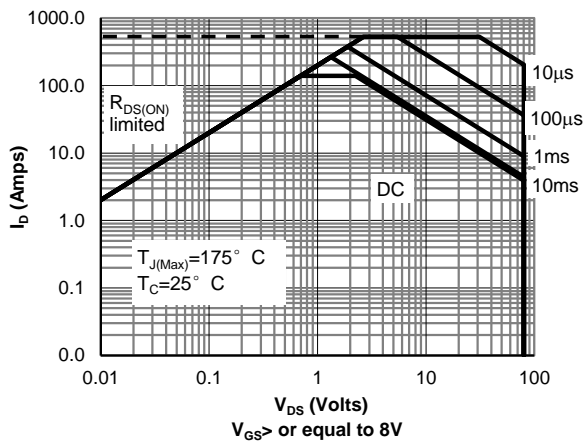


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

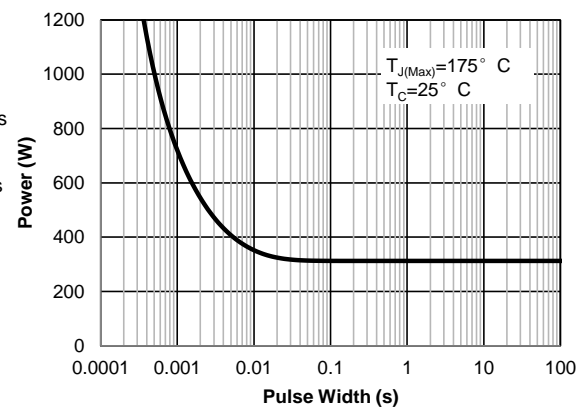


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

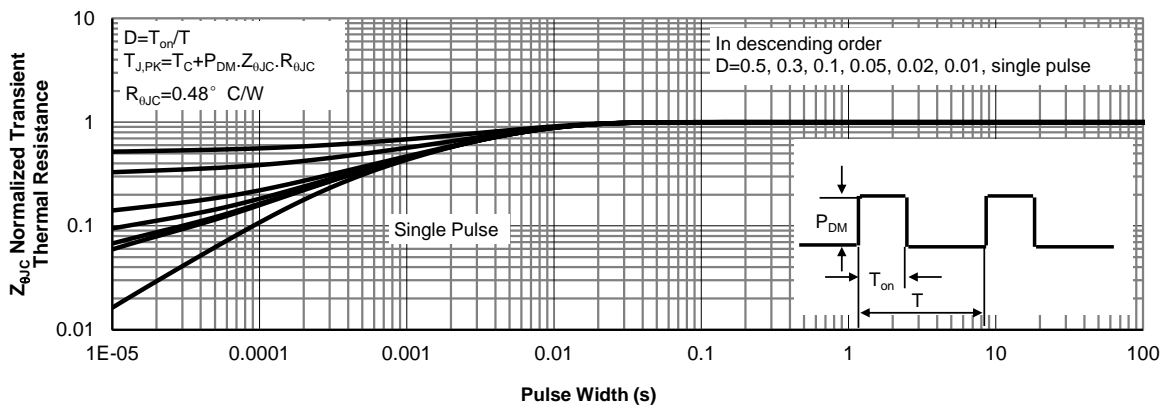


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

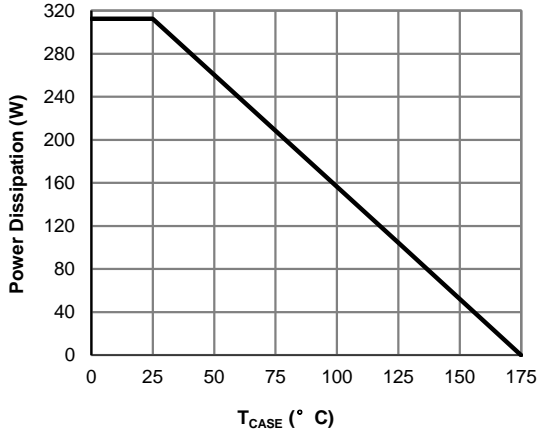


Figure 12: Power De-rating (Note F)

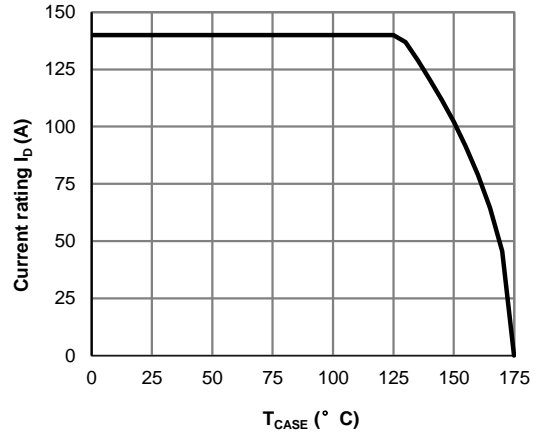


Figure 13: Current De-rating (Note F)

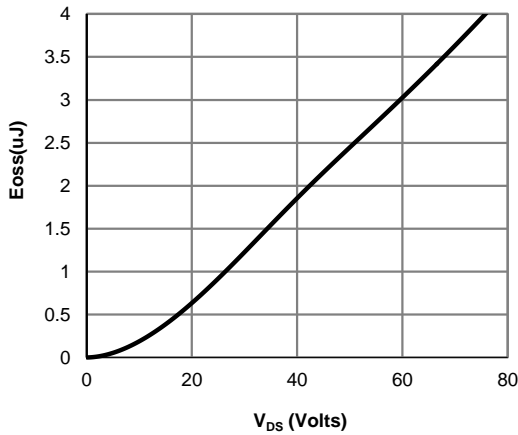


Figure 14: Coss stored Energy

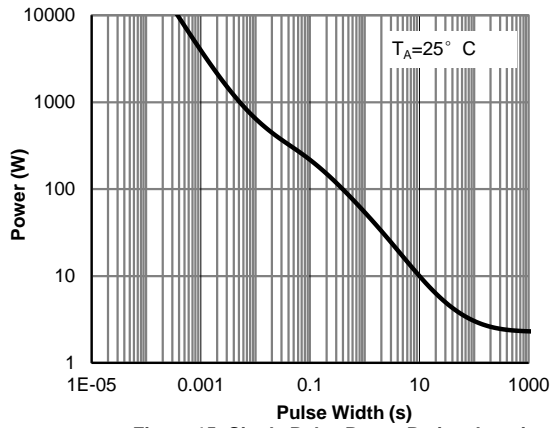


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

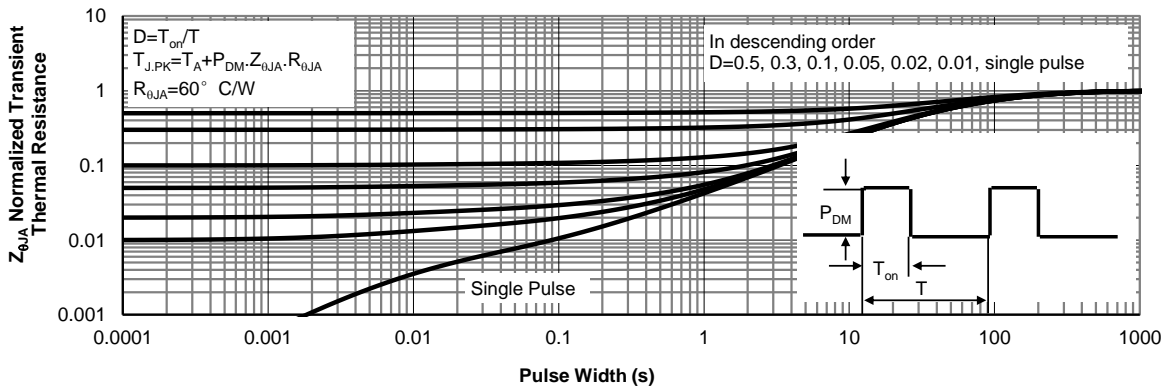


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

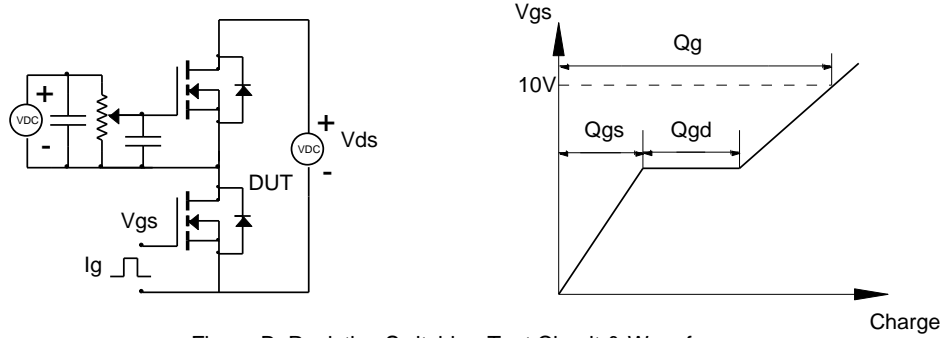


Figure B: Resistive Switching Test Circuit & Waveforms

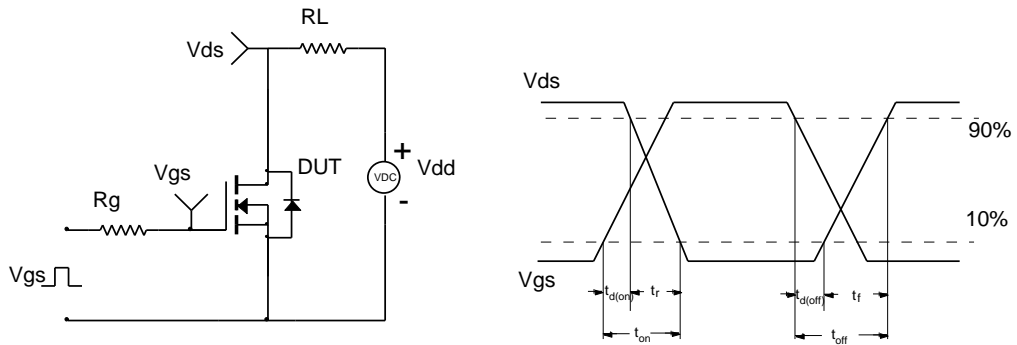


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

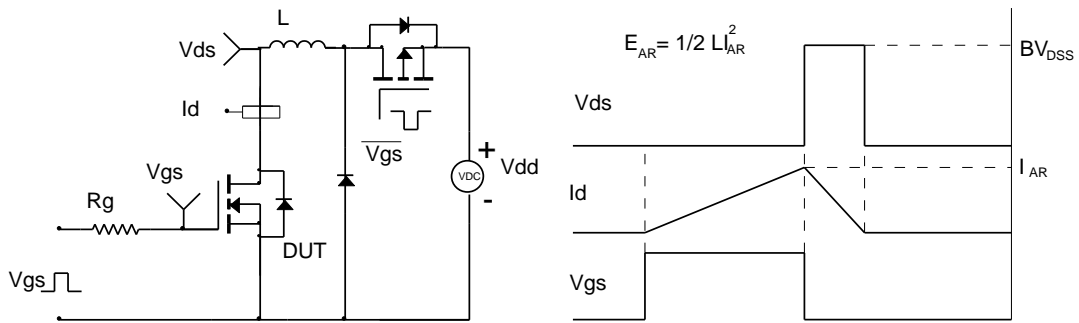


Figure D: Diode Recovery Test Circuit & Waveforms

