AOZ7501

Current Mode Flyback Controller with HV Start-Up and Advanced Features

General Description

AOZ7501 is a series of current mode controllers for flyback topology applications. The AOZ7501 series integrates high voltage start-up circuitry. The series also provides frequency foldback and skip mode during light load conditions to achieve excellent light load efficiency and low power standby mode. As well as a digital Spread Spectrum Clock Generator (SSCG) to improve EMI emissions. In addition, AOZ7501 includes cycle-by-cycle current limit, Under Voltage Lockout (UVLO), VDD OVP, DMAG pin OVP, Over Load Protection (OLP), CS pin protection and Secondary-Side Diode Short protection (SSDS).

Applications

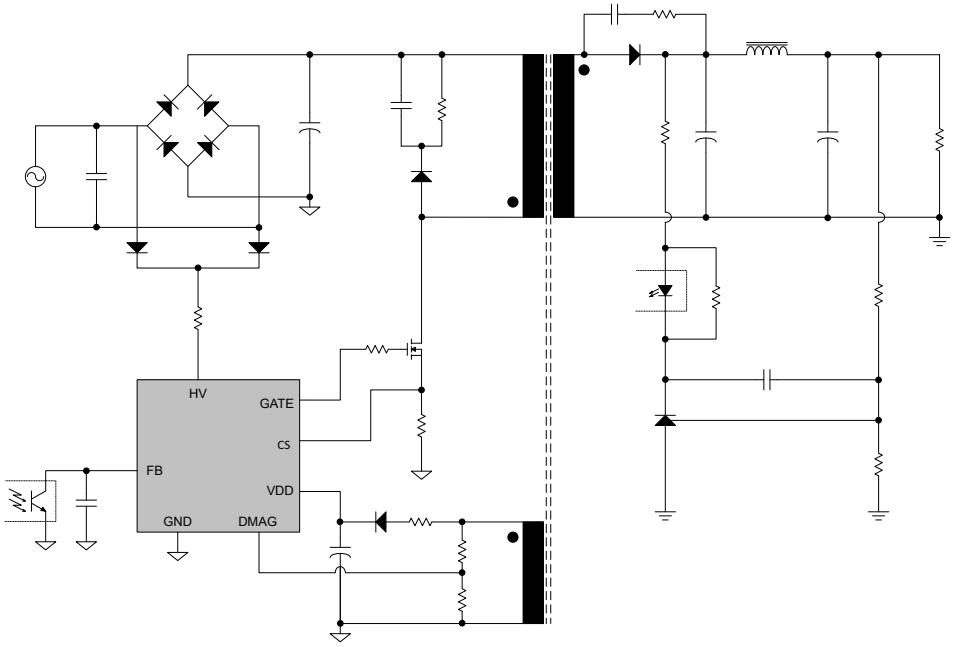
- SMPS
- NB adapter
- Charger

Features

- Integrated HV start-up circuitry
- Under-voltage lockout: 7V/15V
- Cycle-by-cycle current limit
- Minimum on time modulation to minimize acoustic noise
- Frequency foldback mode and skip mode operation
- Frequency spread by spread spectrum clock generator
- VDD over-voltage protection
- DMAG pin over-voltage protection
- Secondary-side diode short protection
- CS pin protection
- Internal over-temperature protection

Green Product

Typical Application



Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ7501XAI	-40°C to +125°C	SO-7	Green Product

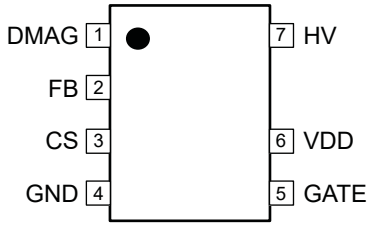
AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

AOZ7501□AI
Protection
G, L, A, R, H

Part Number	AOZ7501GAI	AOZ7501LAI	AOZ7501AAI	AOZ7501RAI	AOZ7501HAI
Switching Frequency	65kHz	65kHz	65kHz	65kHz	130kHz
OLP / SSDS	Auto Recovery	Auto Recovery	Latch	Auto Recovery	Auto Recovery
VDD OVP	Auto Recovery	Latch	Latch	Auto Recovery	Auto Recovery
DMAG OVP	Latch	Latch	Latch	Auto Recovery	Latch
DMAG Low	Auto Recovery	Latch	Latch	Latch	Auto Recovery
Internal OTP	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery

Table 1. Protection Version

Pin Configuration



SO-7
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	DMAG	Demagnetize pin for voltage sense.
2	FB	Feedback pin for voltage loop.
3	CS	Current sense pin for current loop.
4	GND	Ground.
5	GATE	PWM output driver for external power MOSFET.
6	VDD	Power supply pin for controller.
7	HV	High voltage start-up current supply.

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
V_{HV}	0V to 500V
V_{VDD}	0V to 30V
V_{GATE}	-0.3V to 15V
V_{DMAG} , V_{FB}, V_{CS}	-0.3V to 6V
GND	-0.3V to +0.3V
Package Power Dissipation	0.650W
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD HBM(1) (Except HV Pin)	4kV
ESD CDM(1) (Except HV Pin)	1kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{DD})	7.5V to 25V
Ambient Temperature (T_A)	-40°C to +105°C
Package Thermal Resistance SO-7 (θ_{JA})	160°C/W

Electrical Characteristics

T_A = -25°C to 85°C, V_{CC} = 15V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
HV						
I_{HV}	Supply Current from HV Pin	V_{HV} = 100V, V_{DD} = 0V, Controller Off		1.5		mA
I_{HV-LC}	Leakage Current from HV Pin	V_{HV} = 500V, V_{DD} = 15V, Controller On		0.8		µA
VDD						
V_{DD-OVP}	VDD Over-Voltage Protection		26	27.5	29	V
$T_{VDD-OVP}$	VDD Over-Voltage Protection De-Bounce Time			20		µs
V_{DD-ON}	Turn-On Threshold Voltage		14	15	16	V
$V_{DD-UVLO}$	Turn-Off and Under-Voltage Lock-Out		6.5	7	7.5	V
V_{DDM-E}	VDD Hold-Up Mode Entry Level			7.5		V
V_{DDM-D}	VDD Hold-Up Mode Depart Level			8		V
V_{DD-L}	VDD in Latch Mode			9		V
I_{ST}	Start-Up Current			150	200	µA
I_{DD-OP}	Operation Current	V_{DD} = 15V, Controller On, C_L = 1nF		3.5	4	mA
$I_{DD-SKIP}$	Skip Mode Operation Current	V_{DD} = 9V, FB < 1V		350	450	µA
I_{DD-F}	Fault Mode Operation Current		150	250	350	µA
FREQUENCY						
F_{OSC}	General Continuous Operation Frequency		61	65	69	kHz
		For AOZ7501H	122	130	138	kHz
F_{MIN}	Minimum Continuous Operation Frequency		17	20	23	kHz
F_{SSCG}	Spread Spectrum Clock Generator			±6		%
D_{MAX}	Minimum Duty Cycle			75		%

Electrical Characteristics *(Continued)*

T_A = -25°C to 85°C, V_{CC} = 15V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FB						
Z_{FB}	FB Pin Impedance		36	40	44	kΩ
$V_{FB-OPEN}$	FB Pin Pull-Up Voltage	FB Pin Open		4.4		V
G_{FC}	Gain-to-CS			0.5		V/V
V_{FB-E}	Entry FR Threshold Voltage			2.1		V
V_{FB-D}	Depart FR Threshold Voltage			1.8		V
V_{SK-E}	Skip Mode Entry Level			0.7		V
V_{SK-D}	Skip Mode Depart Level			0.82		V
GATE DRIVE						
T_{RISE}	Rising Time	V_{DD} = 15V, C_L = 1nF		120		ns
T_{FALL}	Falling Time	V_{DD} = 15V, C_L = 1nF		80		ns
T_{RISE}	Rising Time	V_{DD} = 7V, C_L = 1nF		120		ns
T_{FALL}	Falling Time	V_{DD} = 7V, C_L = 1nF		80		ns
$V_{G-CLAMP}$	Gate Clamping Voltage	V_{DD} = 15V		12	13	V
DMAG						
V_{CLAMP}	Minimum Clamp Voltage		0.7	1	1.3	V
T_{MIN}	Minimum On Time	Sourcing = 180µA(2)		3		µs
		Sourcing = 750µA(2)		0.8		µs
$T_{MIN-MAX}$	Maximum T_{MIN} Clamp	Sourcing = 100µA(2)		3.2		µs
$T_{MIN-MIN}$	Minimum T_{MIN} Clamp	Sourcing = 900µA(2)		0.7		µs
$I_{D-SOURCE}$	Maximum Sourcing Current		1			mA
V_{D-OVP}	DMAG Over-Voltage Protection		2.9	3	3.1	V
T_{D-OVP}	V_{D-OVP} De-Bounce Time	5 Clock Cycles, for AOZ7501H		30	40	µs
		5 Clock Cycles		60	100	µs
V_{DIS}	Disable Protection		0.25	0.3	0.35	V
T_{DIS}	Disable De-Bounce Time			30	40	µs
SOFT-START						
T_{SS}	Soft-Start Time			4		ms
$F_{SS-SKIP}$	Soft-Start Skip Frequency	V_{CS} > 1V, for AOZ7501H		65		kHz
		V_{CS} > 1V		32.5		kHz
CURRENT SENSE						
V_{CL}	General Continuous Operation Limited Current Sense Level		0.85	0.9	0.95	V
T_{OLP}	Over Load Protection De-Bounce Time			60	80	ms
V_{CL2}	SSDS Level			1.5		V
T_{CL2}	De-Bounce Time for V_{CL2}	Continuous 5 Clock Cycles		75	100	µs
T_{LEB}	Leading Edge Blanking Time			250	400	ns
T_P	Propagation Delay Time			50	100	ns

Electrical Characteristics *(Continued)*

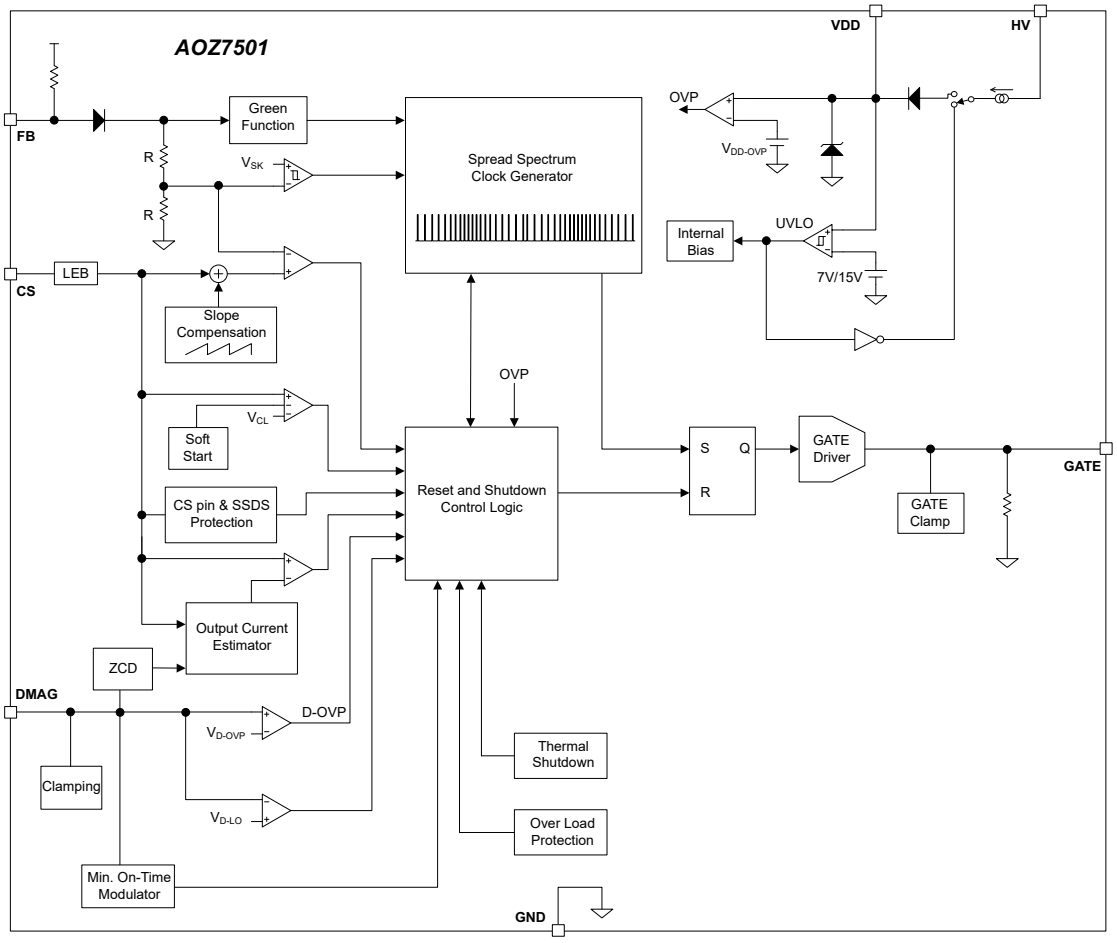
T_A = -25°C to 85°C, V_{CC} = 15V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OVER TEMPERATURE PROTECTION						
OTP	Internal Over Temperature Protection	T_J Rising		145		°C
OTP_{REC}	Thermal Shutdown Recovery Threshold	T_J Falling		125		°C

Note:

2. Guaranteed by design.

Functional Block Diagram



Typical Characteristics

Figure 1. Supply Current From HV Pin vs. Temperature

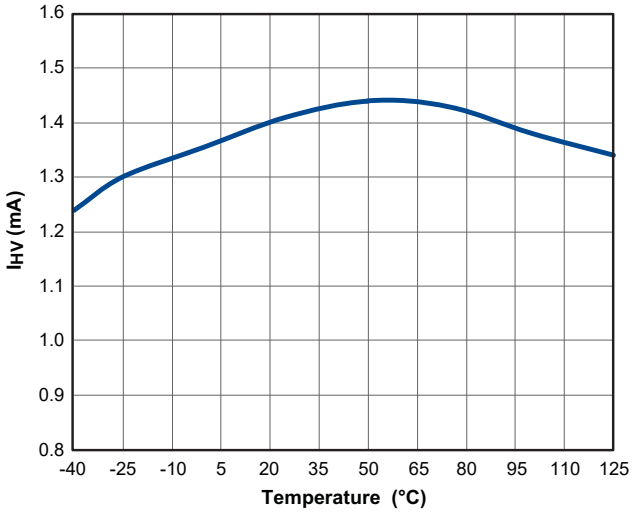


Figure 2. Turn-On Threshold Voltage vs. Temperature

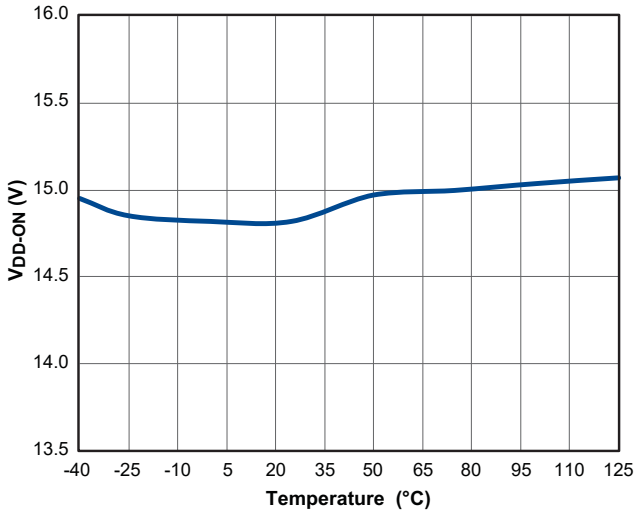


Figure 3. Operating Current vs. Temperature

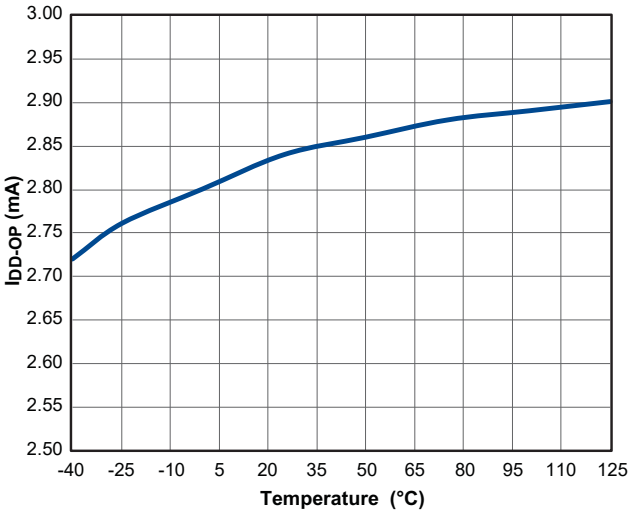


Figure 4. Under-Voltage Lockout Voltage vs. Temperature

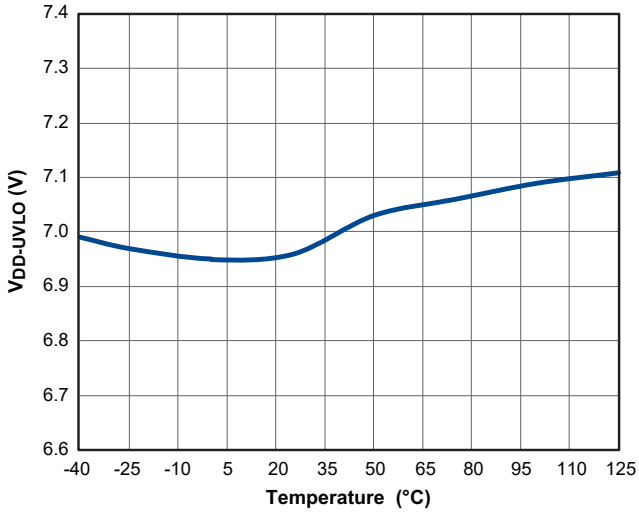


Figure 5. Gate Clamping Voltage vs. Temperature

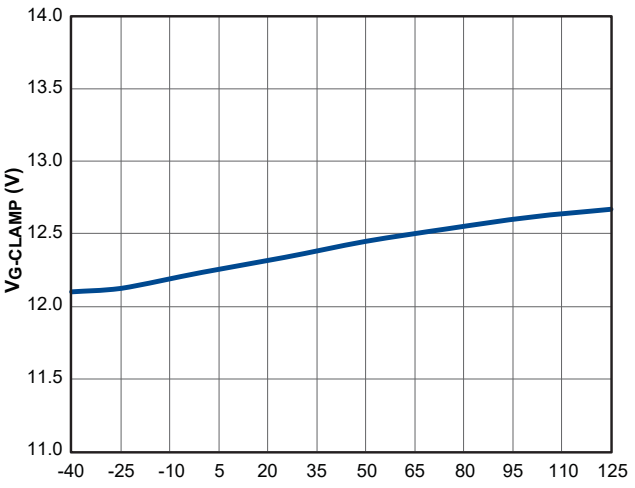
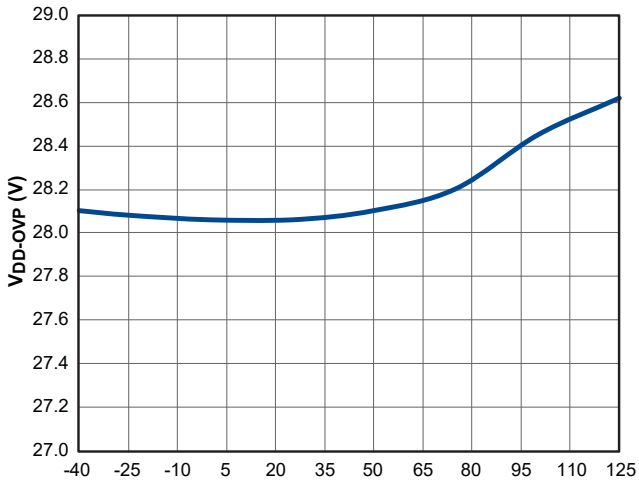


Figure 6. VDD OVP Level vs. Temperature



Typical Characteristics *(Continued)*

Figure 7. Skip Mode Entry Level vs. Temperature

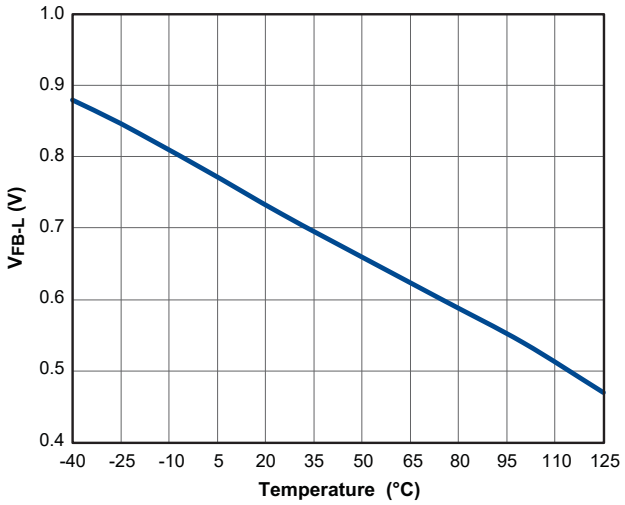


Figure 8. Skip Mode Depart Level vs. Temperature

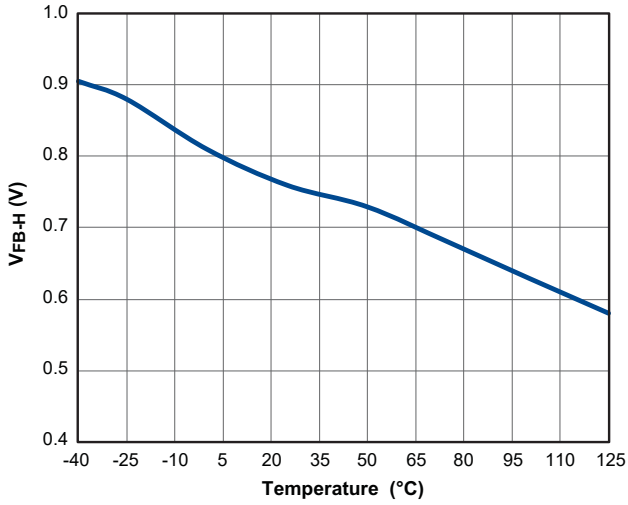


Figure 9. Maximum T_{MIN} Clamp vs. Temperature

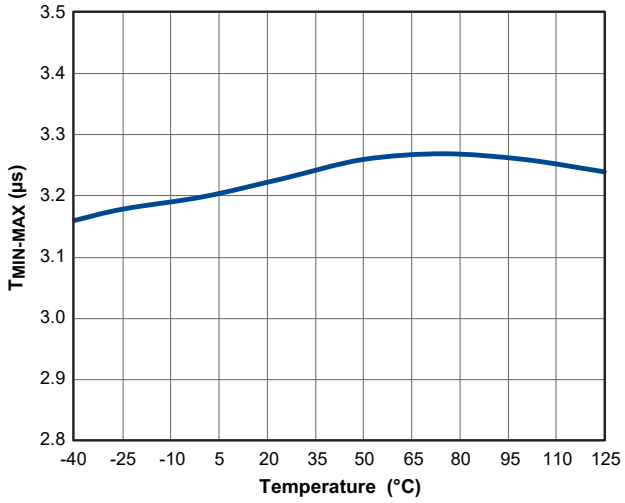


Figure 10. Minimum T_{MIN} CLAMP vs. Temperature

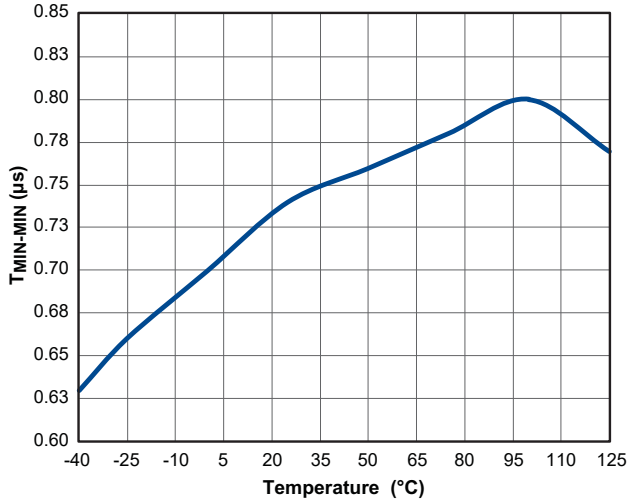


Figure 11. General Continuous Operation Frequency vs. Temperature

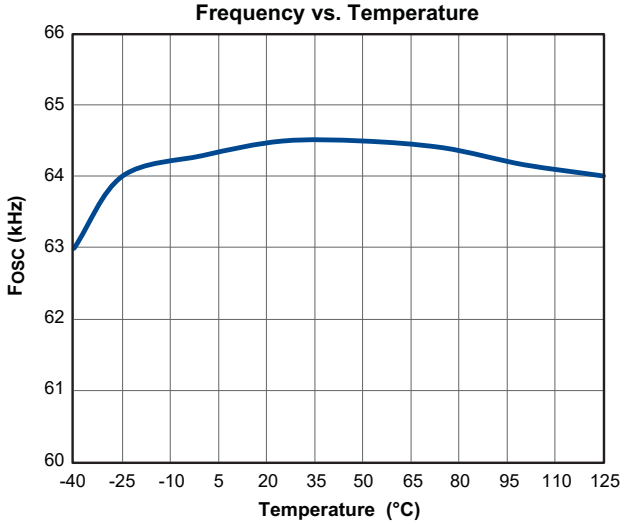
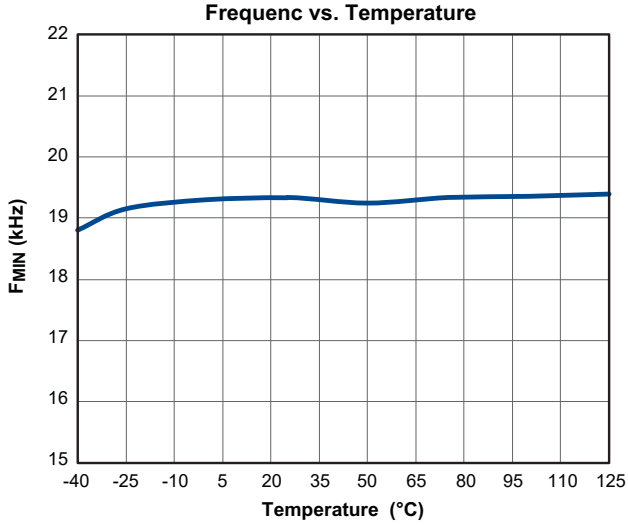


Figure 12. Minimum Continuous Operation Frequenc vs. Temperature



Typical Characteristics *(Continued)*

Figure 13. Maximum Duty Cycle vs. Temperature

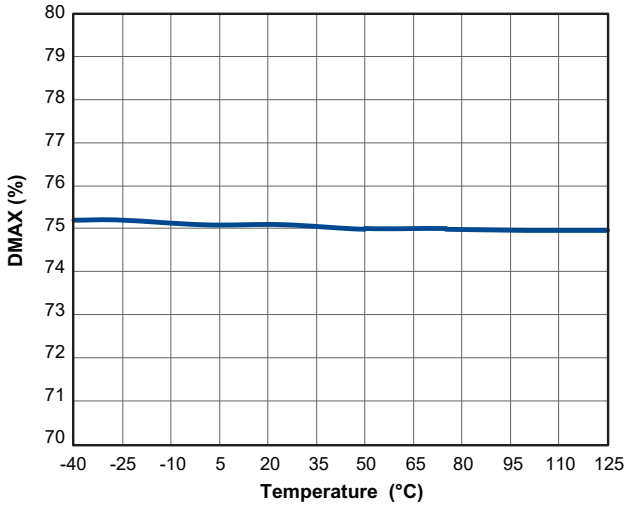


Figure 14. Current Limit vs. Temperature

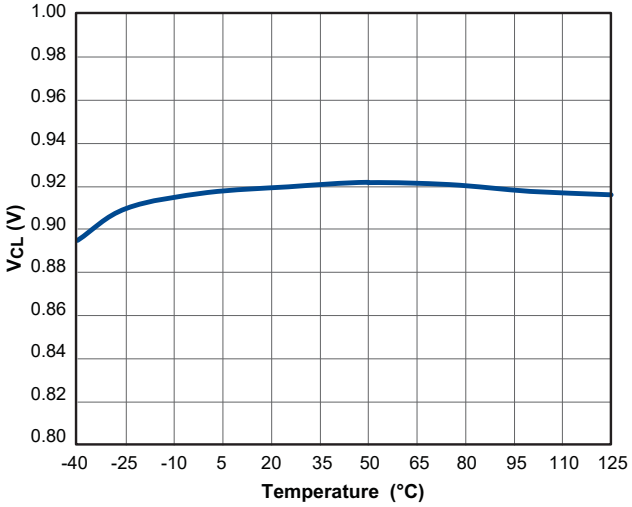


Figure 15. DMAG Pin Over Voltage Level vs. Temperature

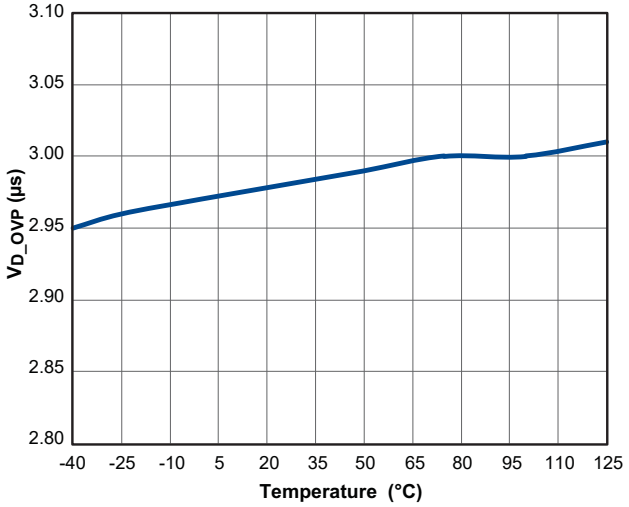


Figure 16. DMAG Sourcing Current 0.5mA vs. Temperature

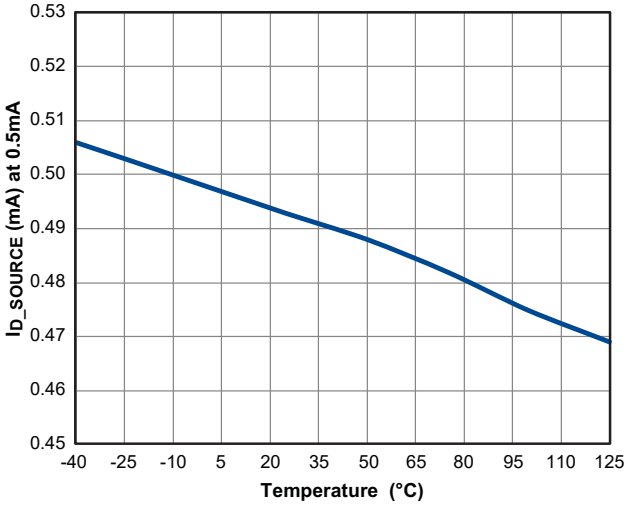
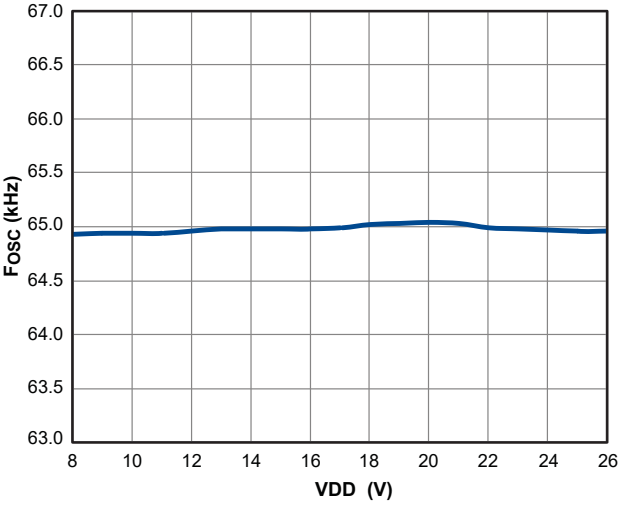


Figure 17. General Continuous Operation Frequency vs. VDD



Typical Operation Description

Start-Up

During the start-up period, the HV device acts as a current source and charges the VDD capacitor until its voltage is higher than the turn-on threshold V_{DD-ON}, PWM signal will start to drive the MOSFET and the peak current of MOSFET will be increased linearly during the soft-start period.

Normal Mode Operation

In normal mode operation, if the output is in heavy load, the controller is switching with maximum frequency (130kHz or 65kHz) and operated with current-mode control.

Frequency Foldback Mode Operation

AOZ7501 provides green mode operation to reduce switching loss and improve system efficiency by frequency foldback function during light load condition. When the voltage of FB pin is decreased below V_{FB-E}. The controller will enter green mode and the switching frequency starts foldback according to load condition. The minimum switching frequency will be clamped to F_{MIN} when the voltage of FB pin is below V_{FB-D}.

Skipping Mode Operation

Under very light load condition, the voltage of FB will be decreased to a very low level. When the voltage of FB is dropped below the threshold (V_{SK-E}) that is the hysteresis voltage of internal PWM comparator, the PWM signal will be blanked and stop to drive MOSFET. After the output voltage dropped and FB voltage increased higher than V_{SK-D}, the PWM signal will be resumed.

VDD Hold-Up Mode Operation

During load transient or ultra light load conditions, FB voltage will drop deeply and enter into skipping cycle mode to stop PWM signal. In some conditions, VDD voltage will drop below controller's turn-off threshold (UVLO) and then the system will be restarted. If another load occurred, the system cannot respond immediately and the output voltage will drop deeply. This mode is very useful to prevent system restarting during ultra light load condition and has a quick response for load transients. It doesn't require a two-stage VDD circuit to keep VDD voltage higher than UVLO.

Minimum On Time Modulation

In order to reduce switching loss and minimize acoustic noise, AOZ7501 provides Modulate On-Time to limit the minimum turn-on time ($T_{on,min}$). The modulate on-time is inversely proportional to input voltage. In the condition of low line input voltage, PWM on-time will be enlarged to reduce switching cycles and increase the efficiency of light load. In the condition of high line input voltage, PWM on time will be tighten to minimize acoustic noise and make the ripple of output voltage close in every line input.

Protection Features

Over Voltage Protection (OVP)

It's critical that over voltage protection (OVP) prevents the output voltage from exceeding the ratings of converter's components. The Over-Voltage Protection (OVP) is embedded by the information at the VDD pin. That information comes from the output voltage through the turn-ratio from auxiliary winding to secondary-side winding. When the voltage further rises and exceeds the comparator's reference voltage of static OVP (27.5V Typ), the OVP comparator will shut down the output PWM pulse. The OVP logic also includes 20μs de-glitch time for false triggering by noise.

DMAG Over Voltage Protection (DOVP)

AOZ7501 provides a more accurate OVP function from DMAG pin that is to protect system component when the output is over voltage. DMAG pin detect the voltage across the auxiliary winding during MOSFET turn-off period with another 1μs de-glitch time. The DMAG pin voltage is proportional to the output voltage. The DMAG OVP will be triggered when the DMAG voltage over 3V continuously with 5 PWM cycles. This DMAG OVP is more accurate and faster than the VDD OVP function. A bypass capacitance (15~100pF) in DMAG pin is needed to avoid false trigger DOVP and malfunction.

DMAG pin Pull Low Protection

AOZ7501 provides a useful protection function in DMAG pin, when DMAG pin is pulled low below 0.3V and continuous with two switching cycles. The pull low current must be larger than 2mA. AOZ7501 will trigger DMAG pin pull low protection to protect system for user defined protection applications.

Cycle-by-Cycle Current Limit

The cycle-by-cycle current-limit protection circuit detects the inductor current and protects power MOSFET by turning off the output driver each cycle when the CS voltage becomes larger than preset voltage level. The voltage across the current detection resistor R_{CS} connected to the GND is fed to the CS pin for current limit detection.

There are two levels for current limit. The slow one, reference voltage set point is V_{CL} = 0.9V. AOZ7501 offers 60ms de-bounce timer for counting to enter Over Load Protection (OLP) mode and the system will be auto-recovery. The fast one, reference voltage set point is V_{CL2} = 1.5V. This protection function will be triggered, if the fast one comparator is continuously triggered by five

times. This condition will be happened during transformer short or Secondary Side Diode Short (SSDS), and the circuit will induce large current in the primary-side.

Over Load Protection (OLP)

AOZ7501 provides Over Load Protection function to prevent the device of power supply system from operating with high stress. The OLP level was set by current sense resistor (R_{CS}) with the equation (1). OLP will be triggered when load condition is larger than preset level and continuous with 60ms (4096 clock cycles).

CS Pin Open Protection

The CS pin features open-loop protection to pass the CS pin single fault testing. When CS pin was opened, CS pin voltage will be pulled high by internal circuit. The pull high voltage was higher than V_{CL2} = 1.5V, such that SSDS protection will be triggered to protect system.

CS Pin Short Protection

CS pin features short to GND protection to pass the CS pin single fault testing. When CS pin is shorted to GND, it means the CS pin voltage is zero. When CS pin voltage is lower than 80mV with modulate minimum on-time and continuous triggered with 5 cycles, the CS pin short protection will be triggered to protect the power supply system. The detection duration are different between high line input voltage and low line input voltage to protect the component in high line input and detect precisely in low line input voltage.

Thermal Shutdown

AOZ7501 provides internal thermal shutdown protection for controller thermal run away. If the temperature of controller is higher than internal set point, the controller will stop PWM until the temperature cools down, below hysteresis of thermal shutdown set point.

Application Information

AOZ7501 is an advanced current mode control controller. Current mode control has many advantages than voltage mode control such as fast response time, simplified feedback loop compensation and cycle-by-cycle current sense. The duty cycle of AOZ7501 is limited by feedback voltage primary-side peak current of flyback converter's main switch. And there is slope compensation circuit which is designed to prevent sub-harmonic oscillation whenever duty cycle is larger than 50% application.

In order to achieve high efficiency and high performance under light load and no load conditions, AOZ7501 provides fix frequency mode, frequency fold-back mode, frequency skipping mode, and minimum on-time ($T_{on,min}$) modulation functions. AOZ7501 also provides VDD hold-up mode to prevent supply voltage drop to UVLO during load transient operation without any extra component.

AOZ7501 has many protection functions, such as VDD Over Voltage Protection (OVP), DMAG pin Over Voltage Protection (DOVP), DMAG pin Pull Low Protection (DPLP). Internal Over Temperature Protection (OTP), Secondary Side Diode Short protection (SSDS), CS pin Open/Short Protection, Over Load Protection (OLP).

High Voltage (HV) Start-Up

A high voltage device is designed as a current source for the controller during the start-up. It doesn't need any external circuit for start-up. This current source will be turned-off after the AOZ7501 is powered on. The start-up waveform of VDD is shown as Figure 18 and HV start-up application circuit is shown as Figure 19.

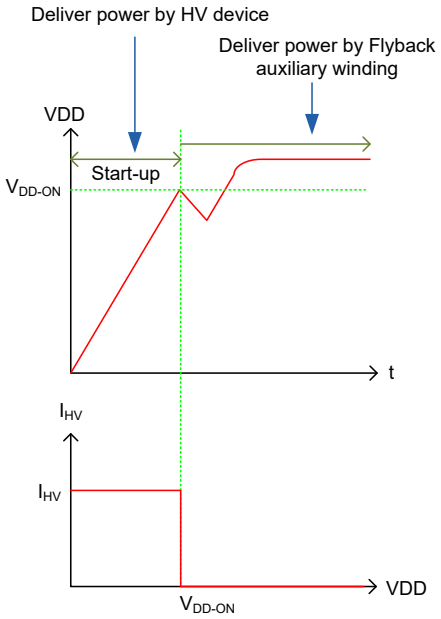


Figure 18. VDD Start-Up Waveform

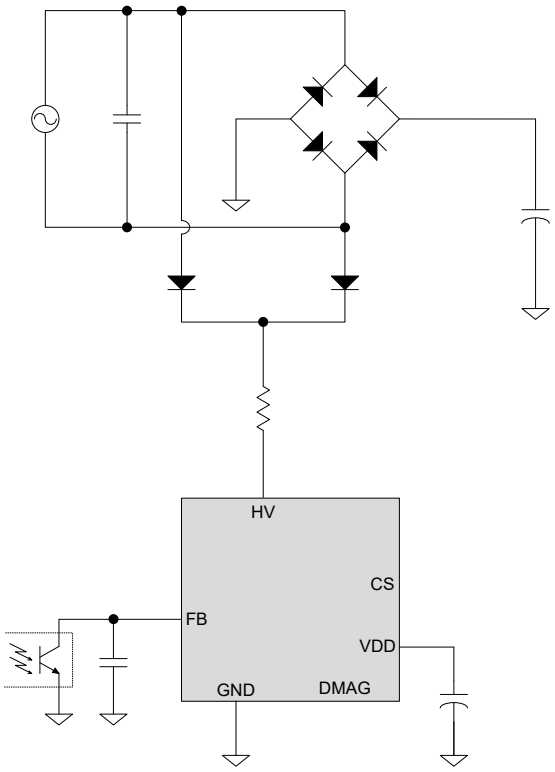


Figure 19. HV Start-Up Application Circuit

VDD

VDD pin is the power supply pin, the controller is turn on by HV start-up current source. After HV startup, the VDD power is supplied by system's auxiliary power. VDD pin also provides over voltage protection functions with 20μs de-glitch time, when VDD voltage is higher than 27.5V (Typ) and keeping 20μs, the VDD OVP will be triggered.

Under Voltage Lock Out (UVLO)

UVLO function is used to prevent controller malfunction when VDD supply voltage drops. When VDD supply voltage reaches 15V (Typ), internal blocks of the IC are enabled and start to operate. When VDD supply voltage drops below 7V (Typ), most of the internal circuits are disabled to reduce the current consumption. The related threshold of VDD pin is shown as Figure 20.

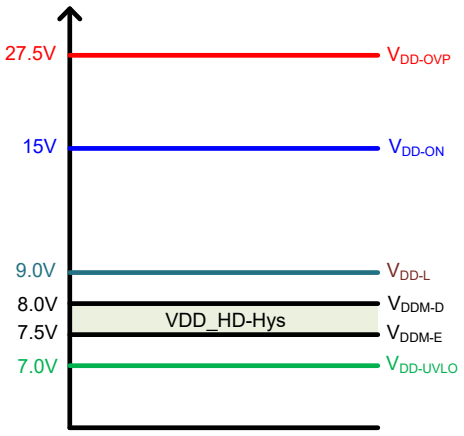


Figure 20. Related Threshold of VDD

VDD Hold-Up Mode

VDD pin also provides VDD hold-up mode to prevent VDD drop below UVLO in every light load or no load conditions. The purpose of VDD hold-up mode is to keep VDD voltage, and prevent VDD to drop below UVLO. VDD hold-up mode at load transient is shown as Figure 21. It's not recommended to design VDD hold-up mode operation in light load or no load conditions. It will increase power consumption in no load condition and output voltage will increase when VDD hold-up mode operation is in light load or no load conditions.

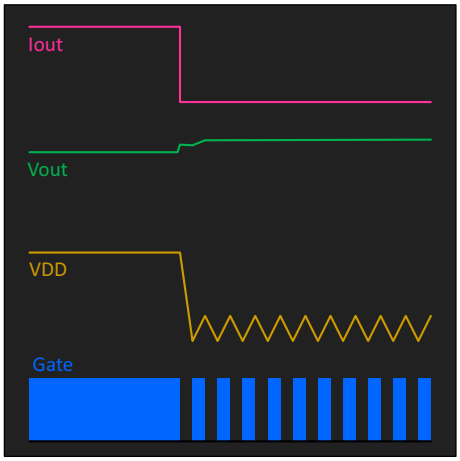


Figure 21. VDD Hold-Up Mode

Soft-Start (SS)

To minimize the inrush current and components stress in the period of start-up time. There is a built-in 4ms timing soft-start circuit in AOZ7501 to minimize the stress of power components during the star-up period.

Leading Edge Blanking (LEB)

A 250ns (Typ) LEB is applied in the current sense pin to prevent false trigger by initial spike of MOSFET turn-on current. The minimum on-time is almost equal to propagation delay time plus LEB time. (T_p+T_{LEB}). During the period of minimum on-time, all of current sense protection functions are masked and PWM cannot be switched off.

Negative voltage (<-0.3V) on each pin will cause substrate injection into AOZ7501. This can induce damage of controller or false trigger event, as shown in Figure 22. It's highly recommended to add a R-C filter to reduce the initial spike and negative voltage on CS pin.

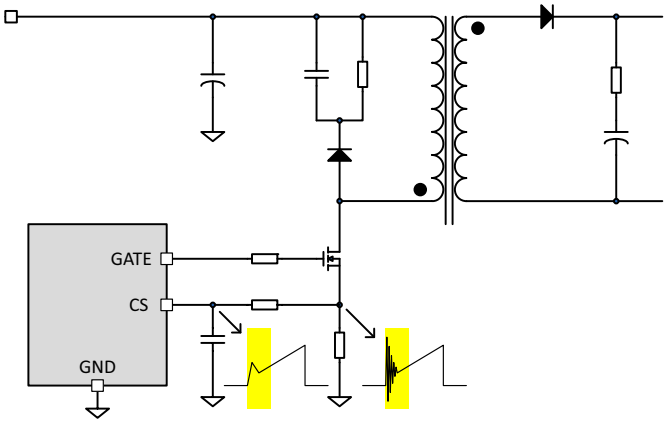


Figure 22. Current Sense Waveform With Spike and Negative Voltage

Current Sense

AOZ7501 is a current-mode controlled PWM controller. The Current Sense pin (CS) is used to sense the peak current of primary-side MOSFET, and make the current loop close. There is a 0.9V limit for cyrcle-by-cyrcle current limit purpose. The current sense resistor can be set by using equation (1):

$$0.27 \times \frac{N_{PRI}}{I_{O(MAX)} \times N_{SEC}}$$

Oscillator

The oscillator frequency of AOZ7501 is 65kHz (130kHz is option), which is designed with Spread Spectrum Clock Generator (SSCG) for spreading the energy around the 65kHz (130kHz) to pass the EMI requirement, as shown in Figure 23. The SSCG spread range is ±6% and SSCG period is 16ms. It also generates a saw tooth waveform for slope compensation that is used to release stability issue of current-mode control.

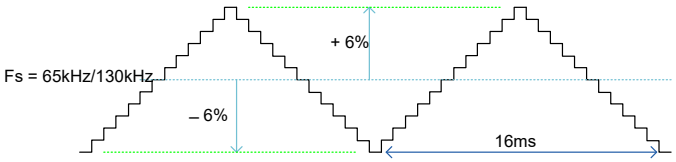


Figure 23. Spread Spectrum Clock Generator (SSCG)

Frequency Foldback and Skip Modes

In order to improve system efficiency, there are frequency foldback and skip modes for light load operation, as shown in Figure 24. The switching frequency will be reduced according to load conditions, from 65kHz (130kHz) to 20 kHz. For extra low load conditions, AOZ7501 provides skip mode which can skip cycles to reduce power consumption improve light load efficiency.

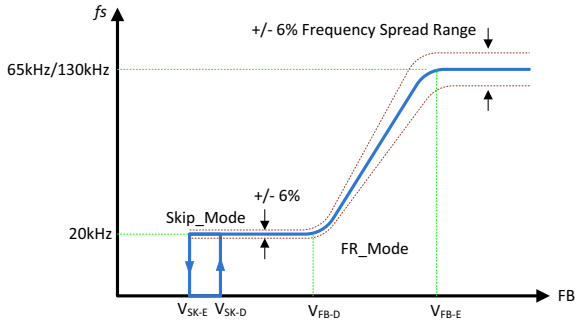


Figure 24. Frequency Reduction Mode and Skip Mode

Feedback

The Feedback (FB) pin is used for voltage feedback looping. The feedback signal is provided from the secondary-side shunt regulator (TL431) and transfer through the opto-coupler to FB pin of AOZ7501. There is a pull high resistor which is built-in the AOZ7501, as shown in Figure 25. The gain to PWM comparator is 0.5V/V, and with one diode offset. The gain of feedback loop will be decreased due to the large pull high resistor. The design of the feedback compensation circuit should be given extra attention.

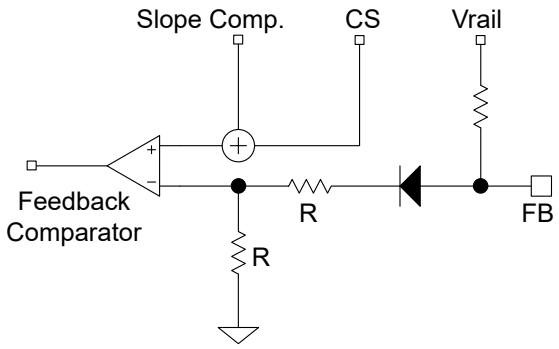


Figure 25. Feedback Pin Internal Behavior Circuit

DMAG

The DMAG pin is used to detect the transformer demagnetize time, output voltage signal and input voltage information. AOZ7501 features T_{on} minimum ($T_{on,min}$) modulation function to reduce the switching loss under light load condition. $T_{on,min}$ can be modulated by different sinking current from DMAG pin. In case of high line input voltage, the sinking current is large and $T_{on,min}$ will be small. When the input voltage is low, the sinking current is lower and $T_{on,min}$ will be larger. AOZ7501 also features DMAG pin over voltage protection function, when the voltage of DMAG pin is higher than 3V with 5 cycles de-glitch time, the DMAG OVP will be issued.

In normal operation, DMAG low voltage will be clamped on 1.0V. DMAG pull low function is available. If DMAG pin voltage forced to lower than 0.3V and continues with 30μs, DMAG pull low protection will be triggered. A by pass capacitor is needed in parallel to DMAG pin to prevent protection functions false trigger or cause malfunction. The by pass capacitance must be larger than 15pF.

Alpha and Omega Semiconductor provides an EXCEL based design tool, an application note and a demonstration board to help the design of AOZ7501 and reduce the R&D cycle time. All the tools can be download from: www.aosmd.com.

PCB Layout Guide

A good PCB layout can minimize EMI and reduce unknown noise, which is helpful during ESD or lighting surge tests. The followings are good PCB layout guideline for an AC/DC adaptor:

1. Bridge rectifier output should directly connect to C_{BULK} first, and use a neck layout to ensure the current flows into C_{BULK} to get better EMI and reduce line frequency ripple.
2. Loop (a), C_{BULK} ⟶ Transformer ⟶ MOSFET ⟶ R_{CS} ⟶ C_{BULK} (2), this loop is a high frequency and high current loop. The trace return to C_{BULK} should be kept as short as possible and directly connect to C_{BULK} ground.
3. Loop (b), the primary-side RCD snubber acts as a high frequency noise tank, it should be kept far away from the controller. The loop should be as short as possible.
4. Loop (c), the secondary-side snubber is a high frequency switching noise, too. The loop should be kept as short as possible.
5. The VDD decoupling capacitor C_{VDD} needs to be placed close to IC, VDD and GND pin as much as possible.
6. Loop (d), the drive loop is also a high frequency loop. The loop must be short to decrease noise coupling and prevent unnecessary interference.
7. Switching current sense (CS pin) is very important for a stable operation. Normally, a RC filter is recommended to reduce the noise applied to the CS pin.
8. If there's a heat sink for the MOSFET, it should be connected to ground.
9. All ground for controller (4, 5, 6, 7, 8, 9, 10) should connect together first and then use a trace connect to C_{BULK} ground (2) by a neck layout.
10. Loop (e), auxiliary power loop still needs to be kept short. C_{VDD} should be placed close to the controller. This one also needs to use a trace to directly connect to C_{BULK} ground (2) by neck layout.
11. Primary-side ground of Y-Cap (11), it needs to use a trace to directly connect to C_{BULK} ground (2) by neck layout.

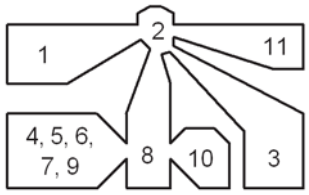


Figure 26. Ground Group of Layout Recommended

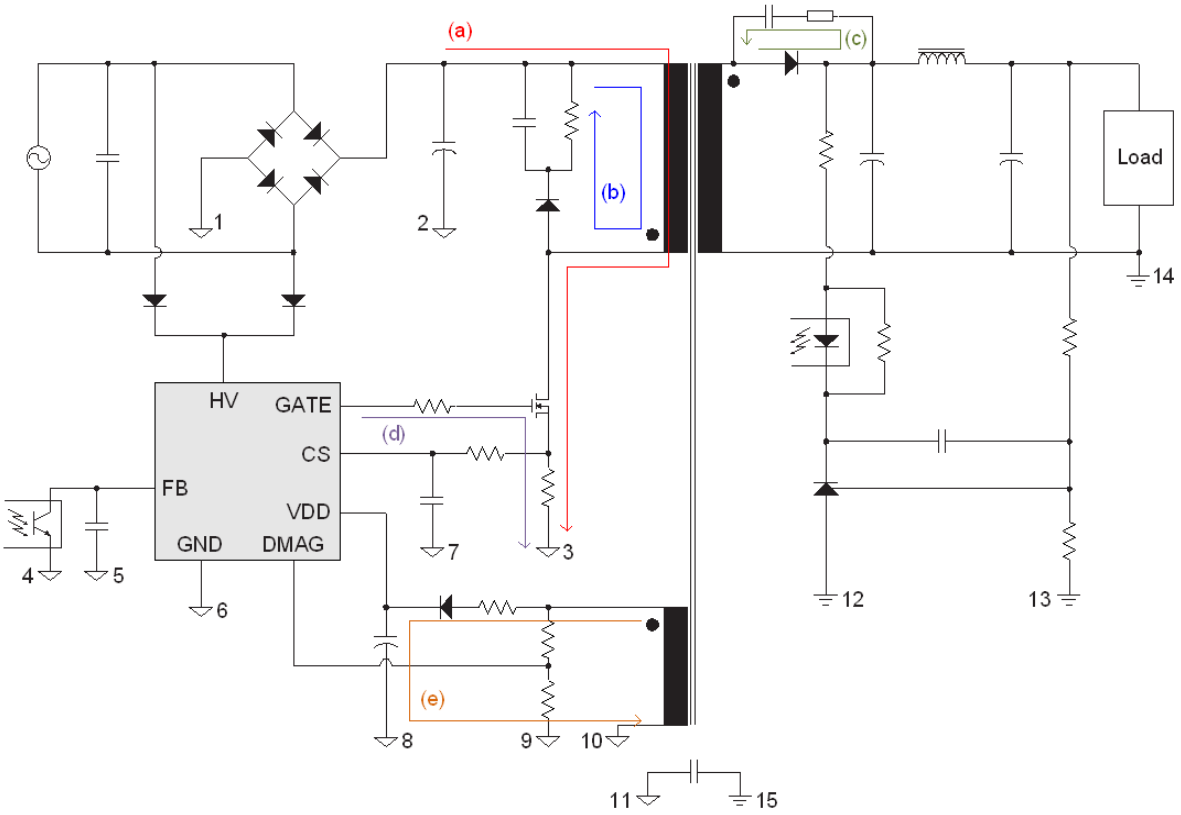


Figure 27. Main Loops for PCB Layout Considerations

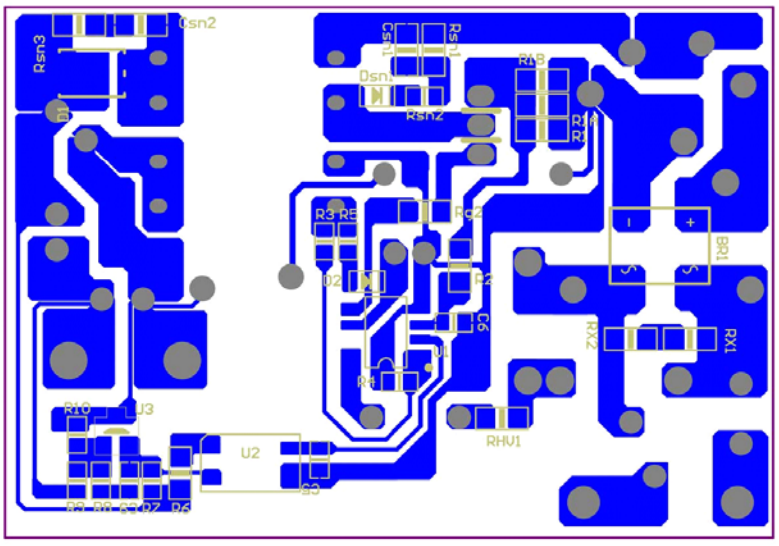
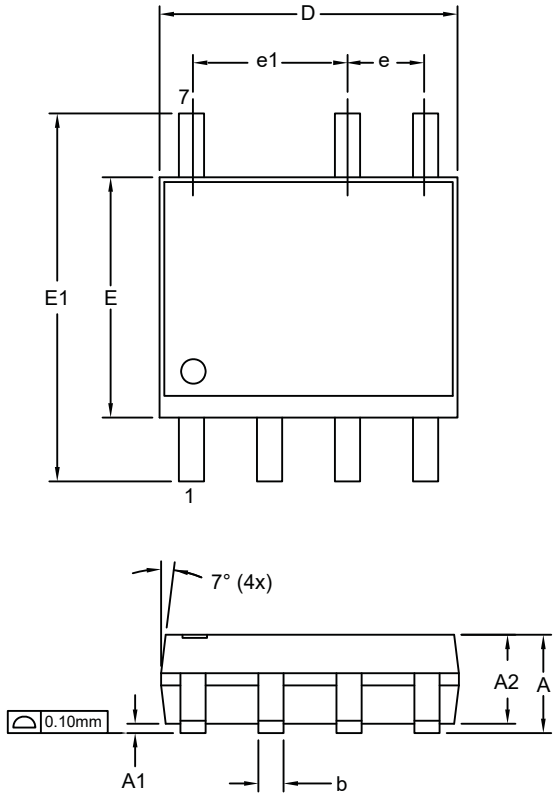
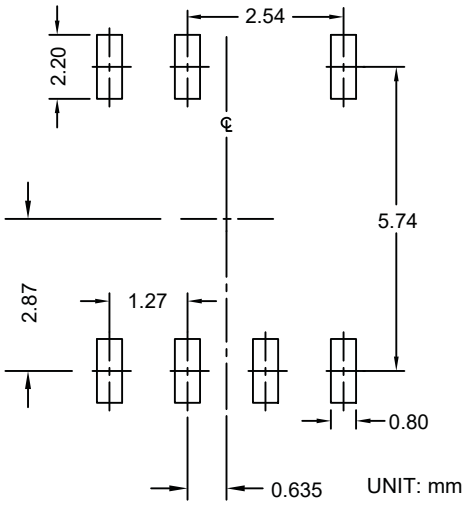


Figure 28. Recommended PCB Layout

Package Dimensions, SO-7L



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
e1	2.54 BSC		
E1	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

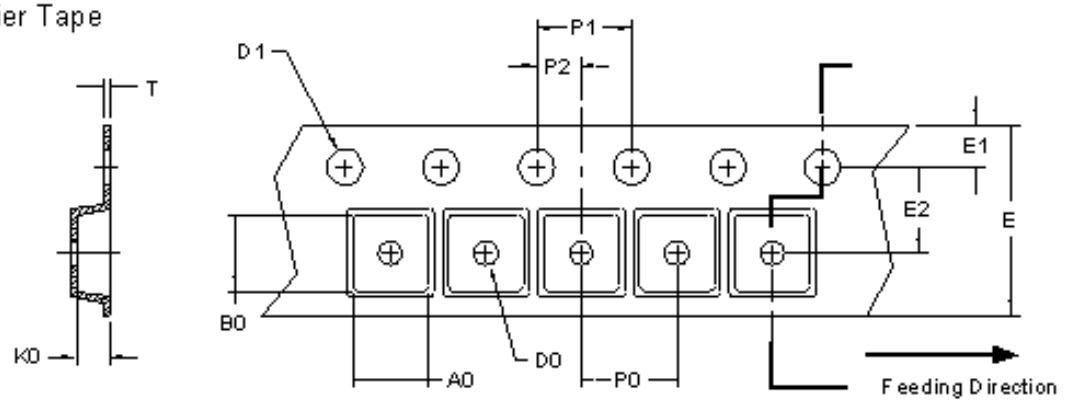
Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E	0.150	0.154	0.157
e	0.050 BSC		
e1	0.100 BSC		
E1	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating.
3. Package body size exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils each.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SO-7L

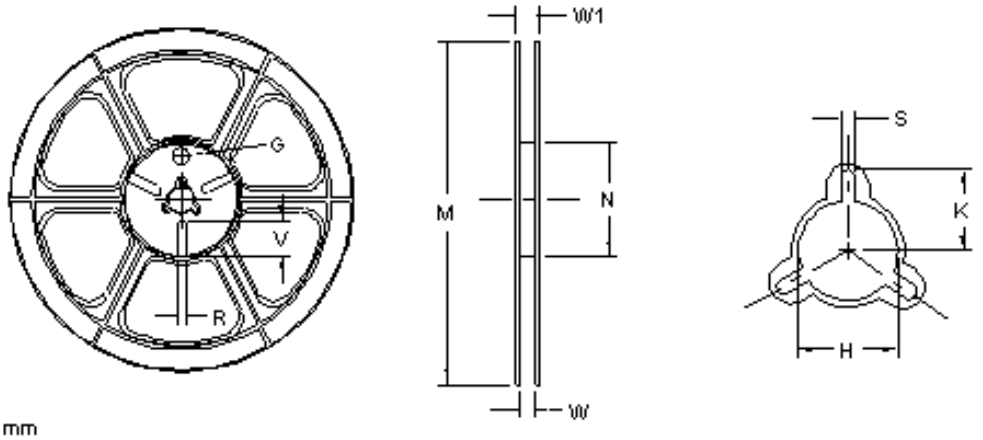
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-7 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.25 ±0.05

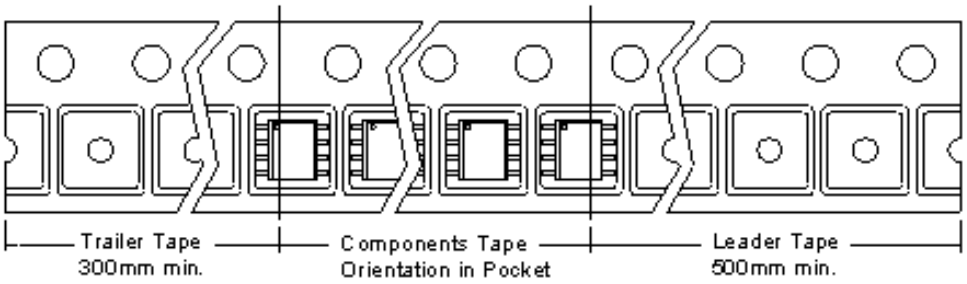
Reel



UNIT: mm

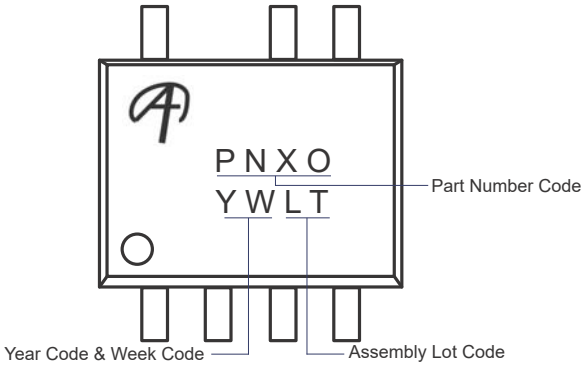
Tape Size	Reel Size	M	N	W	W	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	117.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

Leader/Trailer and Orientation



Part Marking

AOZ7501XAI
(SO-7)



Part Number	Description	Code
AOZ7501GAI	Green Product	AAG0
AOZ7501LAI	Green Product	AAL0
AOZ7501AAI	Green Product	AAA0
AOZ7501RAI	Green Product	AAR0
AOZ7501HAI	Green Product	AAH0