

## General Description

The AOZ9551QV is an integrated half-bridge gate driver with smart functions. The device includes one half-bridge gate driver, capable of driving high-side and low-side N-channel MOSFETs. Using two AOZ9551QV for single phase motor drivers and three AOZ9551QV for three phase motor drivers.

The device features multiple protection functions such as short circuit protection and over temperature protection. Moreover, AOZ9551QV provides adjustable gate drive sink and source current control. By doing this control, the user can optimize performances of EMI and efficiency.

The AOZ9551QV is available in a 5mm×5mm QFN-31L package and is rated over a -40°C to +125°C ambient temperature range.

## Features

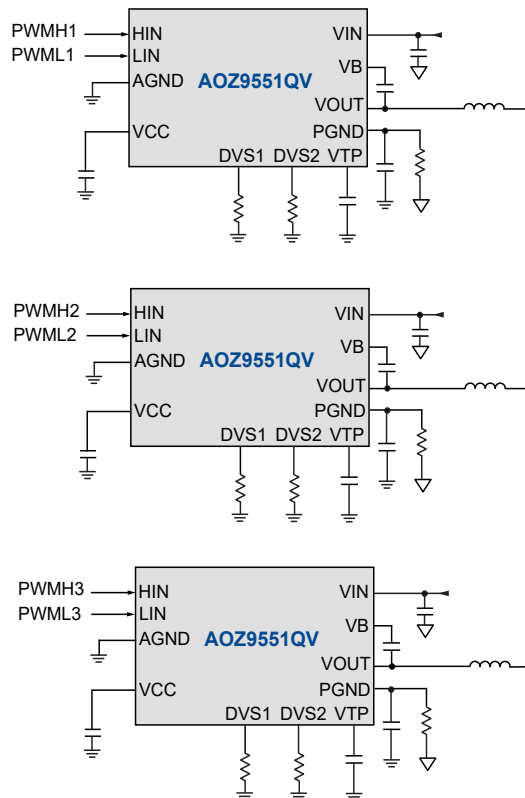
- Input voltage range:
  - 10.8V to 56 V
- Maximum Output Current 12A
- Adjustable Gate Drive Sink/Source Current
- Junction Temperature Monitor
- Integrated Bootstrap Diode
- Low  $R_{DS(ON)}$  internal NFETs
  - 10mΩ for Both HS/LS
- Thermal Protection
- Short Circuit Protection
- Thermally enhanced 31-pin 5×5 QFN

## Applications

- BLDC Motor Drive
- Fans and Pumps
- Power Tools



## Typical Application (Three Phases)



## Ordering Information

Part Number	Temperature Range	Package	Environmental
AOZ9551QV	-40 °C to +125 °C	QFN5x5-31L	Green



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit [www.aosmd.com/media/AOSGreenPolicy.pdf](http://www.aosmd.com/media/AOSGreenPolicy.pdf) for additional information.

## Pin Configuration

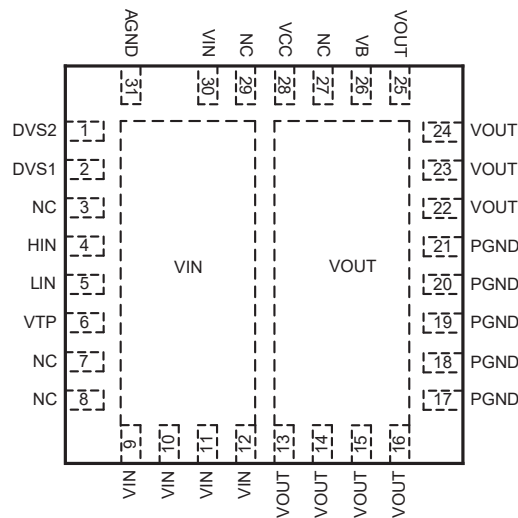


Figure 1. AOZ9551QV  
QFN5x5-31L

## Pin Description

Pin Number	Pin Name	Pin Function
1	DVS2	Adjustable gate drive sink current.
2	DVS1	Adjustable gate drive source current.
4	HIN	PWM input for high-side MOSFET.
5	LIN	PWM input for low-side MOSFET.
6	VTP	Junction temperature monitor and SCP indicator.
3, 7, 8, 27, 29	NC	NC
9, 10, 11, 12, 30	VIN	Supply input. All VIN pins must be connected together.
13, 14, 15, 16, 22, 23, 24, 25	VOUT	Motor drive output.
17, 18, 19, 20, 21	PGND	Power ground.
26	VB	Bootstrap capacitor connection. Connect an external capacitor between VB and VOUT for supplying high-side MOSFET.
28	VCC	Supply input for analog functions. Bypass VCC to AGND with a 1 μF~10 μF ceramic capacitor and as close to VCC pin as possible.
31	AGND	Analog ground.

## Absolute Maximum Ratings<sup>(1)</sup>

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VIN to AGND	-0.3V to 60V
VOUT to AGND	-0.3V to 60V
VB to AGND	-0.3V to 67V
DVS1, DVS2, VCC to AGND	-0.3V to 13.2V
HIN, LIN to AGND	-0.3V to 5.5V
PGND to AGND <sup>(3)</sup>	-0.3V to 1V
Junction Temperature (T <sub>J</sub> )	+150°C
Storage Temperature (T <sub>S</sub> )	-65°C to +150°C
ESD Rating	2 kV

### Notes:

1. Exceeding the Absolute Maximum Ratings may damage the device.
2. The device is not guaranteed to operate beyond the Maximum Operating Ratings.
3. PGND to AGND transient (t<10.80ns) ---- -6.5V to 6.5V.

## Electrical Characteristics

T<sub>A</sub> = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC	VCC	VIN = 12V, HIN/LIN=0V	7.8	8	8.2	V
	Line Regulation	VIN = 12 V~24V, HIN/LIN=0V		0.1		%/V
I <sub>VCC_short</sub>	I <sub>VCC</sub> Short Current	VIN = 24V, HIN/LIN=0V, Monitor I <sub>VCC</sub>		1		mA
V <sub>UVLO_R</sub>	VCC UVLO Rising	VIN = 12V, VCC increase, Monitor DVS1 from low to high	7	7.5	8	V
V <sub>UVLO_F</sub>	VCC UVLO Falling	VIN = 12V, VCC decrease, Monitor DVS1 from high to low		5.1		V
VB <sub>UVLO_R</sub>	VB-VOUT UVLO Rising	VIN = 20V, VB-VOUT increase, HIN = high, Monitor VOUT from low to high	6.3	7.2	8	V
VB <sub>UVLO_F</sub>	VB-VOUT UVLO Falling	VIN = 20V, VB-VOUT decrease, HIN = high, Monitor VOUT from high to low	4.8	5.5	6	V
I <sub>VIN_ST</sub>	I <sub>VIN</sub> Standby Current	HIN/LIN = 0V, Monitor VIN Current		1.5		mA
I <sub>VB-VOUT_ST</sub>	I <sub>VB-VOUT</sub> Standby Current	VIN = 10.8V, HIN/LIN = 0V, VOUT = Floating, VB-VOUT = 10V, Monitor VB-VOUT Current		30		µA
V <sub>HIN_L</sub>	HIN/LIN Logic Low Voltage	VIN = 12V	0		1.2	V
V <sub>HIN_H</sub>	HIN/LIN Logic High Voltage	VIN = 12V	2.2		5.5	V
R <sub>HIN_IN</sub>	HIN/LIN Input Pull Low Impedance			280		kΩ

## Recommended Operating Conditions<sup>(2)</sup>

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

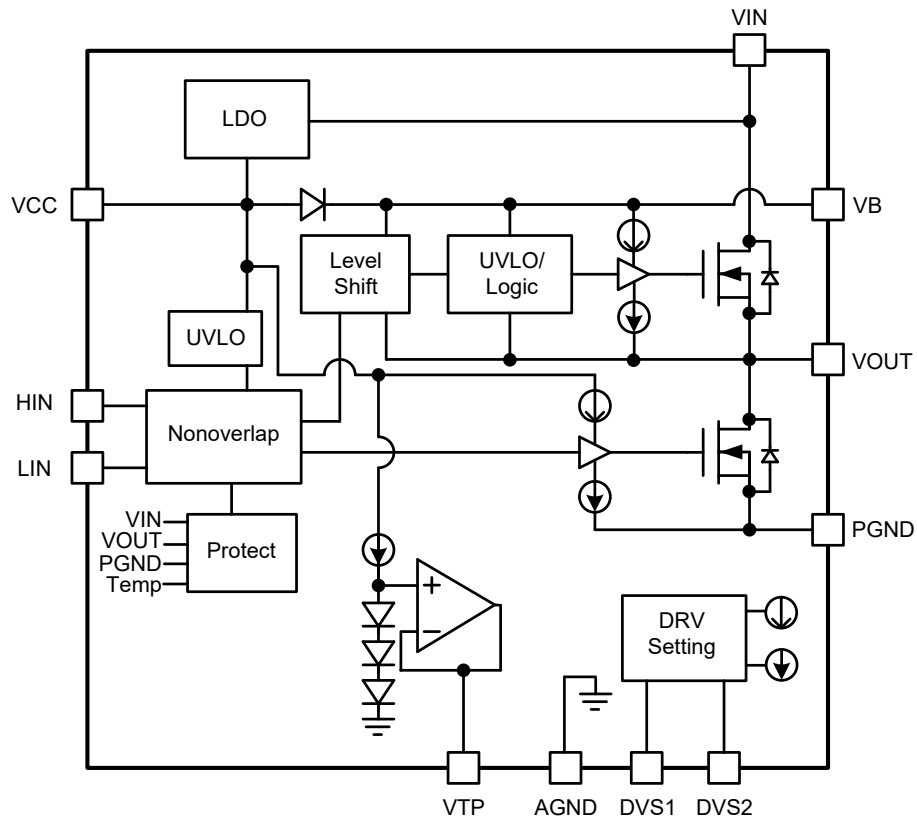
Parameter	Rating
Supply Voltage (V <sub>IN</sub> )	10.8V to 56V
Ambient Temperature (T <sub>A</sub> )	-40°C to +125°C
Package Thermal Resistance	30°C/W
Θ <sub>JA</sub>	3.8°C/W
Θ <sub>JC</sub>	

## Electrical Characteristics

T<sub>A</sub> = -40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>HIN_RP</sub>	HIN Rising Propagation Delay	VIN = 10.8V, DVS = 20kΩ, VOUT to GND = 100Ω, HIN = low to high, Monitor HIN high TH to 10% VOUT		45		ns
t <sub>HIN_FP</sub>	HIN Falling Propagation Delay	VIN = 10.8V, DVS = 20kΩ, VOUT to GND = 100Ω, HIN = high to low, Monitor HIN low TH to 90% VOUT		100		ns
t <sub>LIN_RP</sub>	LIN Rising Propagation Delay	VIN = 10.8V, DVS = 20kΩ, VOUT to VIN = 100Ω, LIN = low to high, Monitor LIN high TH to 90% VOUT		100		ns
t <sub>LIN_FP</sub>	LIN Falling Propagation Delay	VIN = 10.8V, DVS = 20kΩ, VOUT to VIN = 100Ω, LIN = high to low, Monitor LIN low TH to 10% VOUT		50		ns
T <sub>DM_R</sub>	Delay Matching Rising	Difference between t <sub>HIN_RP</sub> , t <sub>LIN_RP</sub>		55		ns
T <sub>DM_F</sub>	Delay Matching Falling	Difference between t <sub>HIN_FP</sub> , t <sub>LIN_FP</sub>		50		ns
V <sub>DVS</sub>	DVS	VIN = 12V, DVS to GND = 20kΩ	0.97	1	1.03	V
I <sub>DVS_MIN</sub>	DVS Min. Source Current	VIN = 12V, DVS = 4V		0.5		μA
I <sub>DVS_MAX</sub>	DVS Max. Source Current	VIN = 10.8V, DVS = 0.8V		140		μA
SR <sub>HIN_R</sub>	HIN Rising Slew Rate (DVS = 20kΩ)	VIN = 10.8V, VOUT to GND = 100Ω, HIN = low to high, Monitor VOUT Rising Slew Rate		1.78		V/ns
SR <sub>HIN_F</sub>	HIN Falling Slew Rate (DVS = 20kΩ)	VIN = 10.8V, VOUT to GND = 100Ω, HIN = high to low, Monitor VOUT Falling Slew Rate		0.025		V/ns
SR <sub>LIN_R</sub>	LIN Rising Slew Rate (DVS = 20kΩ)	VIN = 10.8V, VOUT to VIN = 100Ω, LIN = high to low, Monitor VOUT Rising Slew Rate		0.025		V/ns
SR <sub>LIN_F</sub>	LIN Falling Slew Rate (DVS = 20kΩ)	VIN = 10.8V, VOUT to VIN = 100Ω, LIN = low to high, Monitor VOUT Falling Slew Rate		1.07		V/ns
R <sub>H_ON</sub>	VIN-VOUT RON	VIN = 12V, HIN = 5V, VB-VOUT = 8V, IVOUT = 1A		10		mΩ
R <sub>L_ON</sub>	VOUT-PGND RON	VIN = 12V, LIN = 5V, PGND = 0, IVOUT = 1A		10		mΩ
V <sub>SD</sub>	Boost Diode Forward Voltage	Forward Current = 2mA		0.15		V
T <sub>OTP</sub>	Over Temperature Protection	VIN = 12V		150		°C
I <sub>SCP</sub>	Short Current Protection	VIN = 24V		45		A
V <sub>TP</sub>	V <sub>TP_25°C</sub>	VIN = 12V at 25°C	1.86	1.9	1.94	V
	V <sub>TP_125°C</sub>	VIN = 12V at 125°C	1.26	1.3	1.34	V

## Functional Block Diagram



## Detailed Description

The AOZ9551QV is an integrated half-bridge gate driver for motor drive applications. The device includes one half-bridge gate driver, capable of driving high-side and low-side N-channel MOSFETs. The AOZ9551QV provides adjustable source/sink current of both high/low-side gate drive output current which can optimize performances of EMI and efficiency on different PCB layout and applications.

In addition, the AOZ9551QV provides several fault protections, such as UVLO, SCP, OTP and non-overlapping mechanism.

The AOZ9551QV is available in 31-pin 5mm×5mm QFN package.

### Input Power Architecture

The AOZ9551QV integrates an internal linear regulator to generate 8V (±3%) VCC from input pins. If input voltage is lower than 5.8V, the linear regulator will be triggered VCC UVLO. The VCC maximum source current is 1mA. Therefore, extra external source is needed when operation switching frequency exceeds 30 kHz.

### Non-overlapping

For forbidding shoot-through, HIN or LIN is invalid when HIN or LIN goes high state before other one. For example, low-side gate state keeps low regardless of the state of LIN when HIN is high at first, and vice versa.

So when Shoot-through occurs, VOUT will follow the previous normal state, as illustrated Figure 2.

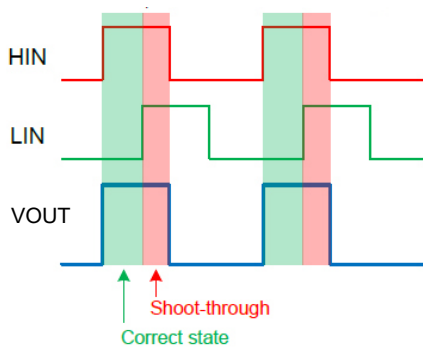


Figure 2. Shoot-through Behavior

## Fault Protection

### Short Current Protection (SCP)

In order to prevent the AOZ9551QV from being damaged during a short circuit, AOZ9551QV has built-in short current protection, and the relationship between the protection point and the input point voltage is shown in Figure 3.

If the current is greater than  $I_{SCP}$ , AOZ9551QV enters SCP, VTP pin will be pulled high, and then AOZ9551QV enters latch, VCC needs to be reset to return to normal operation state.

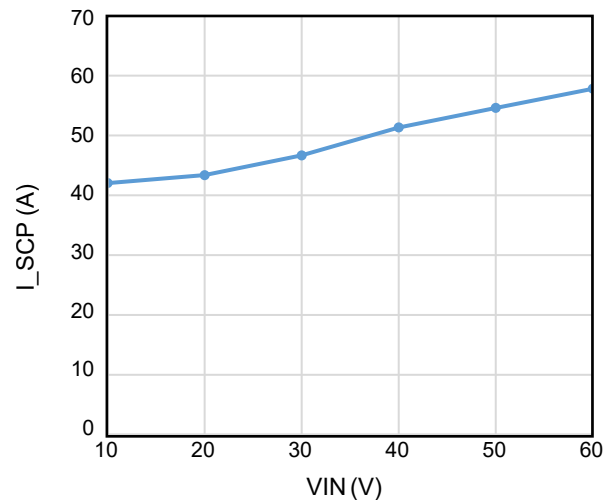


Figure 3. I<sub>SCP</sub> vs. VIN, Short Current Protection Curve

### Over Temperature Protection (OTP)

When the junction temperature reach 150°C, AOZ9551QV enters OTP, and release when the temperature drops to 120°C.

### Thermal Monitor

The junction temperature can be monitored by using internal current mirror pass through internal diodes. The related  $V_{TP}$  equation can be approximated as below:

$$V_{TP} = 1.9V - (\text{Temp} - 25^{\circ}\text{C}) \times 6\text{mV}$$

Please note that VTP is high when SCP is triggered.

### Adjustable Source/Sink Current

It's hard to meet all of EMI specifications in different applications. Therefore, AOZ9551QV provides external adjustable resistors for tuning gate drive source and sink current.

DSV1 and DVS2 are used to tune gate drive source and sink current, respectively. A resistor connects between each DVS pin and GND to setting gate drive source/sink current by internal current mirror, as illustrated Figure 4. Source and sink current use maximum capability to drive when DVS pins are floating or the voltage on DVS pins exceed 4V. The user can get the same source and sink capability by using DVS1 to design and DVS2 floating. The suggestion range of  $R_{DVS}$  is 20 kΩ ~ 100 kΩ.

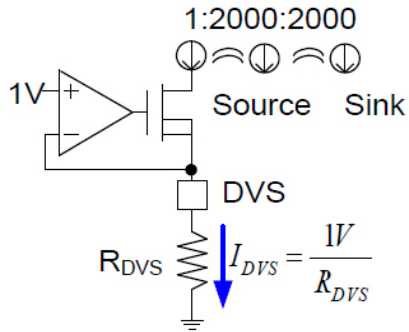


Figure 4. Source/Sink Current Setting

In addition, source and sink current controls are implemented only during MOSFET Miller effect and  $V_{GS} > 1V$ , as illustrated in Figure 5.

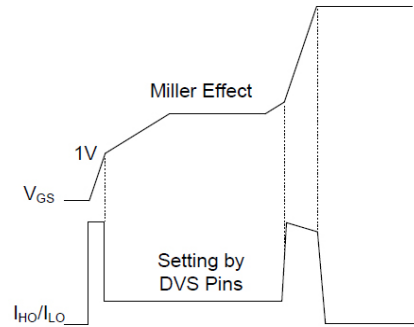


Figure 5. Source/Sink Current Implement Waveform

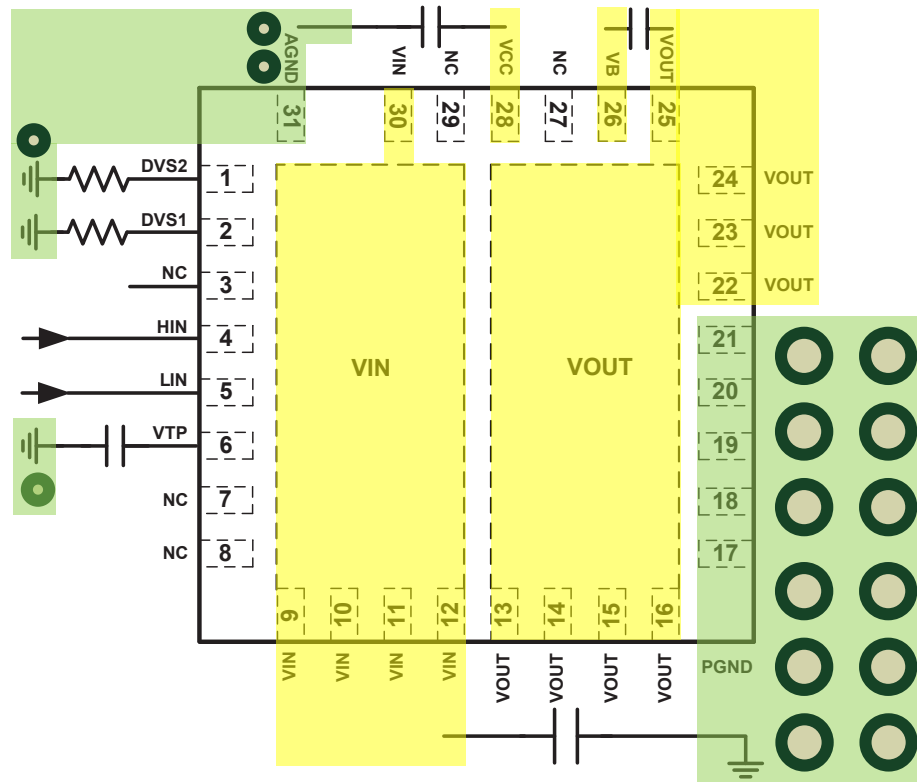
### Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

1. The VIN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to VIN pins to help thermal dissipation.
2. Input capacitors should be connected to the VIN pins and the PGND pins as close as possible to reduce the switching spikes.
3. The VOUT pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connected a large copper plane to VOUT pins to help thermal dissipation.

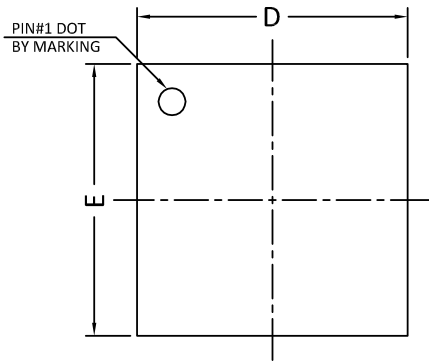
4. Decoupling capacitor CVCC should be connected to VCC and AGND as close as possible.
5. Bootstrap capacitor CB should be connected to VB and VOUT as close as possible.
6. A ground plane is preferred. PGND and AGND must be connected to the ground plane through vias.

Keep sensitive signal traces such as feedback trace and digital signals far away from the VOUT pins.

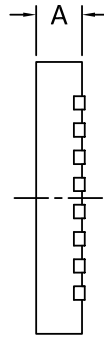




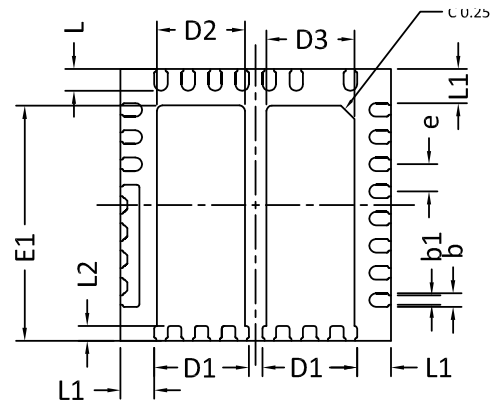
Package Dimensions, QFN5x5-31L



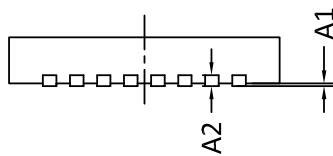
TOP VIEW



SIDE VIEW

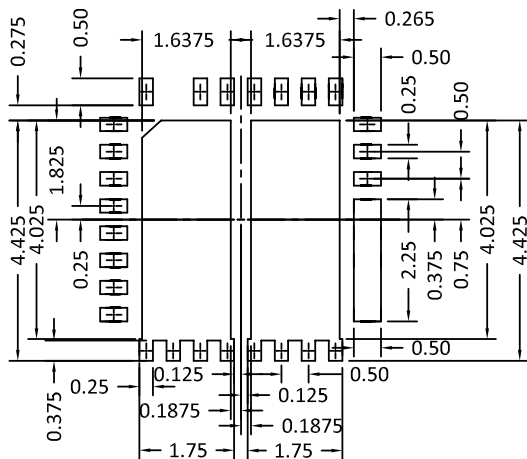


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



UNIT: mm

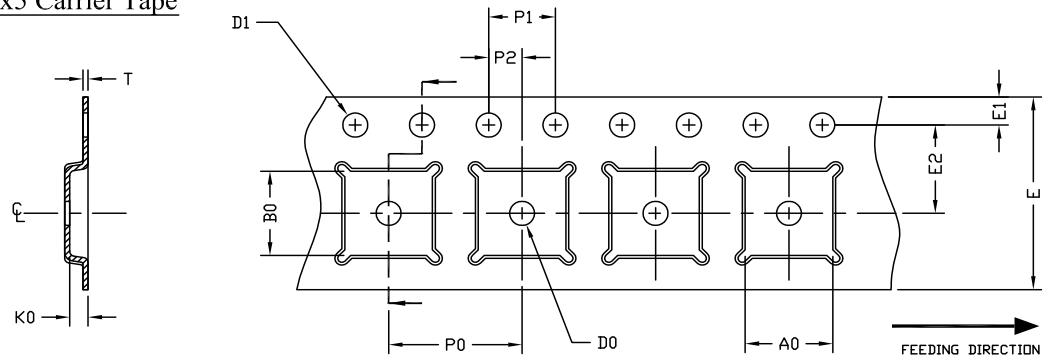
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	---	0.05	0.000	---	0.002
A2	0.2REF			0.008REF		
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	4.22	4.32	4.42	0.166	0.170	0.174
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	1.65	1.75	1.85	0.065	0.069	0.073
D2	1.53	1.63	1.73	0.060	0.064	0.068
D3	1.53	1.63	1.73	0.060	0.064	0.068
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.57	0.62	0.67	0.022	0.024	0.026
L2	0.225	0.275	0.325	0.009	0.011	0.013
b	0.20	0.25	0.30	0.008	0.010	0.012
e	0.50 BSC			0.020BSC		

NOTE:

1. CONTROLLING DIMENSION IS MILLIMETER.  
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. TOLERANCE :±0.05 UNLESS OTHERWISE SPECIFIED.
3. RADIUS ON ALL CORNER ARE 0.152 MAX, UNLESS OTHERWISE SPECIFIED.
4. PACKAGE WARPAGE: 0.012 MAX.
5. PAD PLANARITY: ±0.102.

### Tape and Reel Dimensions, QFN5x5-31L

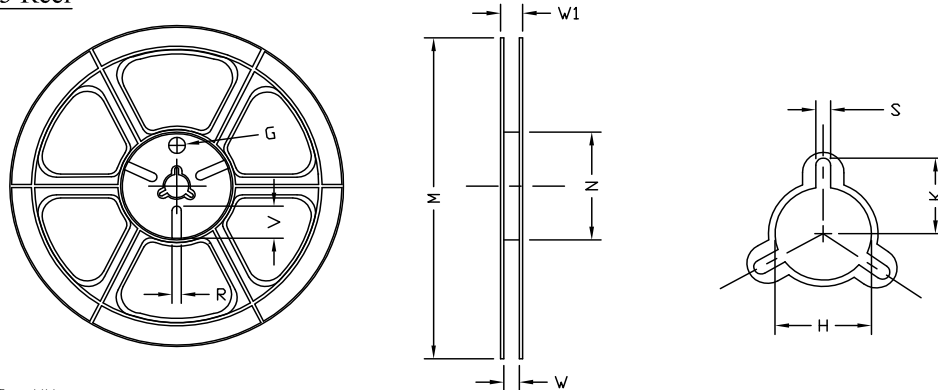
#### QFN5x5 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 <sup>+0.1</sup> <sub>-0.0</sub>	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

#### QFN5x5 Reel

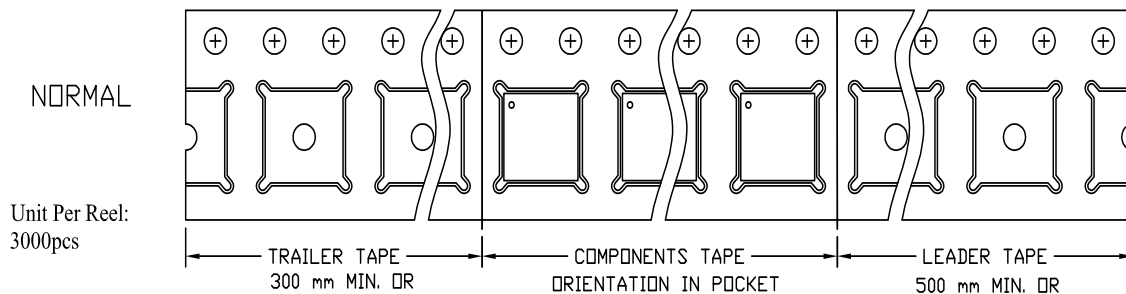


UNIT: MM

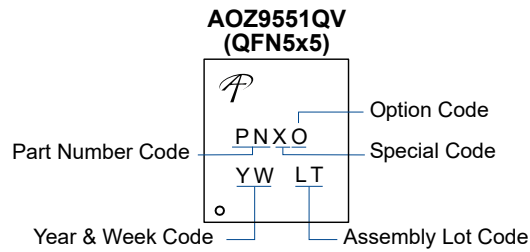
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	φ330	φ330.0 ±2.0	φ100.0 ±1.0	12.4 <sup>+2.0</sup> <sub>-0.0</sub>	17.0 <sup>+2.6</sup> <sub>-1.2</sub>	φ13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

#### QFN5x5 Tape

Leader / Trailer  
& Orientation



## Part Marking



Part Number	Description	Code
AOZ9551QV	Green Product	CP00

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.