

Alpha & Omega Semiconductor Product Reliability Report

AOZ1382DI-01, rev B

Plastic Encapsulated Device

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This AOS product reliability report summarizes the qualification results for AOZ1382DI-01 in DFN3x5.2-20L package. Accelerated environmental tests are performed on a specific sample size and samples are electrically tested before and after each time point. Review of final electrical test results confirm that AOZ1382DI-01 pass the AOS quality and reliability requirements. The released products will be categorized by its process family and routinely monitored for continuous improvement of product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTOL	T _J = 125°C, V _{IN} = Vccmax	168 / 500 / 1000 hours	231 pcs	0	JESD22-A108
Preconditioning (Note A)	168hr 85°C / 85%RH + 3 cycle reflow@260°C (MSL 1)	-	924 pcs	0	JESD22-A113
HAST	T _A = 130°C, RH = 85%, P = 33.3psia	96 hours	231 pcs	0	JESD22-A110
Autoclave	T _A = 121°C, RH = 100%, P = 29.7psia	96 hours	231 pcs	0	JESD22-A102
Temperature Cycle	T _A = -65°C to 150°C, air to air	250 / 500 / 1000 cycles	231 pcs	0	JESD22-A104
High Temperature Storage	T _A = 150°C	1000 hours	231 pcs	0	JESD22-A103

Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

FIT rate (per billion): 15.26

MTTF = 7480 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 \times 10^9 / [2 (N) (H) (Af)] = 15.26$

MTTF = 10^9 / FIT = 7480 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval

N = Total Number of units from burn-in tests

H = Duration of burn-in testing

Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and T_{use} = 55°C)

Acceleration Factor [Af] = Exp $[Ea/k (1/T_J u - 1/T_J s)]$



Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	125 deg C
Af	77	26	9.8	3.9	1.7	1

T_J s = Stressed junction temperature in degree (Kelvin), K = C + 273.16

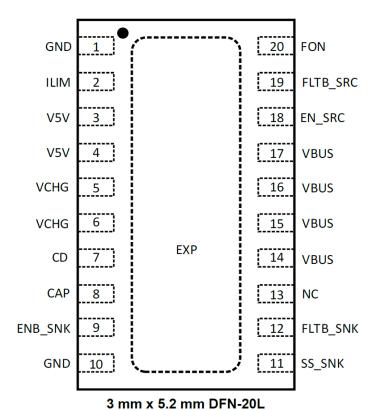
T_J u =The use junction temperature in degree (Kelvin), K = C + 273.16

 \mathbf{k} = Boltzmann's constant, 8.617164 X 10⁻⁵eV / K

III. ESD and Latch Up Test Results

Test	Test Conditions	Total Sample Size	Number of Failures	Reference Standard
Electrostatic Discharge Human Body Model	T _A = 25°C, +/-2kV	3	0	JESD-A114
Electrostatic Discharge Charged Device Model	T _A = 25°C, +/-1kV	3	0	JESD-C101
Latch Up	T _A = 25°C, +/-100mA, 1.5x OV	6	0	JESD78
Latch Up	T _A = 85°C, +/-100mA, 1.5x OV	6	0	JESD78
Electrostatic Discharge Immunity (only VOUT pin)	T _A = 25°C, +/-8kV	3	0	IEC61000-4-2

(1) ATE results are used to determine PASS/FAIL. Parametric shift <10%.



Top Transparent View