ALPHA & OMEGA SEMICONDUCTOR

AON6884

40V Dual N-Channel MOSFET

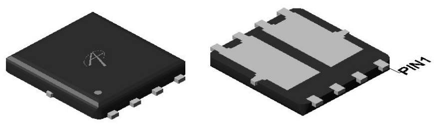
General Description

The AON6884 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. This is an all purpose device that is suitable for use in a wide range of power conversion applications.

Product Summary

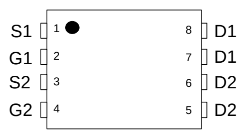
V_{DS}	40V
I_D (at V_{GS}=10V)	34A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 11.3mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	< 13.8mΩ

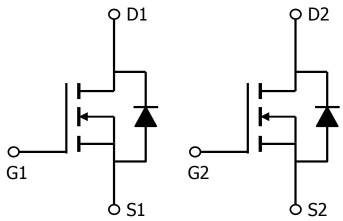
100% UIS Tested
100% R_g Tested



DFN5X6 EP2

Top View





Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	34	A
	T_C=100℃		21	
Pulsed Drain Current [C]		I_{DM}	120	
Continuous Drain Current	T_A=25℃	I_{DSM}	9	A
	T_A=70℃		7	
Avalanche Current [C]		I_{AS}, I_{AR}	35	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	61	mJ
Power Dissipation [B]	T_C=25℃	P_D	21	W
	T_C=100℃		8	
Power Dissipation [A]	T_A=25℃	P_{DSM}	1.6	W
	T_A=70℃		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{θJA}$	35	45	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		65	80	℃/W
Maximum Junction-to-Case	Steady-State	$R_{θJC}$	5	6	℃/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.55	2.1	2.7	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	120			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=10A		9.4	11.3	mΩ
		T_J=125°C		14	17	
		V_{GS}=4.5V, I_D=10A		11	13.8	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=10A		50		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				25	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz	1200	1500	1950	pF
C_{oss}	Output Capacitance		150	215	280	pF
C_{rss}	Reverse Transfer Capacitance		80	135	190	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1.7	3.5	5.3	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=10A	22	27.2	33	nC
Q_g(4.5V)	Total Gate Charge		10	13.6	16	nC
Q_{gs}	Gate Source Charge		3.6	4.5	5.4	nC
Q_{gd}	Gate Drain Charge		3.8	6.4	9	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=2Ω, R_{GEN}=3Ω		6.4		ns
t_r	Turn-On Rise Time			17.2		ns
$t_{D(off)}$	Turn-Off DelayTime			29.6		ns
t_f	Turn-Off Fall Time			16.8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=10A, dI/dt=500A/µs	9	13	17	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=10A, dI/dt=500A/µs	25	35	45	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse ratin g.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

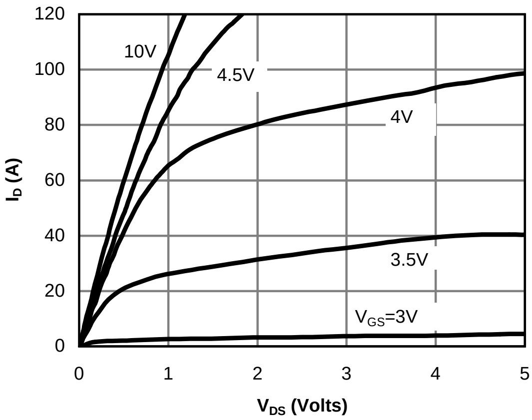


Fig 1: On-Region Characteristics (Note E)

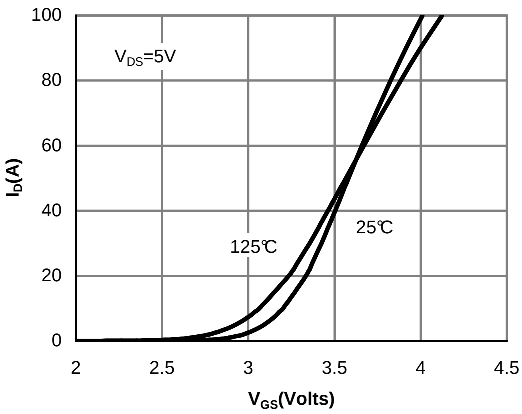


Figure 2: Transfer Characteristics (Note E)

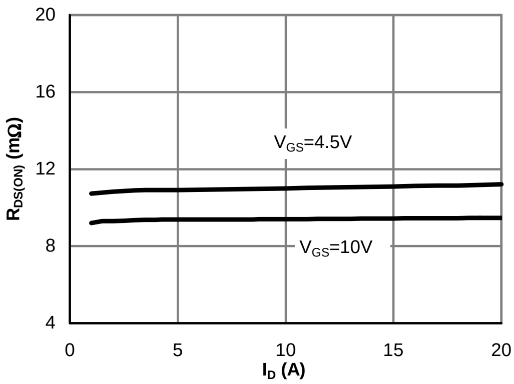


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

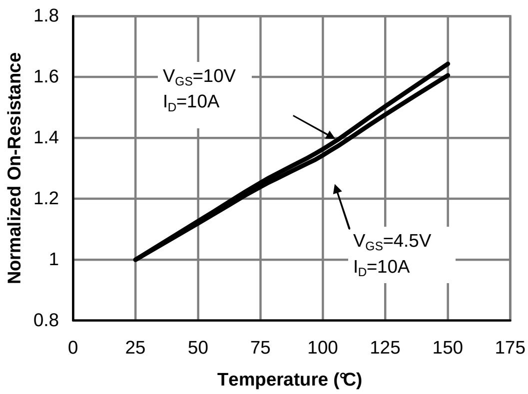


Figure 4: On-Resistance vs. Junction Temperature (Note E)

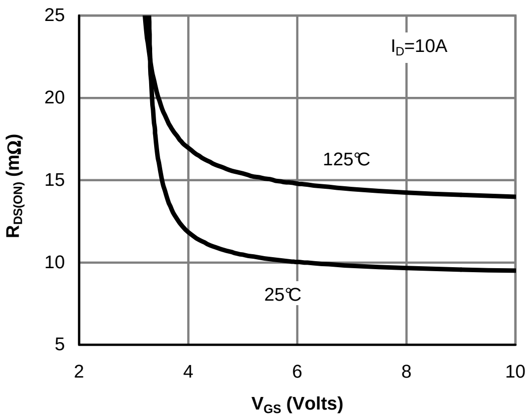


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

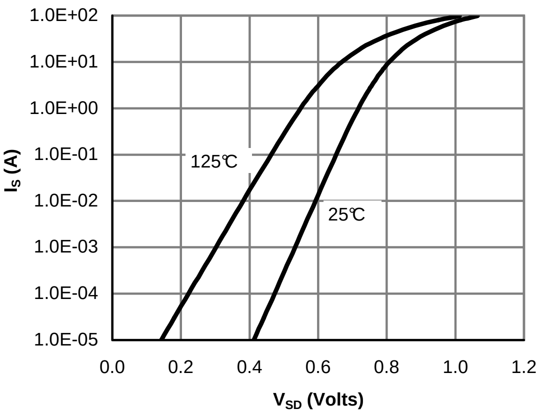


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

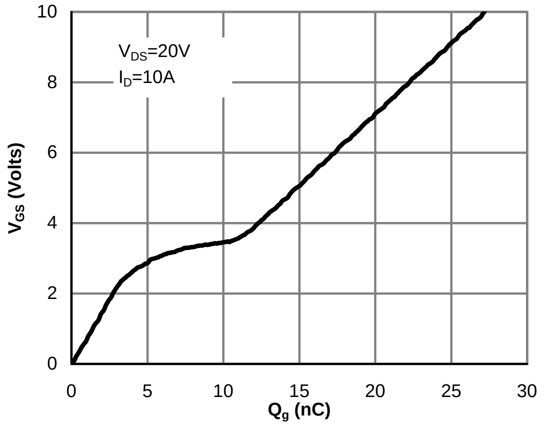


Figure 7: Gate-Charge Characteristics

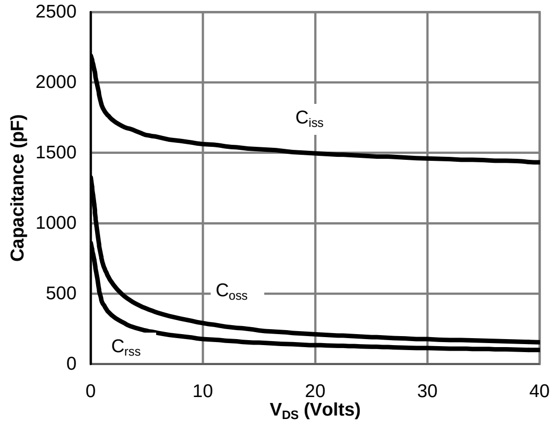


Figure 8: Capacitance Characteristics

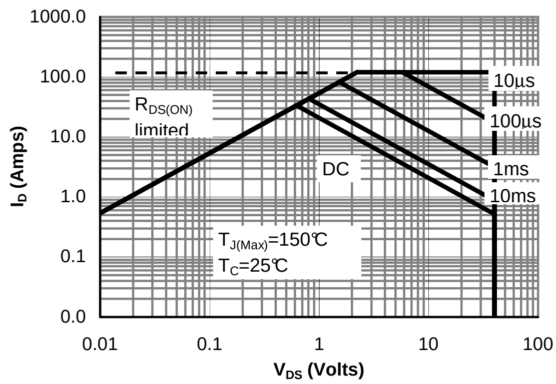


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

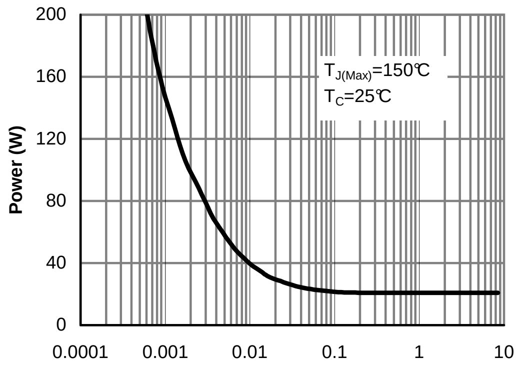


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

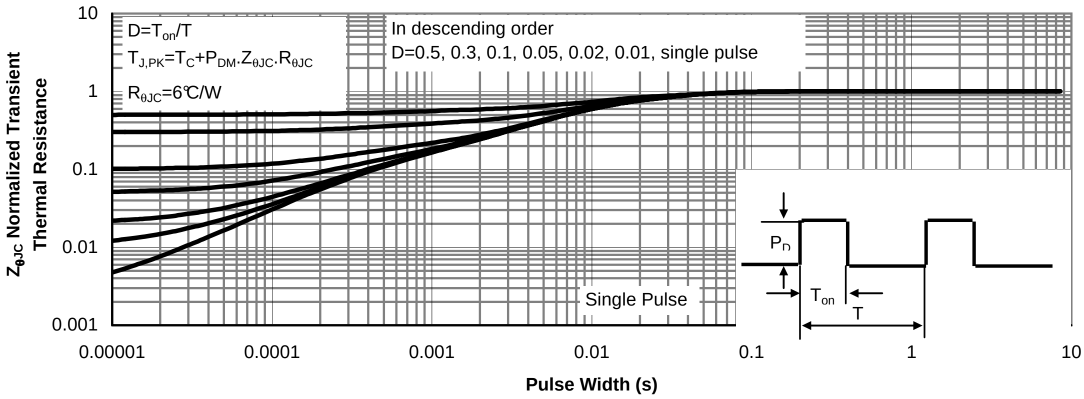


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

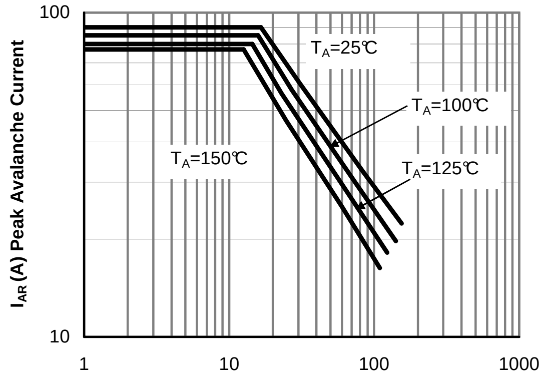


Figure 12: Single Pulse Avalanche capability (Note C)

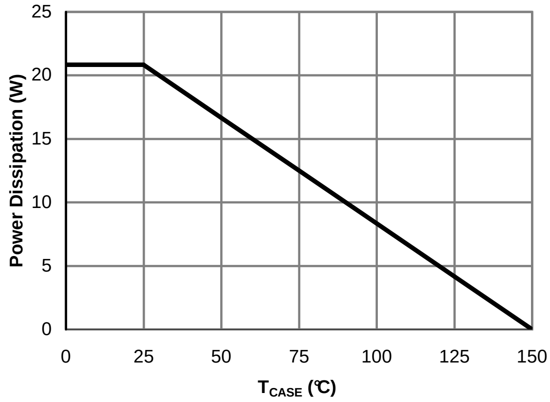


Figure 13: Power De-rating (Note F)

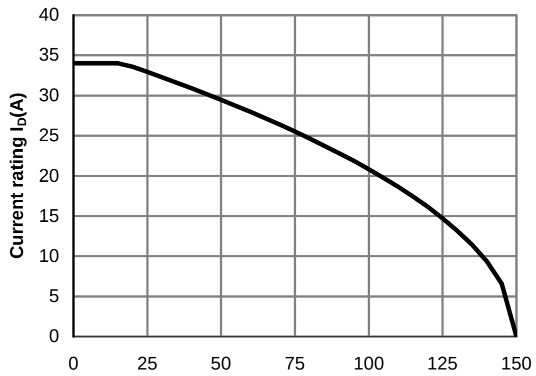


Figure 14: Current De-rating (Note F)

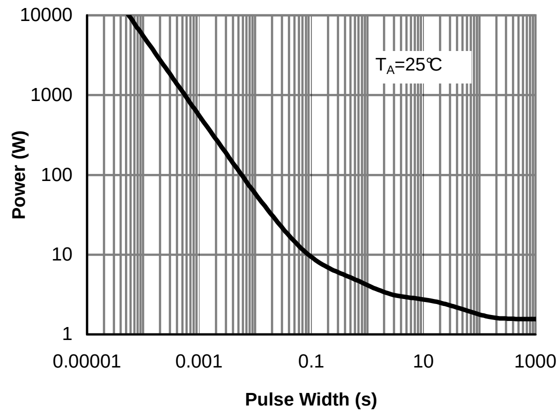


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

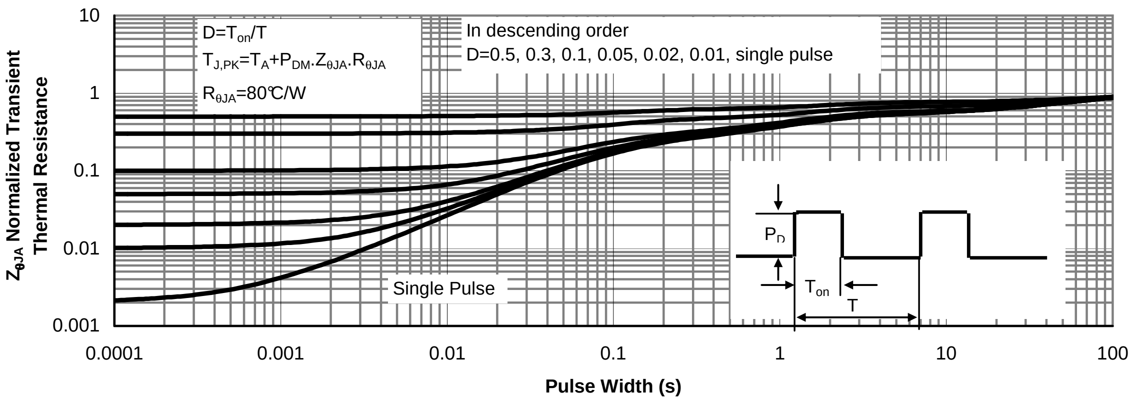
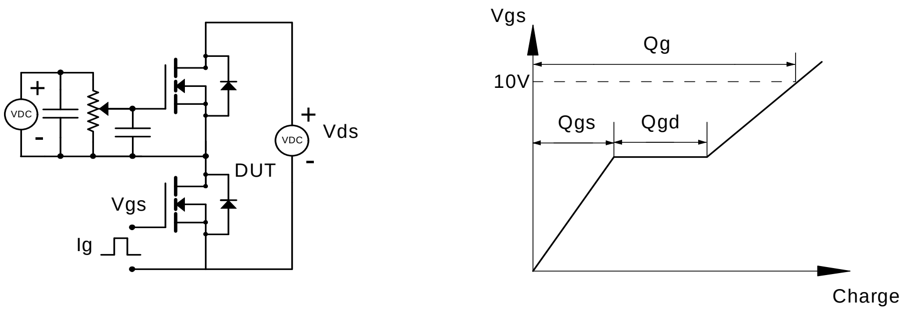
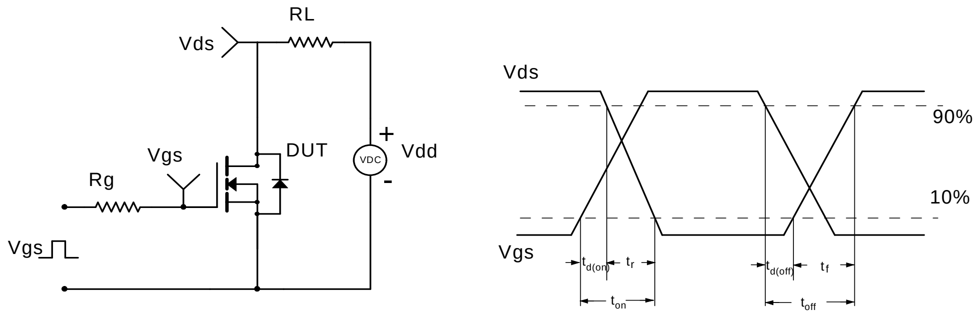


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

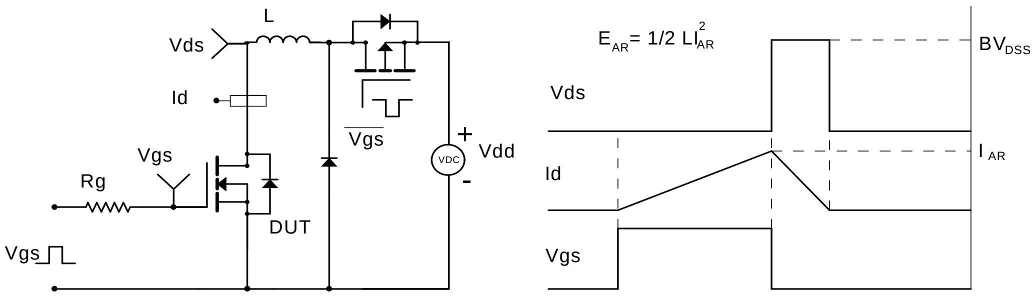
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms