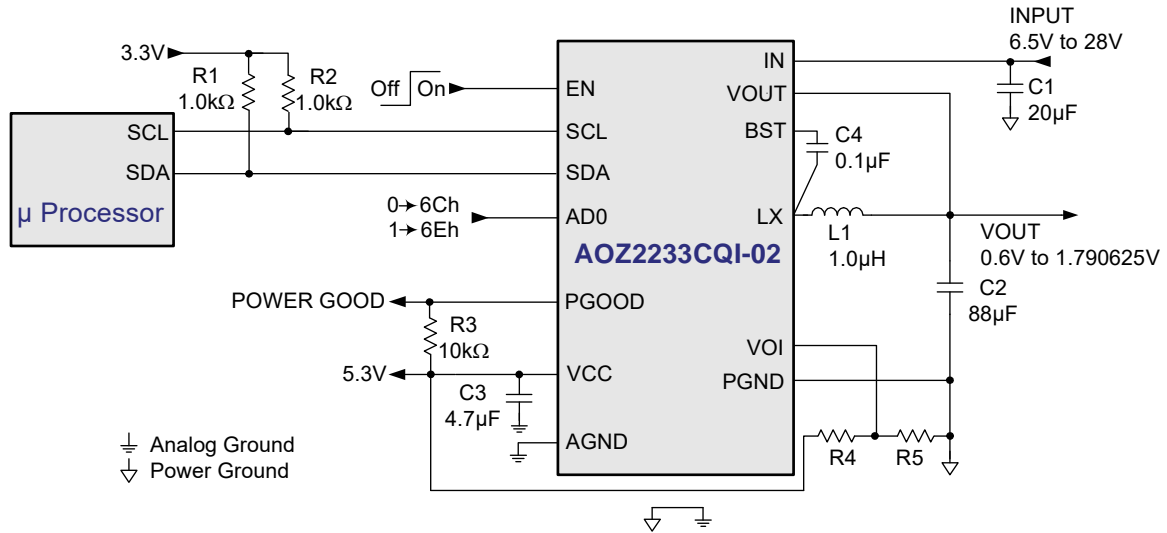


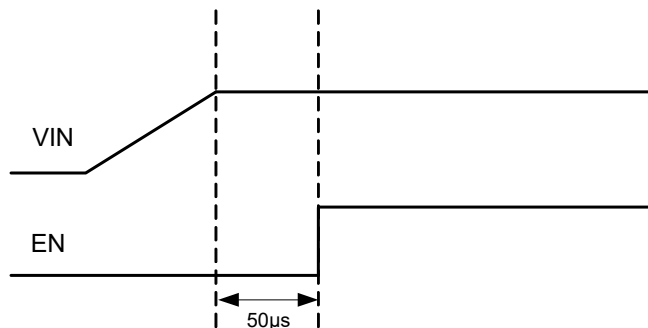
Typical Application



Option Table

Code \ Item	AD0	Address (Binary)	Address (Hex)
AOZ2233CQI-01	Ground (0)	01101000	68h
	Open (1)	01101010	6Ah
AOZ2233CQI-02	Ground (0)	01101100	6Ch
	Open (1)	01101110	6Eh

Recommended Start-up Sequence



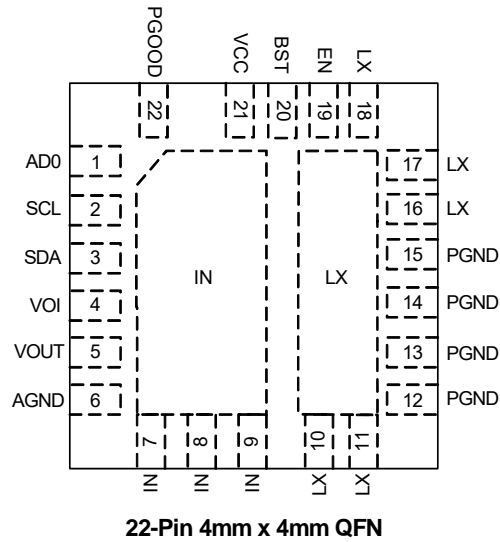
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ2233CQI-02	-40°C to +85°C	22-Pin 4mm x 4mm QFN	Green Product



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant. Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

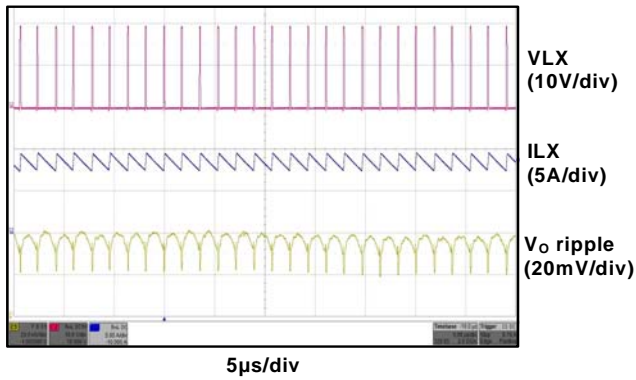
Pin Configuration



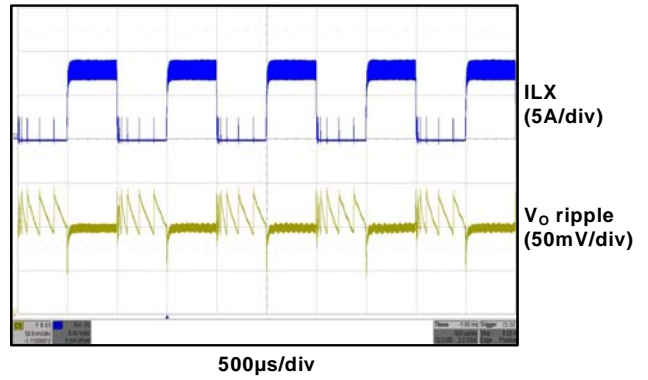
Typical Performance Characteristics

Circuit of Typical Application. $T_A = 25^\circ\text{C}$, $V_{IN} = 19\text{V}$, $V_{OUT} = 1\text{V}$, $f_s = 400\text{kHz}$ unless otherwise specified.

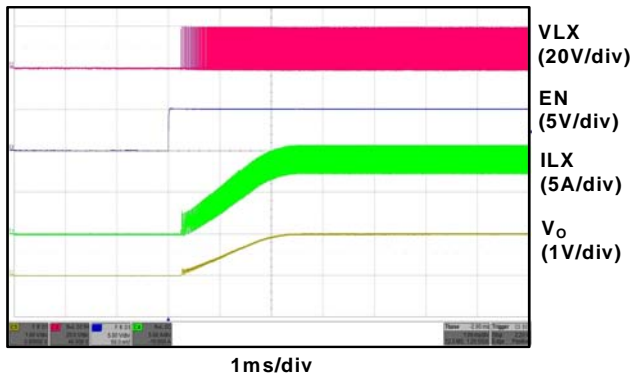
Normal Operation



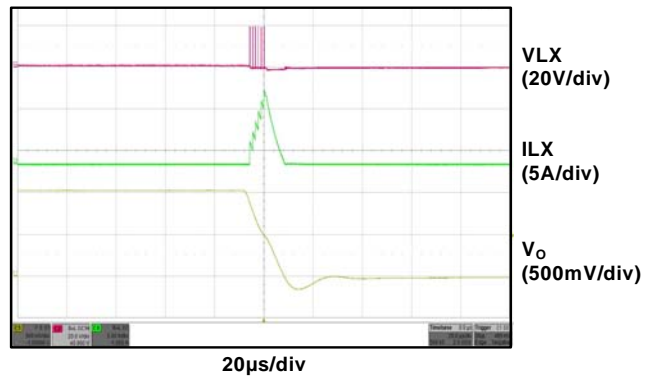
Load Transient 0A to 8A



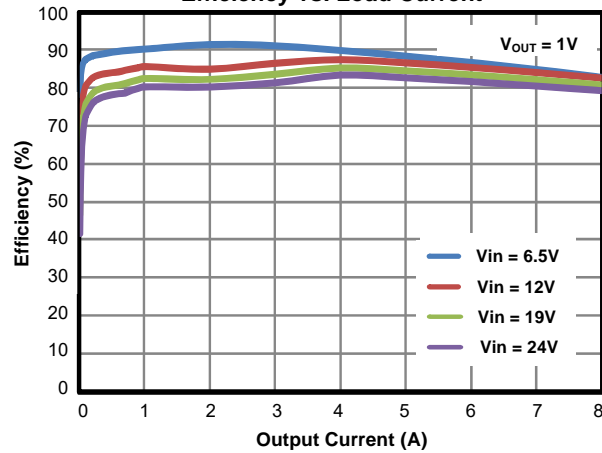
Full Load Start-up



Short Circuit Protection



Efficiency vs. Load Current



I²C Control Specification⁽³⁾⁽⁴⁾⁽⁵⁾

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V _{IL}	Low level input voltage				0.6	V
V _{IH}	High level input voltage		2.9			V
V _{hys}	Hysteresis of Schmitt trigger inputs		0.11			V
V _{OL}	Low level output voltage (Open drain, 3mA sink current)				0.4	V
T _{SP}	Pulse width of spikes suppressed by input filter		32			ns
f _{SCL}	SCL clock frequency				400	kHz
t _{HD;STA}	Hold time (repeated), START condition		0.6			μs
t _{LOW}	Low period of SCL clock		1.3			μs
t _{HIGH}	High period of SCL clock		0.6			μs
t _{SU;STA}	Set-up time for a repeated START condition		0.6			μs
t _{HD;DAT}	Data hold time		50		900	ns
t _{SU;DAT}	Data set-up time		100			ns
t _r	Rise time (SDA or SCL)		20+0.1C _b		300	ns
t _f	Fall time (SDA or SCL)		5+0.1C _b		300	ns
t _{SU;STO}	Set-up time for STOP condition		0.6			μs
t _{BUF}	Bus free time between STOP and START conditions		1.3			μs
C _b	Capacitive load for each bus line				400	pF
I _d	SDA driver capability		25		100	mA

Notes:

3. Ensured by design. Not production tested.
4. Refer to Figure 1 for I²C timing definitions.
5. C_b = capacitance of bus line in pF.

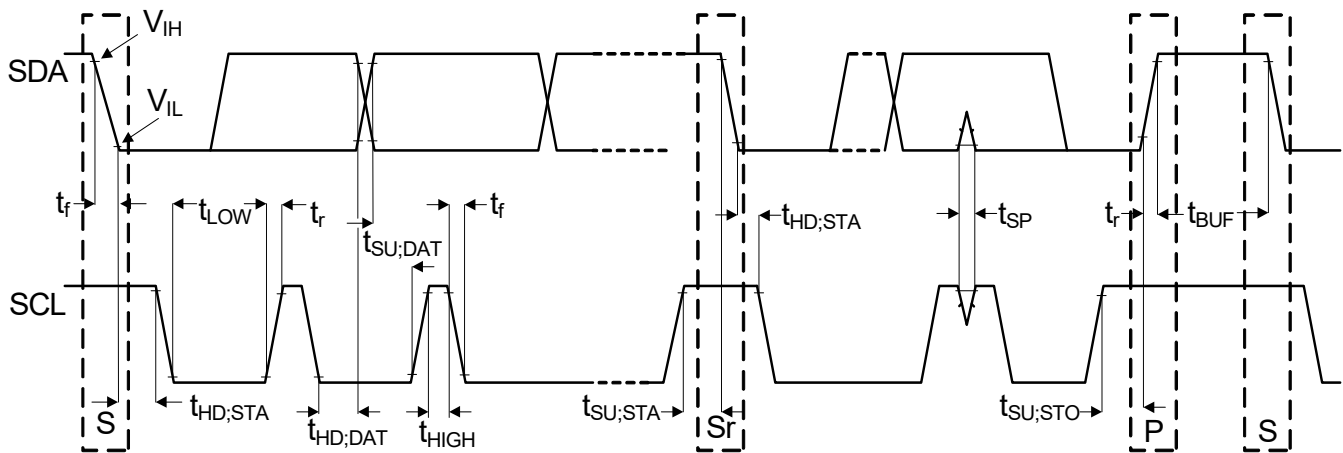


Figure 1. I²C Timing Definitions

I²C Register Maps

Register Name	Register Address	Bit 7	Bit6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Output Voltage	00	Odd Parity	Output Voltage [6:0]						
Control A	01	Internal Mode			Output Voltage Change	PFMb			Protection Mode

Summary of Default Control Bits

Control Bit(s)	Default	Function
VOUT [6:0]	0110010	VOUT code, 7 bits VOUT [6:0]. Part default to 1.068750V.
Internal Mode	0 (External Mode)	0 case: External Mode 1 case: Internal Mode (1). If set to 1, the part switches to internal mode and VOUT register value controls output voltage. (2). The part can be set back to external control mode at any time by wiring this bit to 0.
Output Voltage Change	0	0 case: Internal protection on 1 case: Internal protection off (1). If set to 0, when VOUT code change, the internal protection isn't turned off. (2). If set to 1, when VOUT code change, the internal protection is turned off to avoid triggering internal protection.
PFMb	1	Select PFM or PWM at light load. 0 case: PFM 1 case: PWM Part defaults to PWM.
Protection Mode	1	Select Latch-off or Auto-recovery for protection. 0 case: Auto-recovery mode 1 case: Latch-off mode Part defaults to Latch-off mode.

Odd Parity Bit

The odd parity bit is set by the Master controller to be the exclusive-NOR of the output voltage [6:0] bits. It will be used by the AOZ2233CQI-02 to check that a valid data byte has been received. If odd parity is not equal to the exclusive-NOR of the output voltage [6:0] bits, the

AOZ2233CQI-02 assumes that an error has been occurred during the data transmission, and it will not send an ACK bit, nor will it reset the VOUT to the received code. (or, if the Control register will not reset the register contents as requested). The Master should try again to re-send the data. When reading back the VOUT register, the parity bit is sent back.

