ALPHA & OMEGA SEMICONDUCTOR

AOZ9510QV

28 V/20 A Smart Motor Module

General Description

The AOZ9510QV is an integrated half-bridge gate driver with smart functions. The device includes one half-bridge gate driver, capable of driving high-side and low-side N-channel MOSFETs. Using two AOZ9510QV for single phase motor driver and three AOZ9510QV for three phase motor drivers.

The device features multiple protection functions such as over current protection, short circuit protection, and over temperature protection. Moreover, AOZ9510QV provides adjustable gate drive sink and source current control. By doing this control, user can optimize performances of EMI and efficiency.

The AOZ9510QV is available in a 4mm×4mm QFN-23L package and is rated over a -40°C to +125°C ambient temperature range.

Features

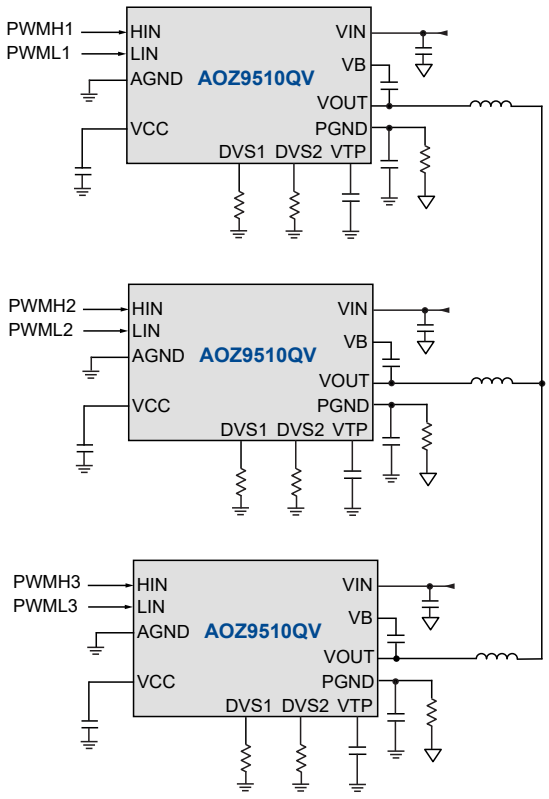
- Input voltage range:
  - 10.8 V to 28 V
- Maximum Output Current 20A
- Adjustable Gate Drive Sink/Source Current
- Junction Temperature Monitor
- Support 100% PWM Operation
- Integrated Bootstrap Diode
- Low $R_{DS(ON)}$ internal NFETs
  - 6 mΩ for Both HS/LS
- Thermal Protection
- Over Current Protection
- Short Circuit Protection
- Thermally enhanced 23-pin 4×4 QFN

Applications

- BLDC Motor Drive
- Fans and Pumps
- Power Tools

Green Product

Typical Application (Three Phases)



Ordering Information

Part Number	Temperature Range	Package	Environmental
AOZ9510QV	-40 °C to +125 °C	QFN4x4-23L	Green

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

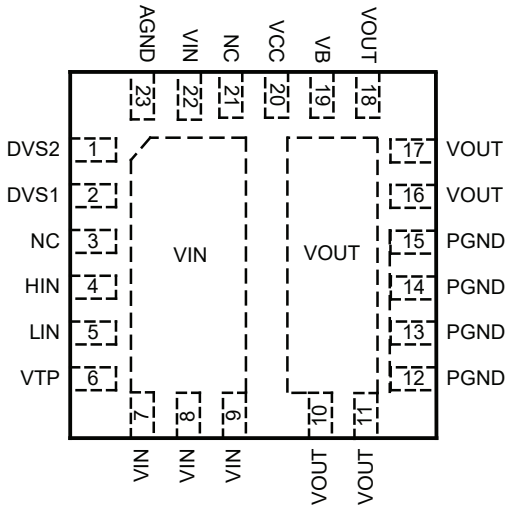


Figure 1. AOZ9510QV
QFN4x4-23L

Pin Description

Pin Number	Pin Name	Pin Function
1	DVS2	Adjustable gate drive sink current.
2	DVS1	Adjustable gate drive source current.
3,21	NC	No connect.
4	HIN	PWM input for high-side MOSFET.
5	LIN	PWM input for low-side MOSFET.
6	VTP	Junction temperature monitor and SCP indicator.
7, 8, 9, 22	VIN	Supply input. All VIN pins must be connected together.
10, 11, 16, 17, 18	VOUT	Motor drive output.
12, 13, 14, 15	PGND	Power ground.
19	VB	Bootstrap capacitor connection. Connect an external capacitor between VB and VOUT for supplying high-side MOSFET.
20	VCC	Supply input for analog functions. Bypass VCC to AGND with a 0.1 µF~10 µF ceramic capacitor and as close to VCC pin as possible.
23	AGND	Analog ground.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VIN to AGND	-0.3 V to 30 V
VOUT to AGND	-0.3 V to 30 V
VOUT to AGND (transient, 30 ns)	-7V to VIN+7V
VB to AGND	-0.3V to 40V
DVS, VCC to AGND	-0.3 V to 13.2 V
HIN, LIN to AGND	-0.3 V to 5.5V
PGND to AGND	-0.3 V to +0.3 V
PGND to AGND (transient, 100 ns)	-6.5V to 6.5V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating	2 kV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	10.8 V to 28 V
Ambient Temperature (T_A)	-40°C to +125°C
Package Thermal Resistance Θ_{JA} Θ_{JC}	 32 °C/W 4 °C/W

Electrical Characteristics

T_A = 25 °C, unless otherwise specified.

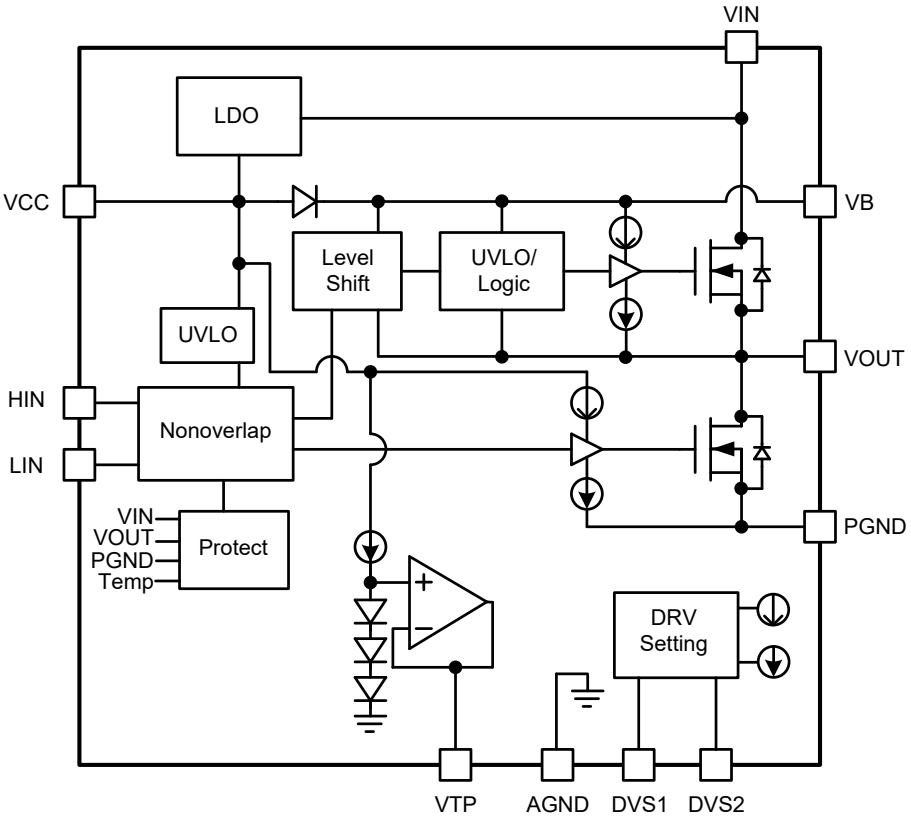
Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC	VCC	VIN = 12 V, HIN/LIN=0 V	7.8	8	8.2	V
	Line Regulation	VIN = 12 V~24 V, HIN/LIN=0 V		0.1		%/V
I_{VCC_short}	I_{VCC} Short Current	VIN = 24 V, HIN/LIN=0 V, Monitor I_{VCC}		1		mA
V_{UVLO_R}	VCC UVLO Rising	LIN = High, HIN = Low, Monitor VOUT Floating to Short	7	7.5	8	V
V_{UVLO_F}	VCC UVLO Falling	LIN = High, HIN = Low, Monitor VOUT Short to Floating		5.1		V
VB_{UVLO_R}	VB-VOUT UVLO Rising	HIN = High, LIN = Low, Monitor VOUT Floating to Short	6.7	7.2	7.7	V
VB_{UVLO_F}	VB-VOUT UVLO Falling	HIN = High, LIN = Low, Monitor VOUT Short to Floating	5.2	5.5	5.8	V
I_{VIN_ST}	I_{VIN} Standby Current	HIN/LIN = 0 V, Monitor VIN Current		2.4		mA
$I_{VB\text{-}VOUT\_ST}$	$I_{VB\text{-}VOUT}$ Standby Current	VIN = 10 V, HIN/LIN = 0 V, VOUT = 0 V, VB-VOUT= 10 V, Monitor VB-VOUT Current		25		µA
V_{HLIN_L}	HIN/LIN Logic Low Voltage	VIN = 12 V	0		1.2	V
V_{HLIN_H}	HIN/LIN Logic High Voltage	VIN = 12 V	2.2		5.5	V
R_{HLIN_IN}	HIN/LIN Input Pull Low Impedance			280		kΩ
t_{HIN_RP}	HIN Rising Propagation Delay	VIN = 10 V, DVS = 20 kΩ, VOUT to GND = 100 Ω, HIN = Low to High, Monitor HIN High TH to 10% VOUT		45		ns

Electrical Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HIN_FP}	HIN Falling Propagation Delay	VIN = 10 V, DVS = 20 kΩ, VOUT to GND = 100 Ω, HIN = High to Low, Monitor HIN High TH to 90% VOUT		80		ns
t_{LIN_RP}	LIN Rising Propagation Delay	VIN = 10 V, DVS = 20 kΩ, VOUT to VIN = 100 Ω, LIN = Low to High, Monitor LIN High TH to 90% VOUT		85		ns
t_{LIN_FP}	LIN Falling Propagation Delay	VIN = 10 V, DVS = 20 kΩ, VOUT to VIN = 100 Ω, LIN = High to Low, Monitor LIN Low TH to 10% VOUT		40		ns
T_{DM_R}	Delay Matching Rising	Difference between t_{HIN_RP}, t_{LIN_RP}		40		ns
T_{DM_F}	Delay Matching Falling	Difference between t_{HIN_FP}, t_{LIN_FP}		45		ns
V_{DVS}	DVS	VIN = 12 V, DVS to GND = 20 kΩ	0.97	1	1.03	V
I_{DVS_MIN}	DVS Min. Source Current	VIN = 12 V, DVS = 4 V		0.5		µA
I_{DVS_MAX}	DVS Max. Source Current	VIN = 12 V, DVS = 0.8 V		140		µA
R_{H_ON}	VIN-VOUT R_{ON}	VIN = 12 V, HIN = 5 V, VB-VOUT = 8 V, I_{VOUT}=1A		6		mΩ
R_{L_ON}	VOUT-PGND R_{ON}	VIN = 12 V, LIN = 5 V, PGND = 0, I_{VOUT} = 1 A		6		mΩ
V_{SD}	Boost Diode Forward Voltage	Forward Current = 2 mA		0.15		V
T_{OTP}	Over Temperature Protection	VIN = 12 V		140		°C
I_{OCP}	Over Current Protection	VIN = 12 V		34		A
I_{SCP}	Short Current Protection	VIN = 12 V		68		A
t_{oc}	OCP/SCP debounce time	VIN = 12 V		1.5		µs
V_{TP}	$V_{TP\_25°C}$	VIN = 12 V at 25°C		1.9		V
	$V_{TP\_125°C}$	VIN = 12 V at 125°C		1.3		V

Functional Block Diagram



Typical Characteristics

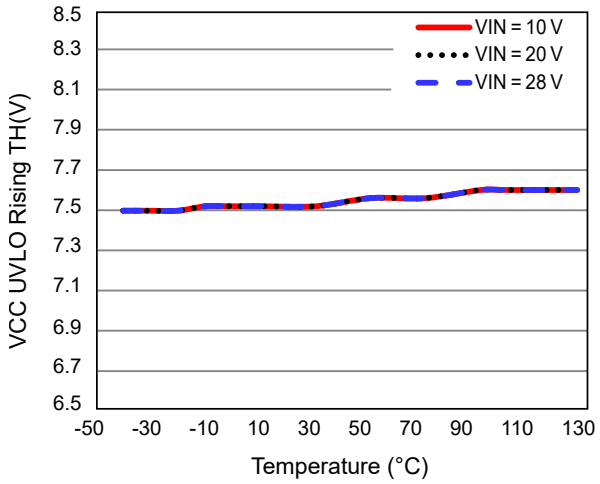


Figure 2. VCC UVLO Rising Threshold

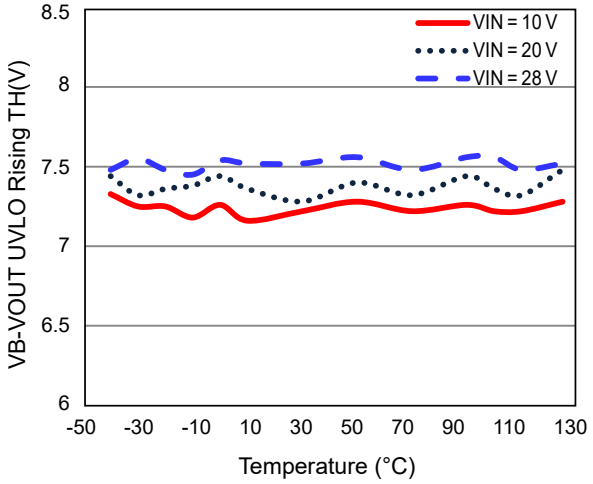


Figure 3. VB-VOUT UVLO Rising Threshold

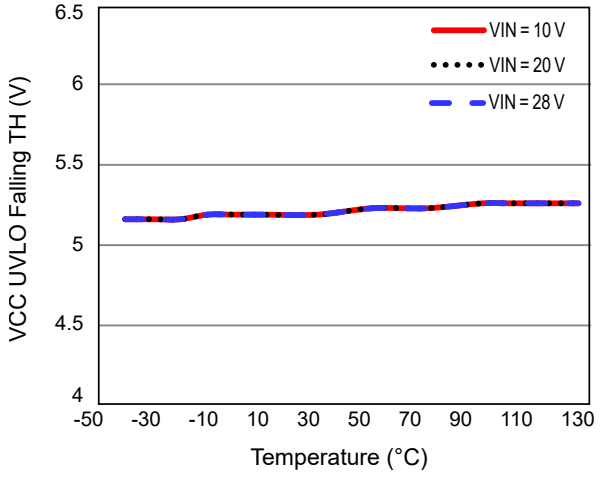


Figure 4. VCC UVLO Falling Threshold

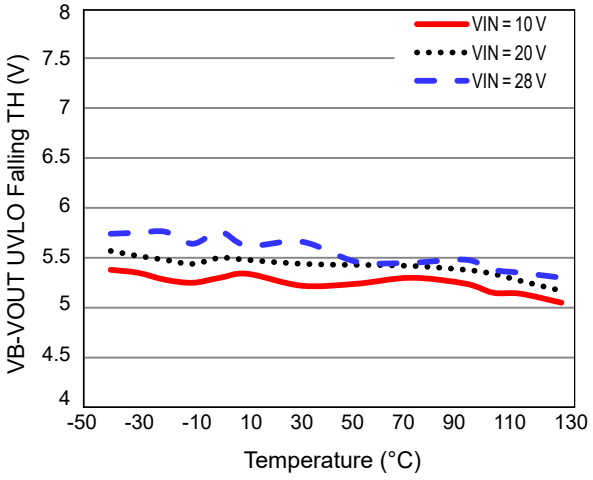


Figure 5. VB-VOUT UVLO Falling Threshold

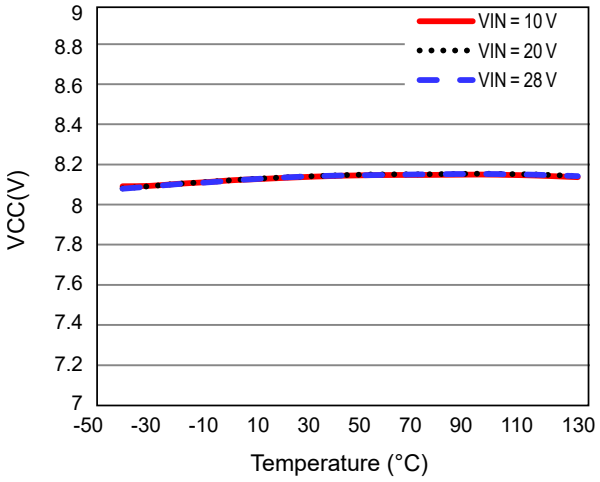


Figure 6. VCC Regulation

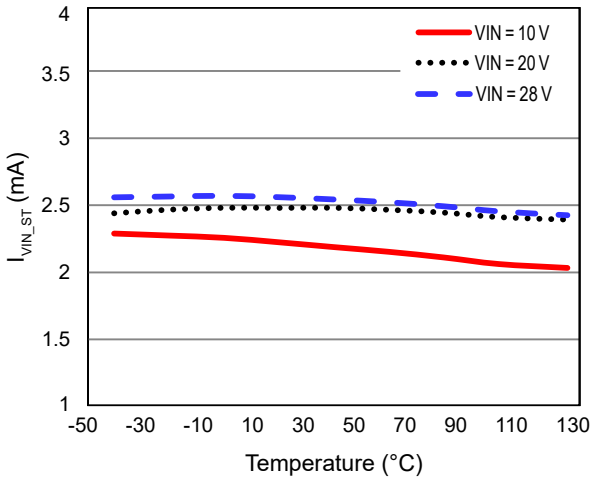


Figure 7. Input Standby Current

Typical Characteristics *(Continued)*

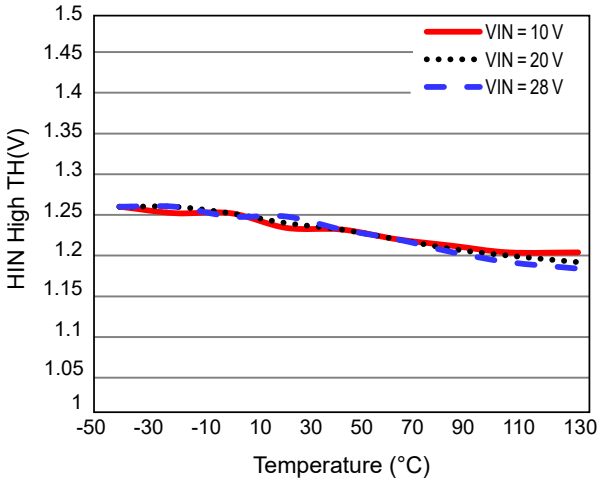


Figure 8. HIN High Threshold

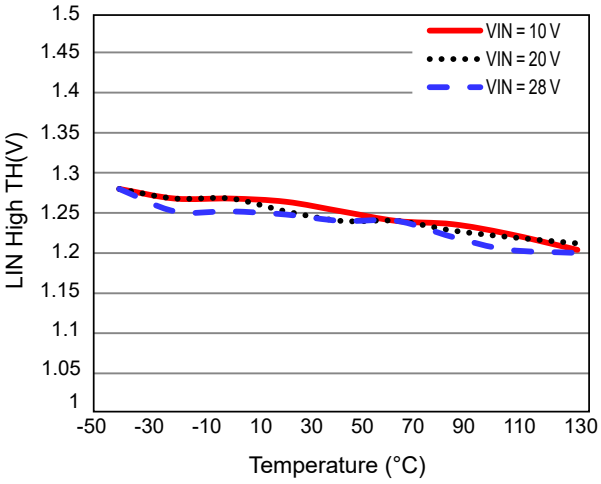


Figure 9. LIN High Threshold

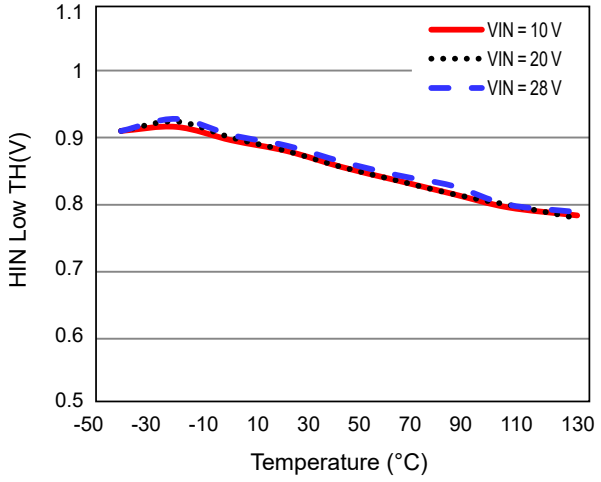


Figure 10. HIN Low Threshold

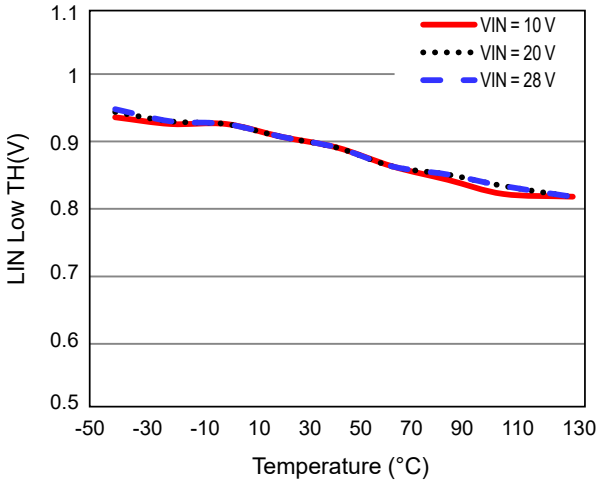


Figure 11. LIN Low Threshold

Detailed Description

The AOZ9510QV is an integrated half-bridge gate driver for motor drive applications. The device includes one half-bridge gate driver, capable of driving high-side and low-side N-channel MOSFETs. The AOZ9510QV provides adjustable source/sink current of both high/low-side gate drive output current which can optimize performances of EMI and efficiency on different PCB layout and applications.

In addition, the AOZ9510QV provides several fault protections, such as OCP, UVLO, SCP, OTP and non-overlapping mechanism.

The AOZ9510QV is available in 23-pin 4mm×4mm QFN package.

Input Power Architecture

The AOZ9510QV integrates an internal linear regulator to generate 8 V (±3%) VCC from input pins. If input voltage is lower than 5.8V, the linear regulator will be triggered VB-VOUT UVLO. The VCC maximum source current is 0.8 mA. Therefore, extra external source is needed when operation switching frequency exceeds 30 kHz.

Non-overlapping

For forbidding shoot-through, HIN or LIN is invalid when HIN or LIN goes high state before other one. For example, low-side gate state keeps low regardless of the state of LIN when HIN is high at first, and vice versa.

So when Shoot-through occurs, VOUT will follow the previous normal state, as illustrated Figure 12.

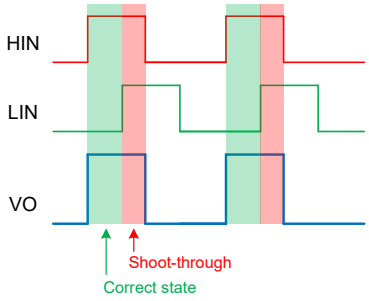


Figure 12. Shoot-through Behavior

Fault Protection

Over Current Protection (OCP)

There are fixed OCP/SCP points on AOZ9510QV I_{OCP} = 34 A and I_{SCP} = 68 A.
The time point of OCP detection is 1.5 µs (debounce time) after the rising edge of HIN. If the current exceeds the I_{OCP}, the internal counter will start counting, as illustrated Figure 13. When 14 consecutive OCPs are detected, the high side MOSFET will be turned off on the 14th time and the low side MOSFET is turned on. This behavior is called current limit. When the current is less than 0.8*I_{OCP} the current limit is released.

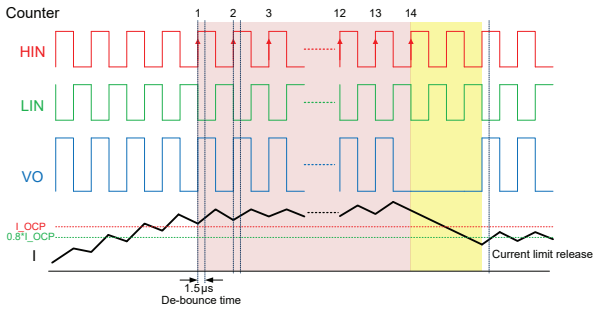


Figure 13. OCP timing diagram

Short Current Protection (SCP)

If the current is greater than SCP point, AOZ9510QV enters SCP, VTP pin will be pulled high, and then AOZ9510QV enters latch, VCC needs to be reset to return to normal operation state.

Over Temperature Protection (OTP)

When the junction temperature reach 140°C, AOZ9510QV enters OTP, and release when the temperature drops to 120°C.

Thermal Monitor

The junction temperature can be monitored by using internal current mirror pass through internal diodes. The related V_{TP} equation can be approximated as below:

$$V_{TP} = 1.9\,V - (Temp - 25°C) \times 6\,mV$$

Please note that VTP is high when SCP is triggered.

Adjustable Source/Sink Current

It's hard to meet all of EMI specifications in different applications. So, AOZ9510QV provides external adjustable resistors for tuning gate drive source and sink current.

DVS1 and DVS2 are used to tune gate drive source and sink current, respectively. A resistor connects between each DVS pin and GND to setting gate drive source / sink current by internal current mirror, as illustrated in Figure 14. Source and sink current use maximum capability to drive when DVS pins are floating or the voltage on DVS pins exceed 4 V. The user can get the same source and sink capability by using DVS1 to design and DVS2 floating. The suggestion range of R_{DVS} is 20 kΩ~100 kΩ.

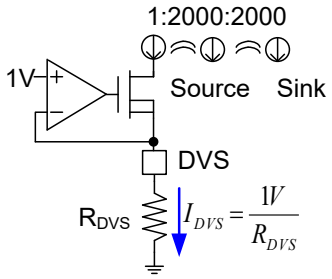


Figure 14. Source/Sink Current Setting

In addition, source and sink current controls are implemented only during MOSFET Miller effect and V_{GS} > 1 V, as illustrated in Figure 15.

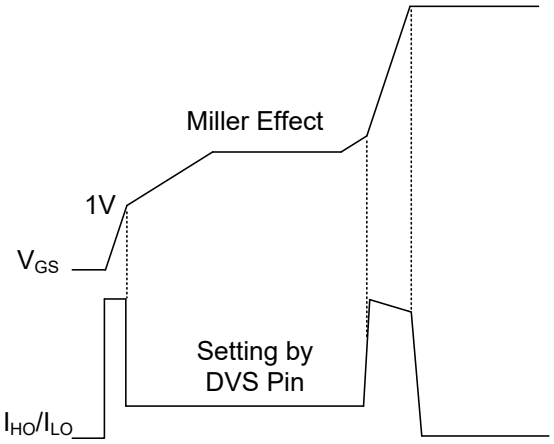
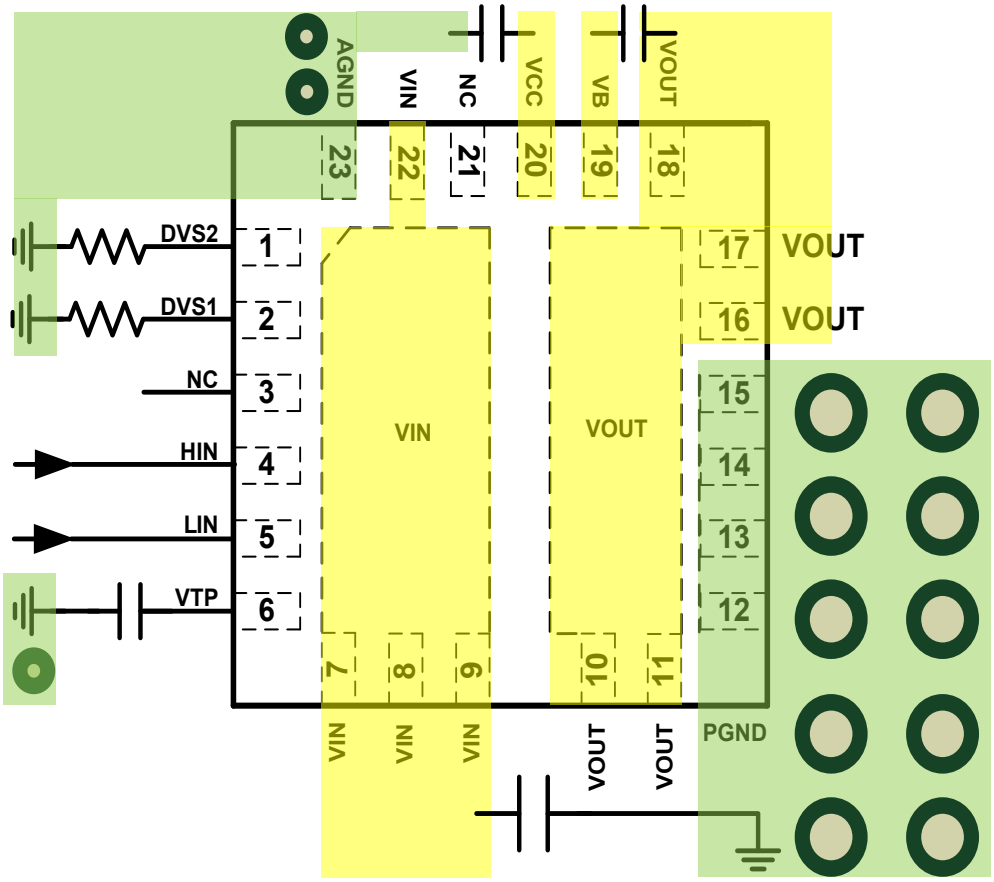


Figure 15. Source/Sink Current Implement Waveform

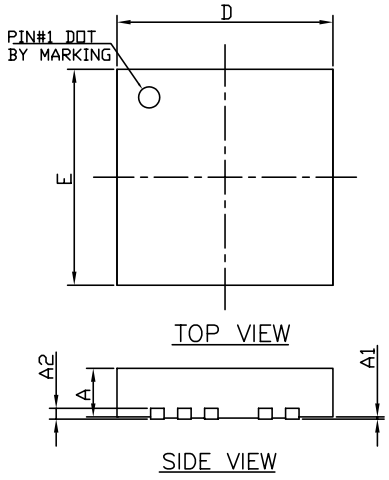
Layout Considerations

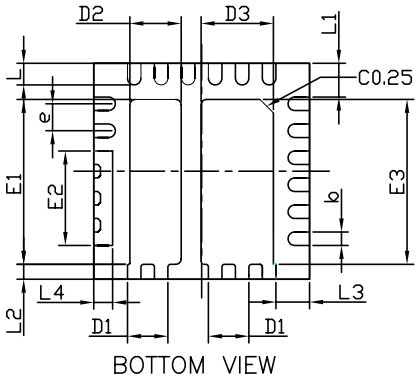
Several layout tips are listed below for the best electric and thermal performance.

1. The VIN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to VIN pins to help thermal dissipation.
2. Input capacitors should be connected to the VIN pins and the PGND pins as close as possible to reduce the switching spikes.
3. The VOUT pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connected a large copper plane to VOUT pins to help thermal dissipation.
4. Decoupling capacitor C_{VCC} should be connected to VCC and AGND as close as possible.
5. Bootstrap capacitor C_B should be connected to VB and VOUT as close as possible.
6. A ground plane is preferred. PGND and AGND must be connected to the ground plane through vias.
7. Keep sensitive signal traces such as feedback trace and digital signals far away from the VOUT pins.



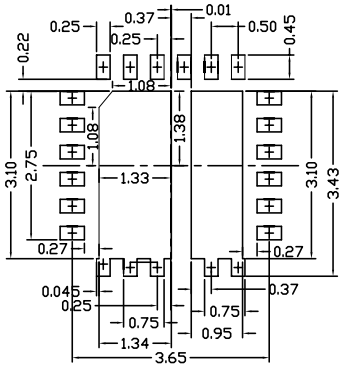
Package Dimensions, QFN4x4-23L



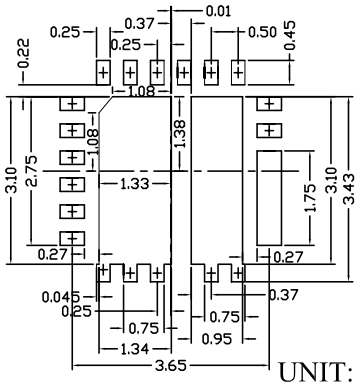


RECOMMENDED LAND PATTERN

Option 1



Option 2



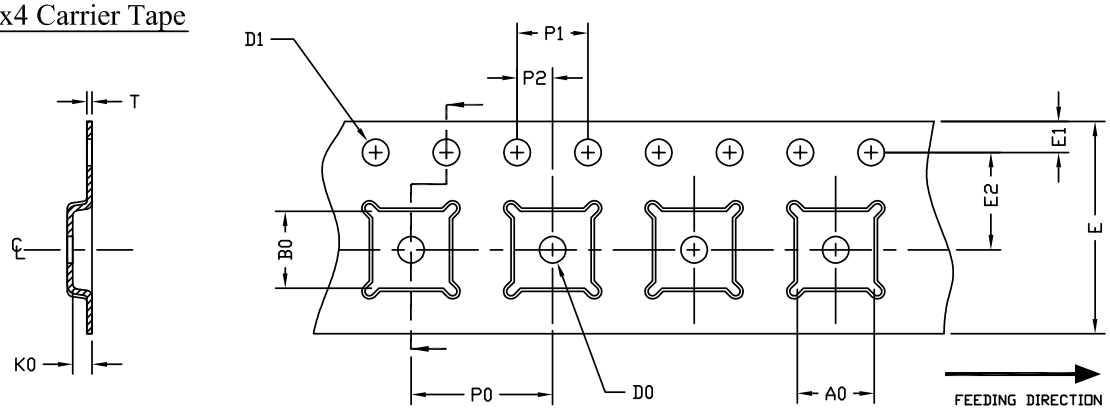
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	---	0.05	0.000	---	0.002
A2		0.2 REF			0.008 REF	
E	3.90	4.00	4.10	0.153	0.157	0.161
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.65	1.75	1.85	0.065	0.069	0.073
E3	2.95	3.05	3.15	0.116	0.120	0.124
D	3.90	4.00	4.10	0.153	0.157	0.161
D1	0.65	0.75	0.85	0.026	0.030	0.034
D2	0.85	0.95	1.05	0.033	0.037	0.041
D3	1.24	1.34	1.44	0.049	0.053	0.057
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.57	0.62	0.67	0.022	0.024	0.026
L2	0.23	0.28	0.33	0.009	0.011	0.013
L3	0.57	0.62	0.67	0.022	0.024	0.026
L4	0.30	0.35	0.40	0.012	0.014	0.016
b	0.20	0.25	0.30	0.008	0.010	0.012
e		0.50 BSC			0.020 BSC	

UNIT: mm

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. TOLERANCE :±0.05 UNLESS OTHERWISE SPECIFIED.
3. RADIUS ON ALL CORNER ARE 0.152 MAX., UNLESS OTHERWISE SPECIFIED.
4. PACKAGE WARPAGE: 0.012 MAX.
5. NO ANY PLASTIC FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
6. PAD PLANARITY: ±0.102
7. CRACK BETWEEN PLASTIC BODY AND LEAD IS NOT ALLOWED.

Tape and Reel Dimensions, QFN4x4-23L

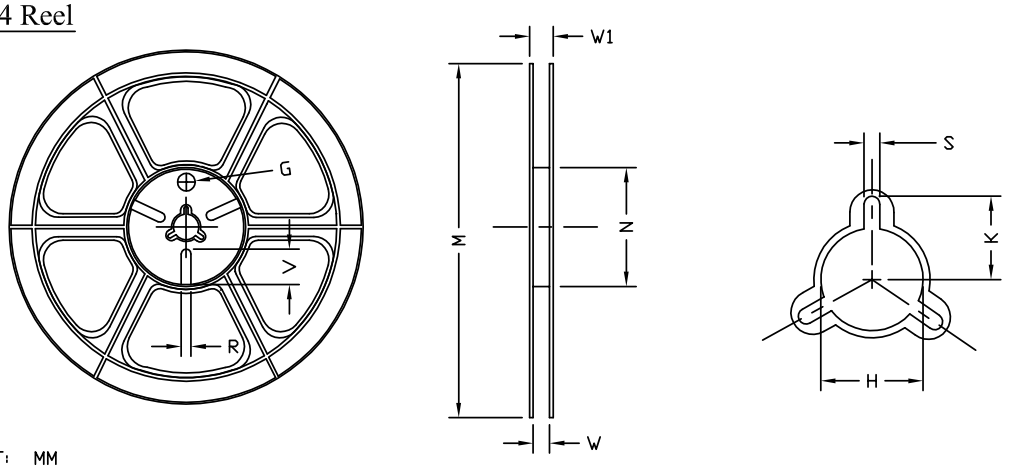
QFN4x4 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 $^{+0.1}_{-0.0}$	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

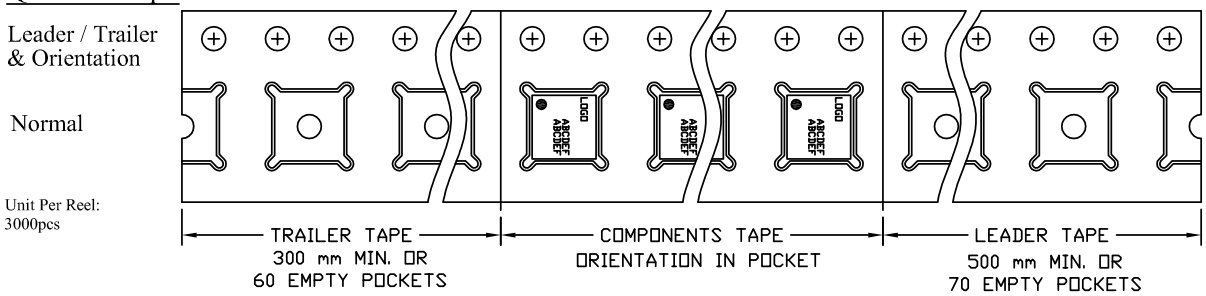
QFN4x4 Reel



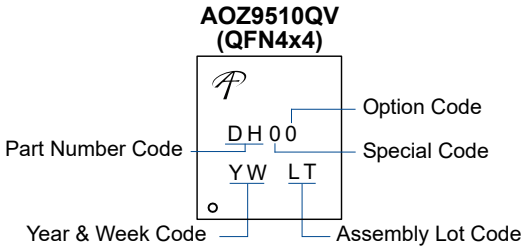
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 $^{+2.0}_{-0.0}$	17.0 $^{+2.6}_{-1.2}$	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

QFN4x4 Tape



Part Marking



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LIFE SUPPORT POLICY

ALPHA AND OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.