AOZ9511QV

28 V/20 A Smart Motor Module

General Description

The AOZ9511QV is an integrated half-bridge gate driver with smart functions. The device includes one half-bridge gate driver, capable of driving high-side and low-side N-channel MOSFETs. Using two AOZ9511QV for single phase motor drivers and three AOZ9511QV for three phase motor drivers.

The device features multiple protection functions such as UVLO and over temperature protection. Moreover, AOZ9511QV provides adjustable gate drive sink and source current control. By using this control, the user can optimize performances of EMI and efficiency.

The AOZ9511QV is available in a 4 mm×4mm QFN-23L package and is rated over a -40°C to +125°C ambient temperature range.

Features

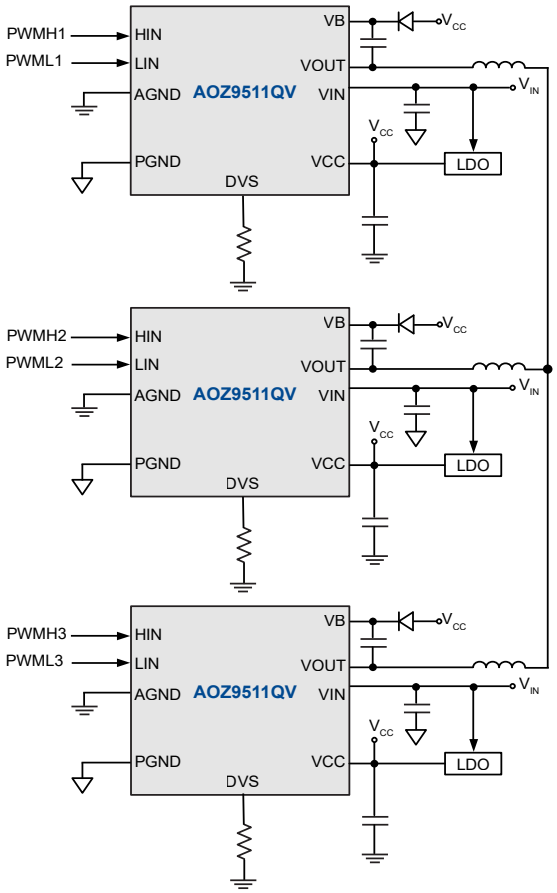
- 3.8 V to 28 V Input voltage range
- 20 A Maximum output current
- Low $R_{DS(ON)}$ internal NFETs
  - 7.5 mΩ for Both HS/LS
- Adjustable slew-rate control to improve Radiation EMI performance
- Build-in protect function – UVLO, OTP
- Thermally enhanced 23-pin 4×4 QFN

Applications

- BLDC motor drive
- Fans and pumps
- Power tools

Green Product

Typical Application



Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ9511QV	-40 °C to +125 °C	23-Pin 4×4 QFN	RoHS

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

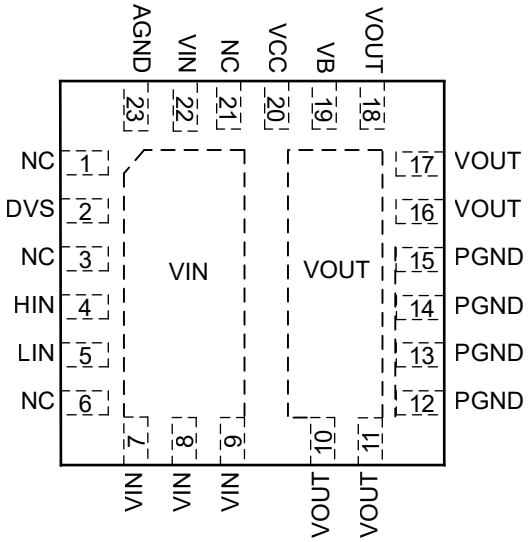


Figure 1. AOZ9511QV 23-Pin 4mm x 4mm QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	NC	No Connect.
2	DVS	Slew-Rate Control to Adjust Driver Speed of Internal MOSFET.
3	NC	No Connect.
4	HIN	PWM Input for High-Side MOSFET.
5	LIN	PWM Input for Low-Side MOSFET.
6	NC	No Connect.
7, 8, 9, 22	VIN	Supply Input. All IN pins must be connected together.
10, 11, 16, 17, 18	VOUT	Switching Node for Half-Bridge. All VOUT must be connected together.
12, 13, 14, 15	PGND	Power Ground.
19	VB	Bootstrap Capacitor Connection. Connect an external capacitor between VB and VOUT for supplying high-side MOSFET.
20	VCC	Supply Input for Analog Functions. Bypass VCC to AGND with a 0.1μF~10μF ceramic capacitor and as close to VCC pin as possible.
21	NC	No Connect.
23	AGND	Analog Ground.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VIN to AGND	-0.3 V to +30 V
VOUT to GND	-0.3 V to +30 V
VB to AGND	-0.3 V to +40 V
VB to VOUT	-0.3 V to +6 V
DVS, VCC to AGND	-0.3 V to +6 V
PGND to AGND	-0.3 V to +1 V
Junction Temperature (T_J)	+150 °C
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating	±2 kV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	3.8 V to 28 V
Supply Voltage (V_{CC})	4.75 V to 5.5 V
Ambient Temperature (T_A)	-40 °C to +125 °C
Package Thermal Resistance (ΘJC) (ΘJA)	 0.6 °C/W 40°C/W

Electrical Characteristics

T_A = -40 °C to +125 °C, unless otherwise specified.

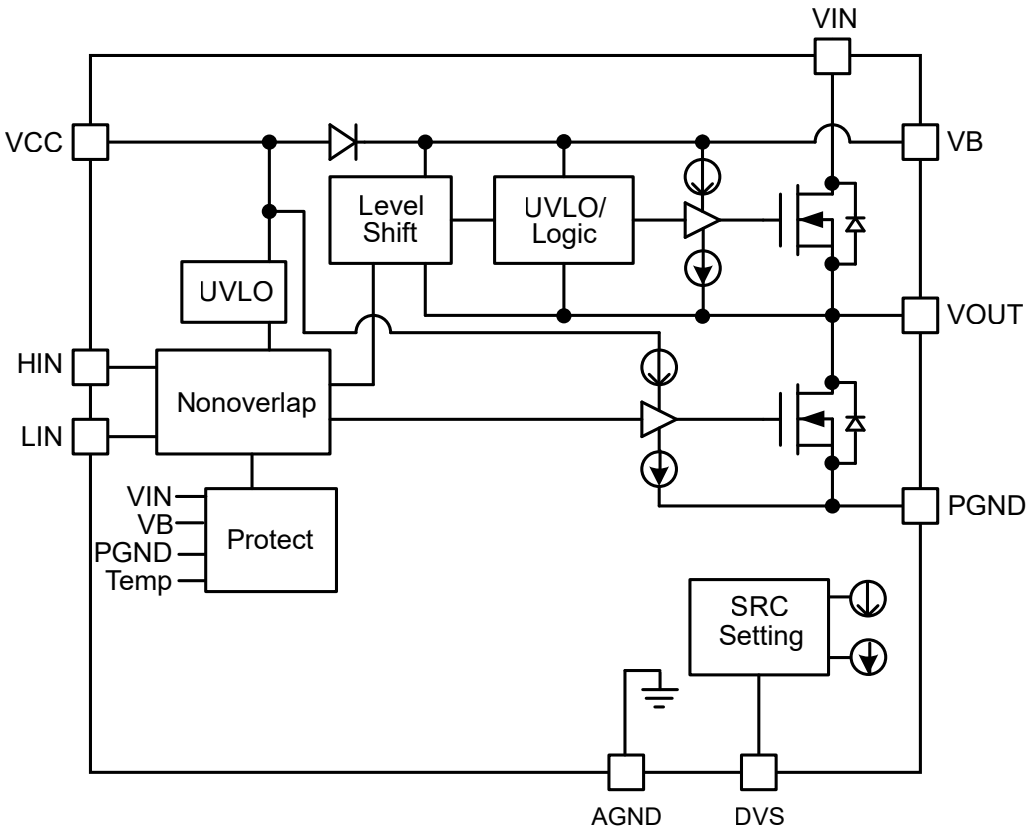
Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
V_{UVLO_R}	V_{CC} UVLO Rising	VIN = 12 V, VCC increase, Monitor DVS from low to high		4.3		V
V_{UVLO_F}	V_{CC} UVLO Falling	VIN = 12 V, VCC decrease, Monitor DVS from high to low		4.2		V
VB_{UVLO_R}	VB-VOUT UVLO Rising	VIN = 20 V, (VB -VOUT) increase, Monitor VOUT from low to high		4.3		V
VB_{UVLO_F}	VB-VOUT UVLO Falling	VIN = 20 V, (VB -VOUT) decrease, Monitor VOUT from high to low		4.2		V
I_{VIN_QC}	I_{VIN} Quiescent Current	VIN = 12V, VCC = 5 V, HIN = LIN = 0 V, DVS = 100 kΩ		20		µA
I_{VCC_QC}	I_{VCC} Quiescent Current	VIN = 12 V, VCC = 5 V, HIN = LIN = 0 V, DVS = 100 kΩ		180		µA
$I_{VB\text{-}VOUT\_QC}$	$I_{VB\text{-}VOUT}$ Quiescent Current	HIN/LIN = 0 V, VOUT = 1 V, (VB-VOUT) = 5 V,			40	mA
V_{HLIN_L}	HIN/LIN Logic Low Voltage	VIN = 12 V	0.7	0.9	1.1	V
V_{HLIN_H}	HIN/LIN Logic High Voltage	VIN = 12 V	1.2	1.4	1.6	V
R_{HLIN_IN}	HIN/LIN Input Pull Low Impedance			280		kΩ
t_{HIN_RP}	HIN Rising Propagation Delay	VIN = 10 V, VCC = 5 V, DVS = 20 kΩ, VOUT to GND = 100 Ω, HIN = Low to High, Monitor VOUT Low to High	62	87	110	ns
t_{HIN_FP}	HIN Falling Propagation Delay	VIN = 10 V, VCC = 5 V, DVS = 20 kΩ, VOUT to GND = 100 Ω, HIN = High to Low, Monitor VOUT High to Low	60	86	110	ns
t_{LIN_RP}	LIN Rising Propagation Delay	VIN = 10 V, VCC = 5 V, DVS = 20 kΩ, VOUT to GND = 100 Ω, LIN = Low to High, Monitor VOUT High to Low	72	91	105	ns
t_{LIN_FP}	LIN Falling Propagation Delay	VIN = 10 V, VCC = 5 V, DVS = 20 kΩ, VOUT to GND = 100 Ω, LIN = High to Low, Monitor VOUT Low to High	50	75	95	ns

Electrical Characteristics

T_A = -40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DM_R}	Delay Matching Rising	Difference between t_{HIN_RP} and t_{LIN_RP}		4		ns
T_{DM_F}	Delay Matching Falling	Difference between t_{HIN_FP} and t_{LIN_FP}		11		ns
V_{DVS}	DVS	VIN = 12 V, VCC = 5 V, DVS = 20 kΩ	0.97	1	1.03	V
I_{DVS_MIN}	DVS Min. Source Current	VIN = 12 V, VCC = 5 V, DVS = 4 V		0.5		µA
I_{DVS_MAX}	DVS Max. Source Current	VIN = 12 V, VCC = 5 V, DVS = 0.8 V		140		µA
SR_{HIN_R}	HIN Rising Slew Rate (DVS = 20 kΩ)	VIN = 10 V, VCC = 5 V, VOUT to GND = 100 Ω, HIN = Low to High, Monitor VOUT Rising Slew Rate		0.4		V/ns
SR_{HIN_F}	HIN Falling Slew Rate (DVS = 20 kΩ)	VIN = 10 V, VCC = 5 V, VOUT to GND = 100 Ω, HIN = High to Low, Monitor VOUT Falling Slew Rate		0.05		V/ns
SR_{LIN_R}	LIN Rising Slew Rate (DVS = 20 kΩ)	VIN = 10 V, VCC = 5 V, VOUT to VIN = 100 Ω, LIN = High to Low, Monitor VOUT Rising Slew Rate		0.5		V/ns
SR_{LIN_F}	LIN Rising Slew Rate (DVS = 20 kΩ)	VIN = 10 V, VCC = 5 V, VOUT to VIN = 100 Ω, LIN = Low to High Monitor VOUT Falling Slew Rate		0.4		V/ns
R_{H_ON}	VIN-VOUT R_{ON}	VIN = 12 V, VCC = 5 V, HIN = 5 V, (VB -VOUT) = 5V, I_{VOUT} = 1 A		7.5		mΩ
R_{L_ON}	VOUT-PGND R_{ON}	VIN = 12 V, VCC = 5 V, LIN = 5 V, PGND = 0, I_{VOUT} = 1 A		7.5		mΩ
V_{SD}	Boost Diode Forward Voltage	Forward Current = 2 mA		0.42		V
T_{OTP}	OTP	VIN = 12 V, VCC = 5 V		150		°C

Functional Block Diagram



Timing Diagram

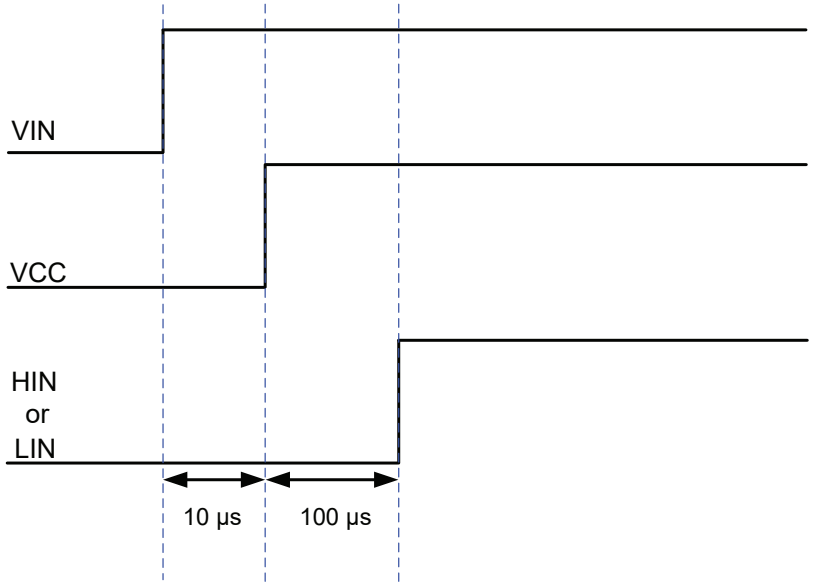


Figure 2. Start-up Sequence

Typical Characteristics

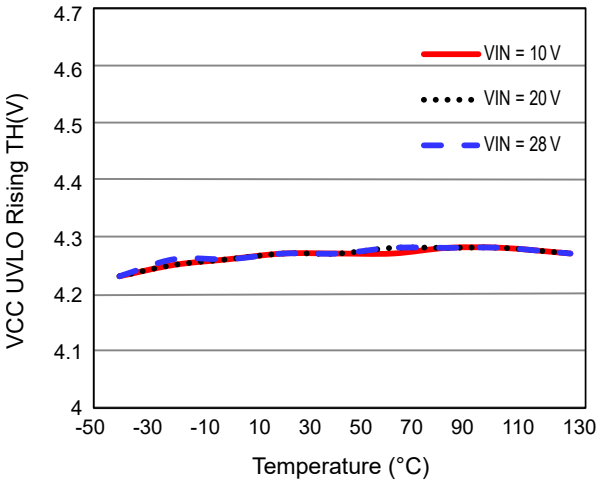


Figure 3. VCC UVLO Rising Threshold

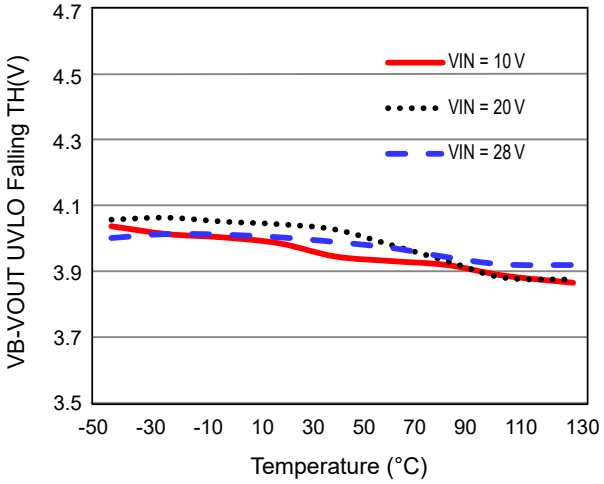


Figure 4. VB-VOUT UVLO Falling Threshold

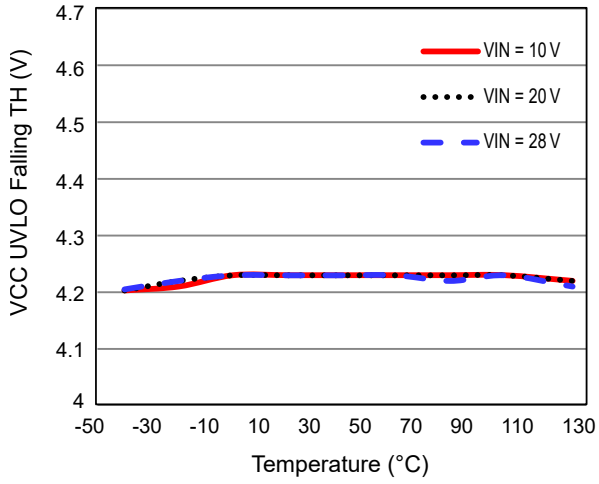


Figure 5. VCC UVLO Falling Threshold

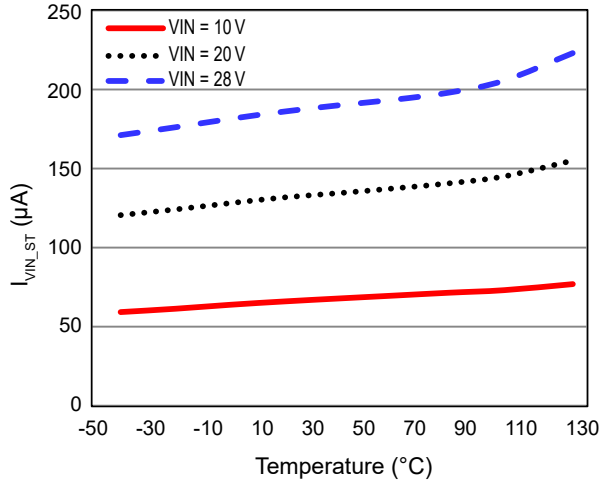


Figure 6. Input Standby Current

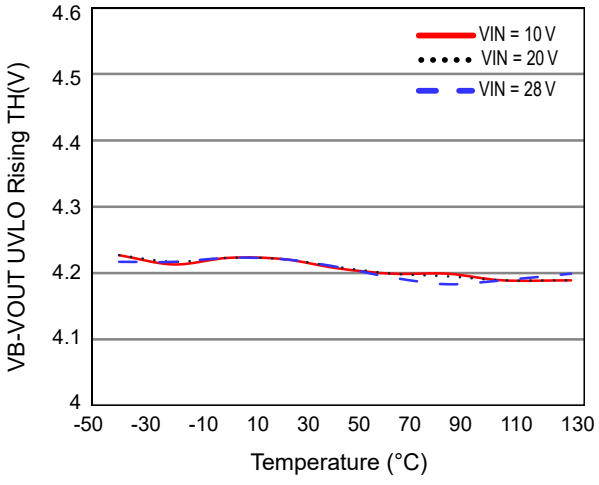


Figure 7. VB-VOUT UVLO Rising Threshold

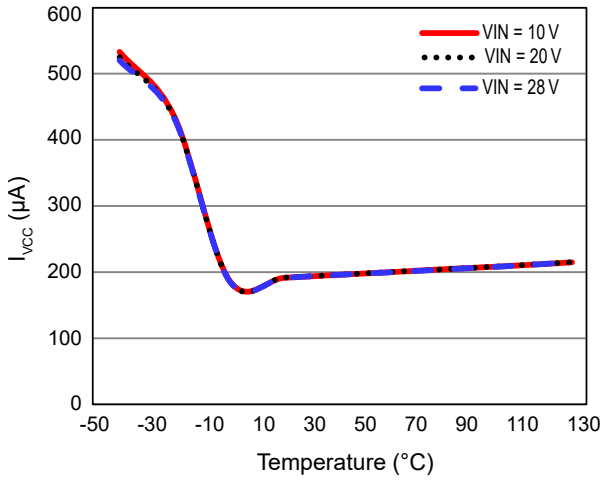


Figure 8. VCC Standby Current

Typical Characteristics *(Continued)*

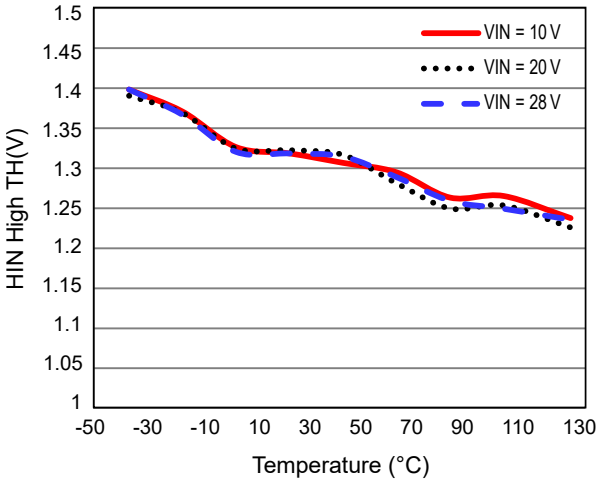


Figure 9. HIN High Threshold

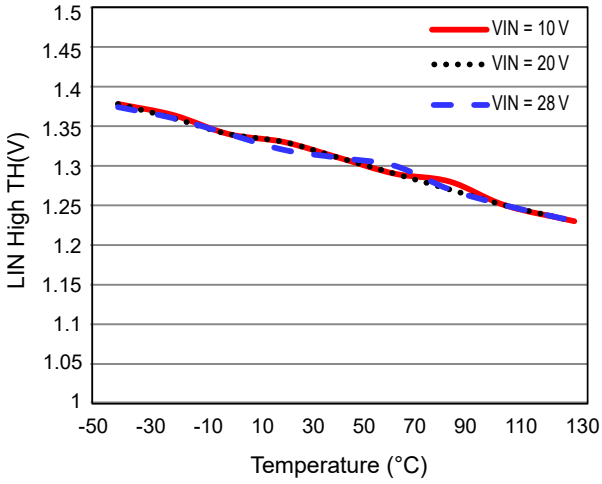


Figure 10. LIN High Threshold

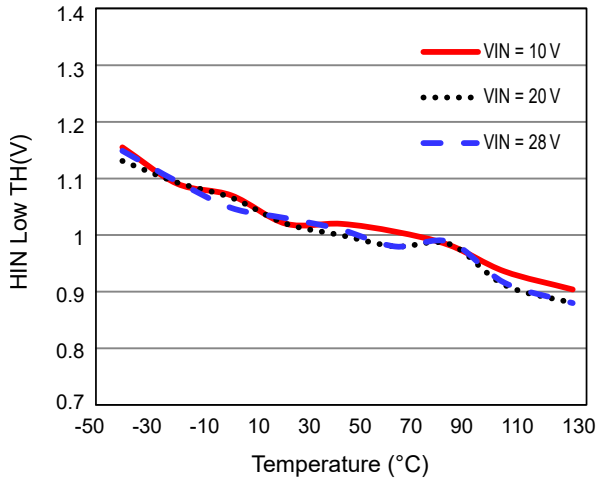


Figure 11. HIN Low Threshold

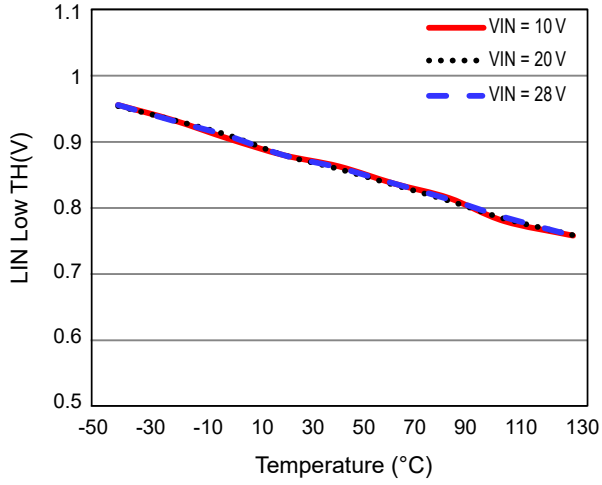


Figure 12. LIN Low Threshold

Detailed Description

The AOZ9511QV is an integrated half-bridge gate driver for motor drive applications. The device includes one half-bridge gate driver, capable of driving high-side and low-side N-channel MOSFETs. The AOZ9511QV provides adjustable source/sink current of both high/low-side gate drive output current which can optimize performances of EMI and efficiency on different PCB layout and applications.

The AOZ9511QV provides adjustable gate drive sink and source current control, by doing this control methodology, it's able to optimize EMI and driver losses to improve overall efficiency performance.

In addition, the AOZ9511QV provides several fault protections, such as UVLO, OTP and non-overlapping mechanism.

The AOZ9511QV is available in a 23-pin 4mm×4mm QFN package.

Non-overlapping

For forbidding shoot-through, HIN or LIN is invalid when HIN or LIN goes high state before other one. For example, low-side gate state keeps low regardless of the state of LIN when HIN is high at first, and vice versa.

Fault Protection

In order to protect power MOSFETs, over temperature protection (OTP) is implemented. AOZ9511QV will be shutdown when OTP is occurred until VCC is reset. The threshold of OTP is 140°C.

Adjustable Source/Sink Current

It's hard to meet all of EMI specifications in different applications. So, AOZ9511QV provides external adjustable resistors for tuning gate drive source and sink current.

DVS is used to tune gate drive source and sink current, respectively. A resistor connects between DVS pin and GND to setting gate drive source/sink current by internal current mirror, as illustrated Figure 13. Source and sink current use maximum capability to drive when DVS pin is floating or the voltage on DVS pin exceeds 4 V. The suggestion range of R_{DVS} is 10 kΩ~100 kΩ.

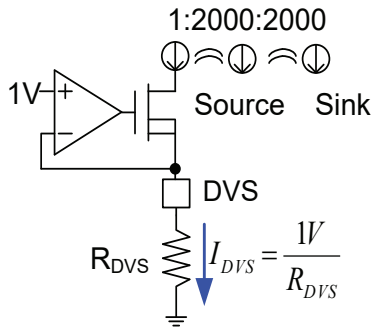


Figure 13. Source/Sink Current Setting

In addition, source and sink current controls are implemented only during MOSFET Miller effect and V_{GS} >1 V, as illustrated in Figure 14.

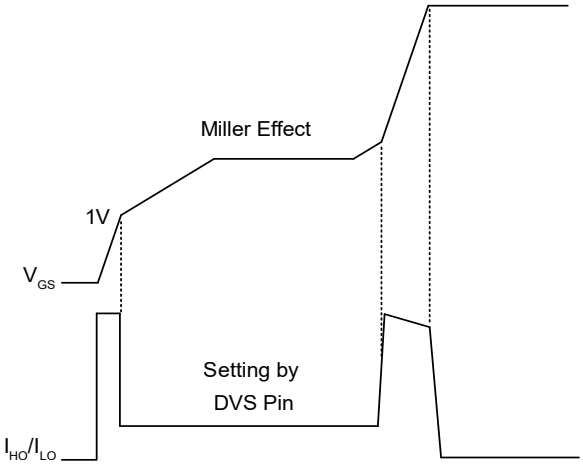


Figure 14. Source/Sink Current Implement Waveform

Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

1. The VIN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to VIN pins to help thermal dissipation.
2. Input capacitors should be connected to the VIN pins and the PGND pins as close as possible to reduce the switching spikes.
3. The VOUT pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connected a large copper plane to VOUT pins to help thermal dissipation.
4. Decoupling capacitor C_{VCC} should be connected to VCC and AGND as close as possible.
5. Bootstrap capacitor C_B should be connected to VB and VOUT as close as possible.A ground plane is preferred. PGND and AGND must be connected to the ground plane through vias.
6. A ground plane is preferred. PGND and AGND must be connected to the ground plane through vias
7. Keep sensitive signal traces such as feedback trace and digital signals far away from the VOUT pins.

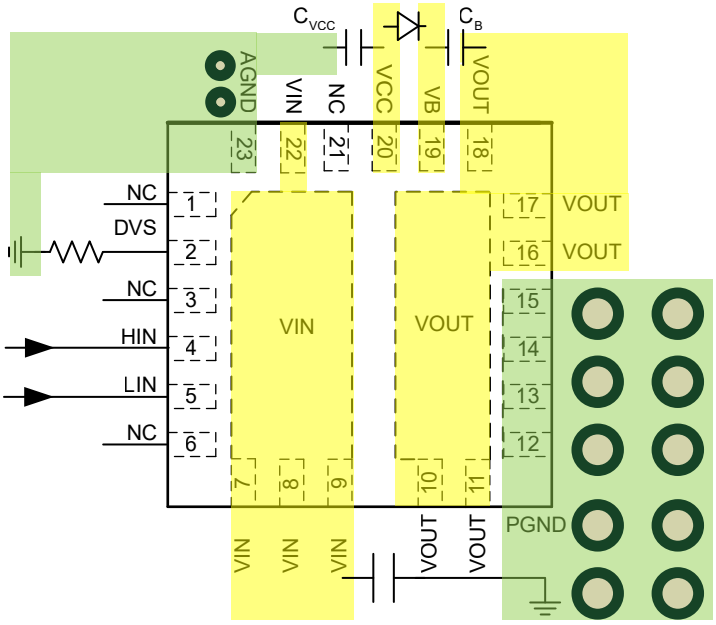
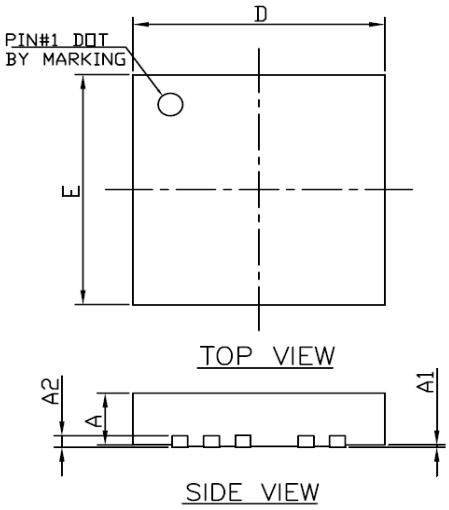
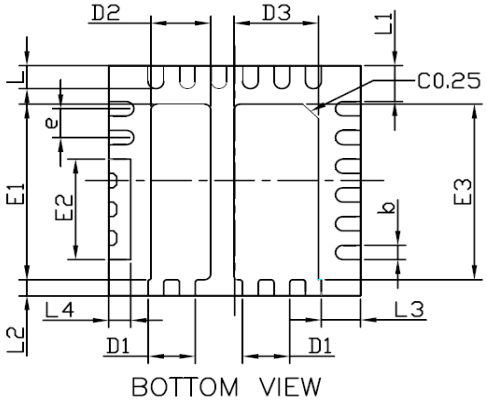


Figure 15. Layout Placement

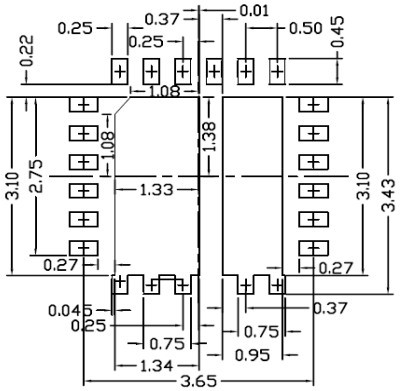
Package Dimensions, QFN 4x4-23L



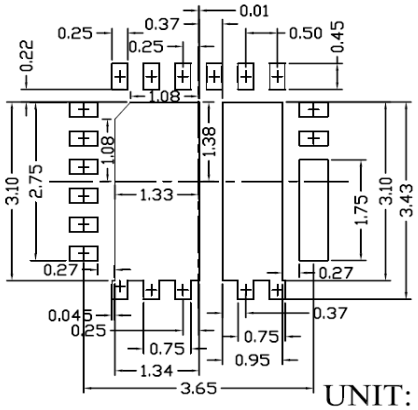


RECOMMENDED LAND PATTERN

Option 1



Option 2



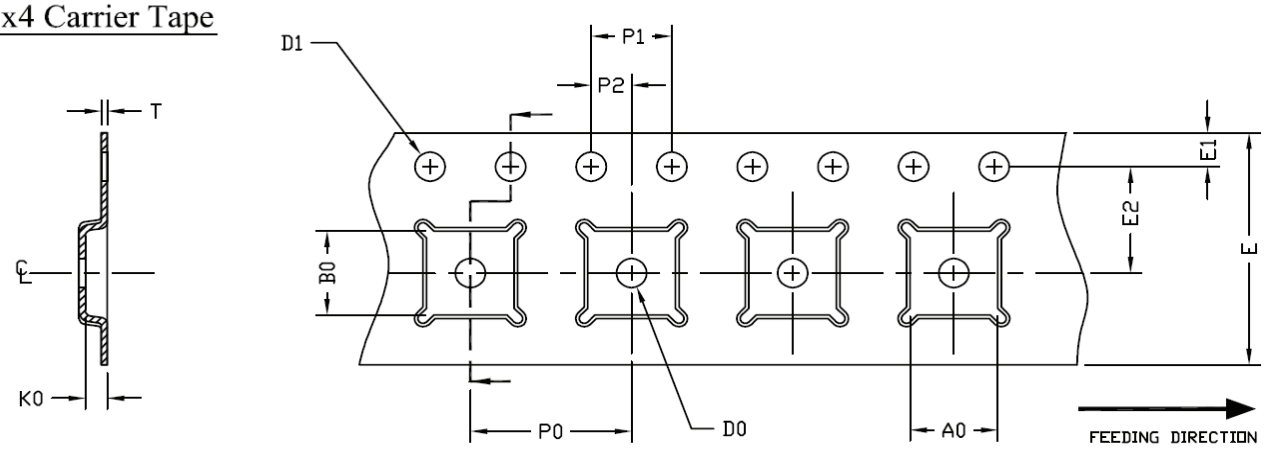
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	—	0.05	0.000	—	0.002
A2		0.2 REF			0.008 REF	
E	3.90	4.00	4.10	0.153	0.157	0.161
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.65	1.75	1.85	0.065	0.069	0.073
E3	2.95	3.05	3.15	0.116	0.120	0.124
D	3.90	4.00	4.10	0.153	0.157	0.161
D1	0.65	0.75	0.85	0.026	0.030	0.034
D2	0.85	0.95	1.05	0.033	0.037	0.041
D3	1.24	1.34	1.44	0.049	0.053	0.057
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.57	0.62	0.67	0.022	0.024	0.026
L2	0.23	0.28	0.33	0.009	0.011	0.013
L3	0.57	0.62	0.67	0.022	0.024	0.026
L4	0.30	0.35	0.40	0.012	0.014	0.016
b	0.20	0.25	0.30	0.008	0.010	0.012
e		0.50 BSC			0.020 BSC	

UNIT: mm

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. TOLERANCE :±0.05 UNLESS OTHERWISE SPECIFIED.
3. RADIUS ON ALL CORNER ARE 0.152 MAX., UNLESS OTHERWISE SPECIFIED.
4. PACKAGE WARPAGE: 0.012 MAX.
5. NO ANY PLASTIC FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
6. PAD PLANARITY: ±0.102
7. CRACK BETWEEN PLASTIC BODY AND LEAD IS NOT ALLOWED.

Tape and Reel Dimensions, QFN 4x4-23L

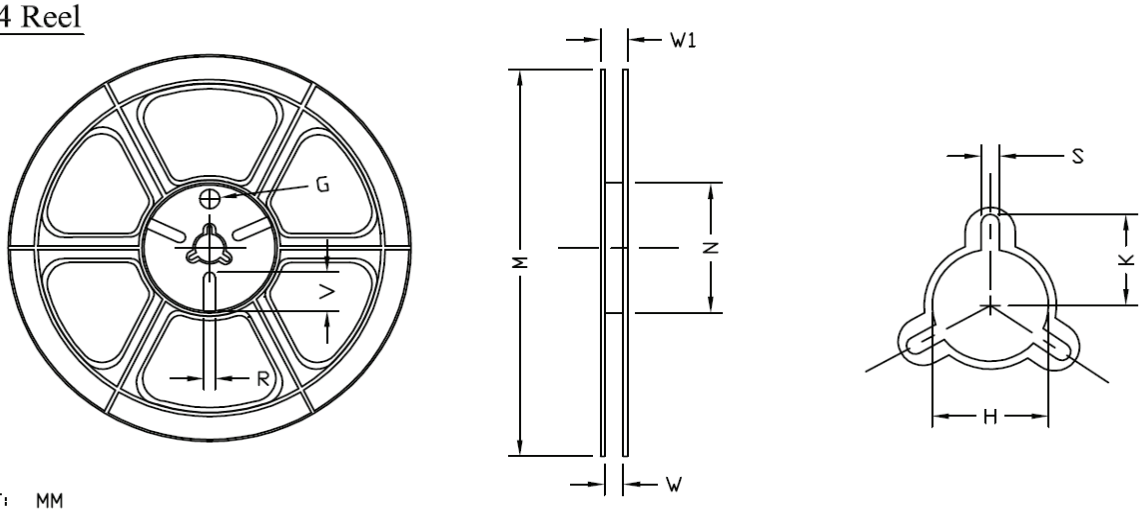
QFN4x4 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN4x4 Reel



UNIT: MM

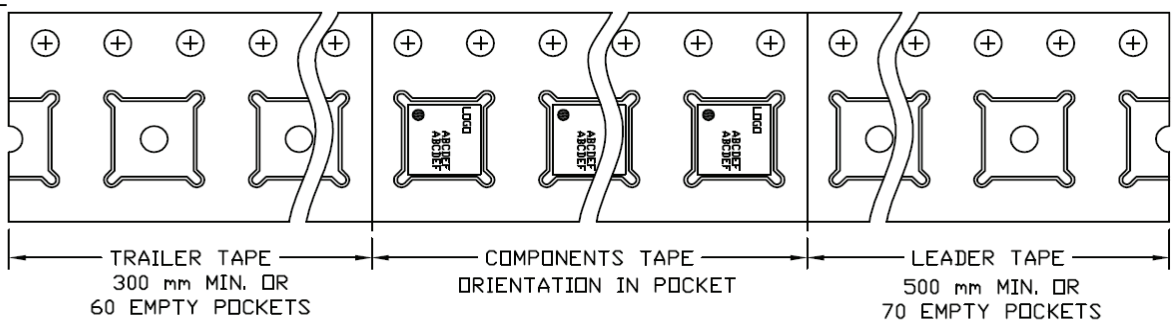
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

QFN4x4 Tape

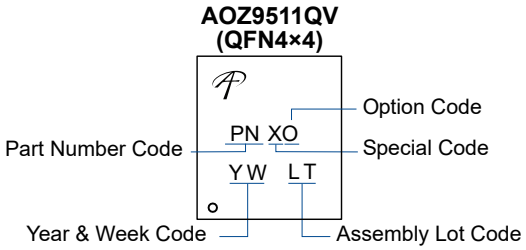
Leader / Trailer & Orientation

Normal

Unit Per Reel: 3000pcs



Part Marking



Part Number	Description	Code
AOZ9511QV	Green Product	DT00

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