

**General Description**

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Integrated Schottky Diode (SRFET) on Low-Side
- Very Low  $R_{DS(on)}$  at 4.5V  $V_{GS}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

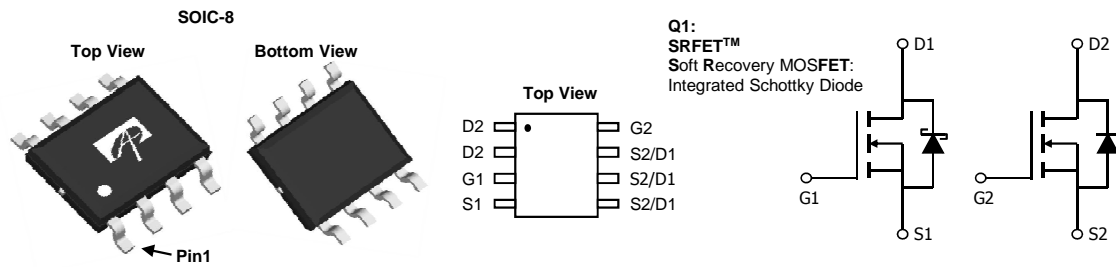
**Application**

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

**Product Summary**

	Q1	Q2
$V_{DS}$	30V	30V
$I_D$ (at $V_{GS}=10V$ )	11A	11A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	<10.5mΩ	<11.5mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	<15.5mΩ	<16.5mΩ

100% UIS Tested  
 100% Rg Tested


**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage	$V_{DS}$	30		V
Gate-Source Voltage	$V_{GS}$	±20	±20	V
Continuous Drain Current	$I_D$	$T_A=25^\circ C$	11	A
		$T_A=70^\circ C$	9	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	75	74	A
Avalanche Current <sup>C</sup>	$I_{AS}$	18	15	A
Avalanche Energy $L=0.1mH$ <sup>C</sup>	$E_{AS}$	16	11	mJ
$V_{DS}$ Spike	$V_{SPIKE}$	36	36	V
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	2	W
		$T_C=70^\circ C$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		°C

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient <sup>A D</sup>		Steady-State	74	
Maximum Junction-to-Case	$R_{\theta JL}$	32	40	°C/W

**Q1 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =10mA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			0.5 100	mA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.4	1.8	2.5	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =11A T <sub>J</sub> =125°C		8.3 11.8	10.5 15	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =9A		12.2	15.5	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =11A		52		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =0.2A, V <sub>GS</sub> =0V		0.45	0.65	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance			605		pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		275		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			37		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1	2	3	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =11A		10.2	15	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			4.9	8	nC
Q <sub>gs</sub>	Gate Source Charge			2		nC
Q <sub>gd</sub>	Gate Drain Charge			2.3		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =1.36Ω, R <sub>GEN</sub> =3Ω		5		ns
t <sub>r</sub>	Turn-On Rise Time			3		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			17.5		ns
t <sub>f</sub>	Turn-Off Fall Time			3		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =11A, dI/dt=500A/μs		11		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =11A, dI/dt=500A/μs		12.5		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current limited by package.

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**Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

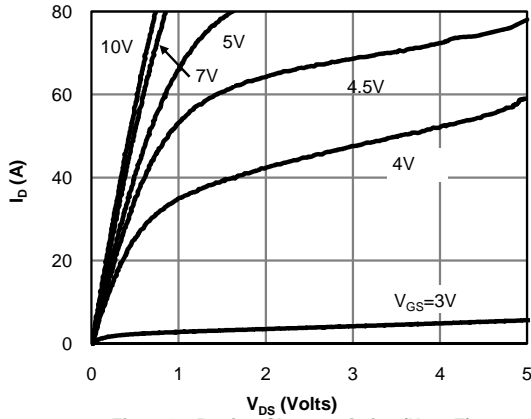


Figure 1: On-Region Characteristics (Note E)

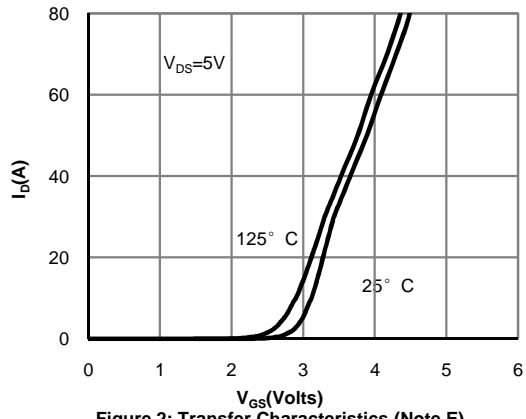


Figure 2: Transfer Characteristics (Note E)

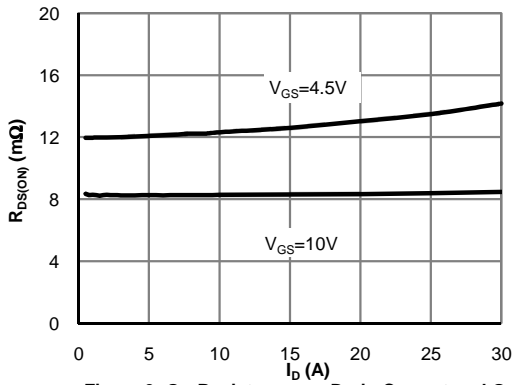


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

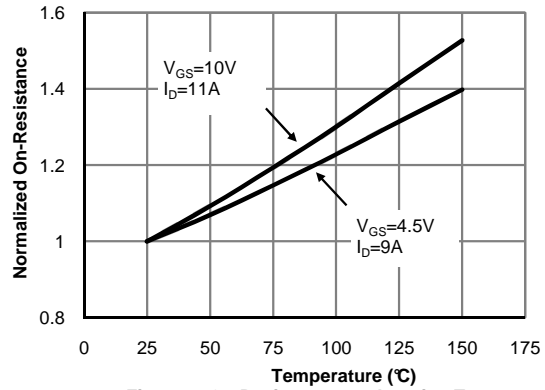


Figure 4: On-Resistance vs. Junction Temperature (Note E)

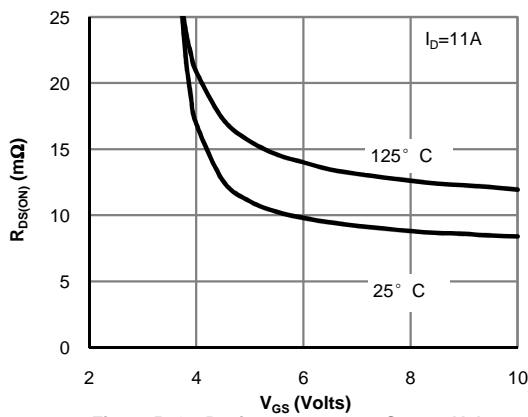


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

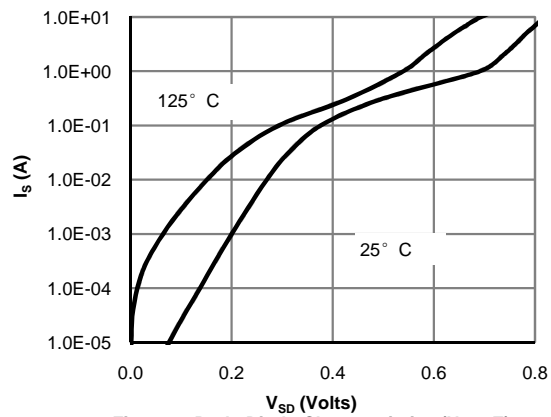


Figure 6: Body-Diode Characteristics (Note E)

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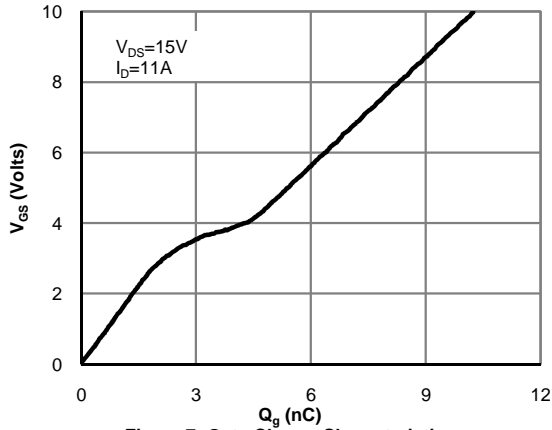


Figure 7: Gate-Charge Characteristics

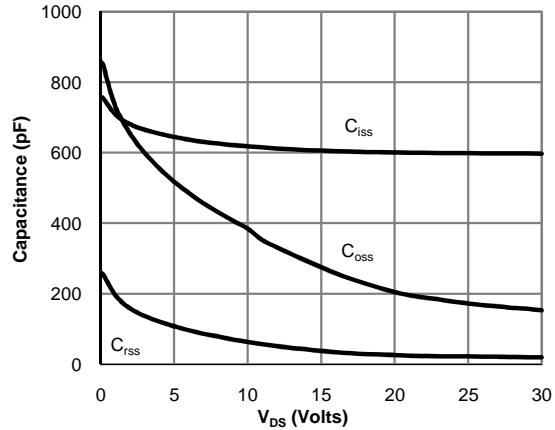
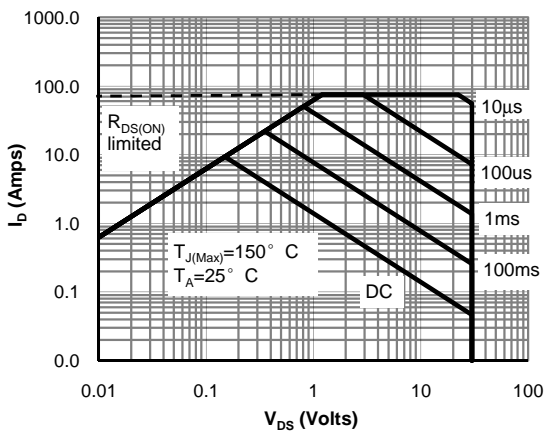


Figure 8: Capacitance Characteristics



VGS > or equal to 4.5V  
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

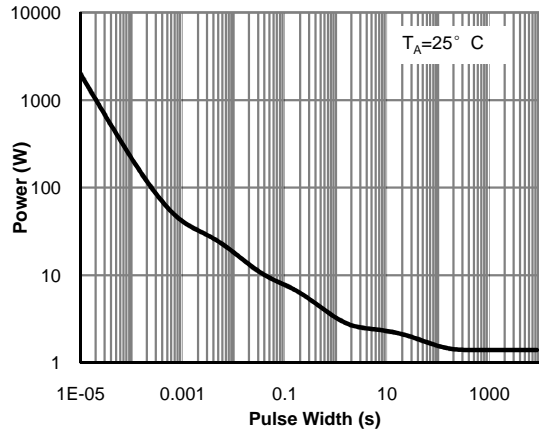


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

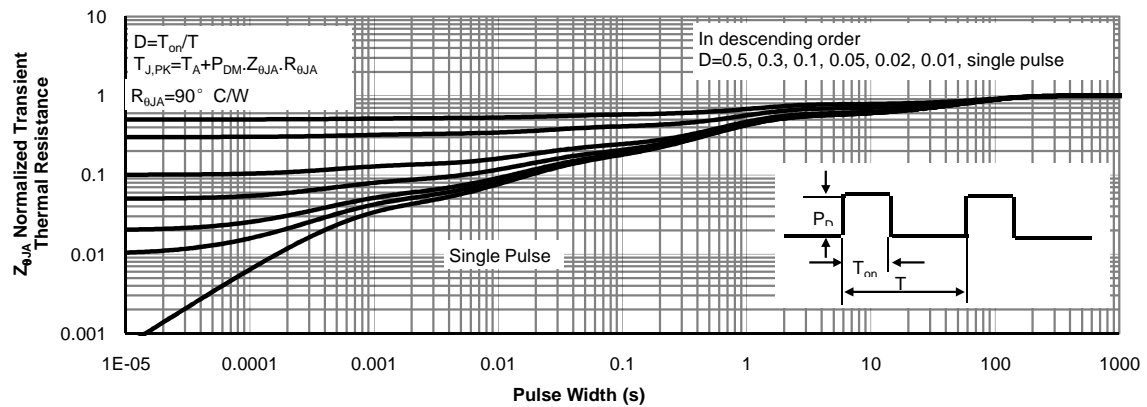


Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

**Q2 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.4	1.8	2.2	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =11A T <sub>J</sub> =125°C		9	11.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =9A		12.8	16.5	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =11A		40		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.72	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance			542		pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		233		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			31		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1	2	3	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =11A		9	12.5	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			4.3	6	nC
Q <sub>gs</sub>	Gate Source Charge			2.2		nC
Q <sub>gd</sub>	Gate Drain Charge			1.7		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =1.36Ω, R <sub>GEN</sub> =3Ω		4		ns
t <sub>r</sub>	Turn-On Rise Time			3.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			18		ns
t <sub>f</sub>	Turn-Off Fall Time			3		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =11A, dI/dt=500A/μs		9.7		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =11A, dI/dt=500A/μs		11.5		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.

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**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

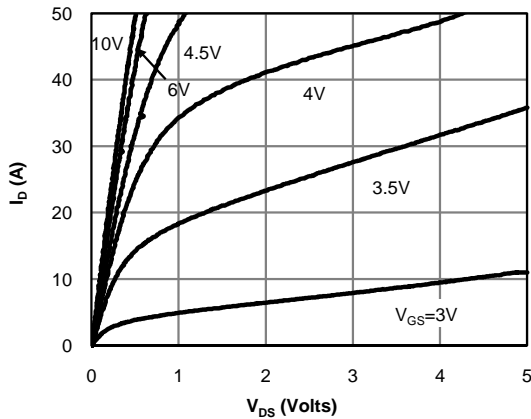


Fig 1: On-Region Characteristics (Note E)

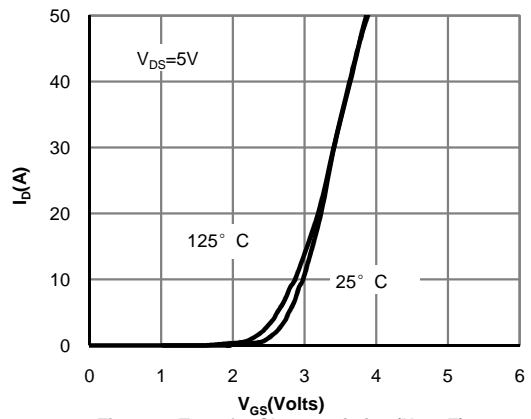


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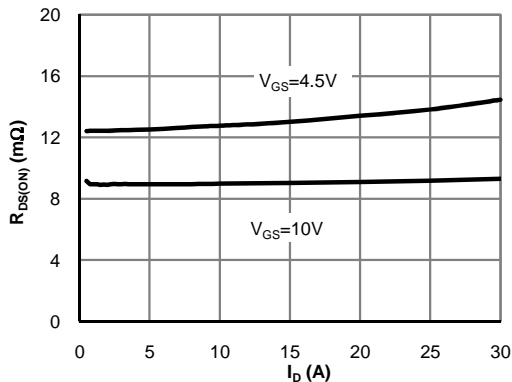


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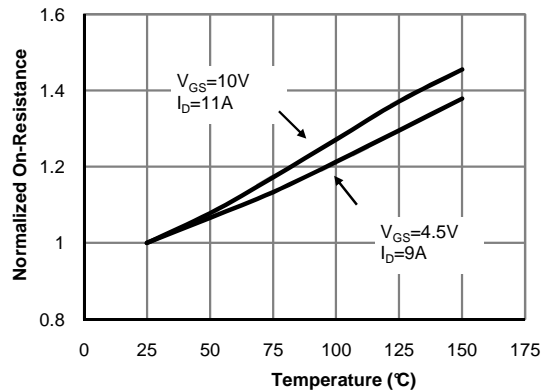


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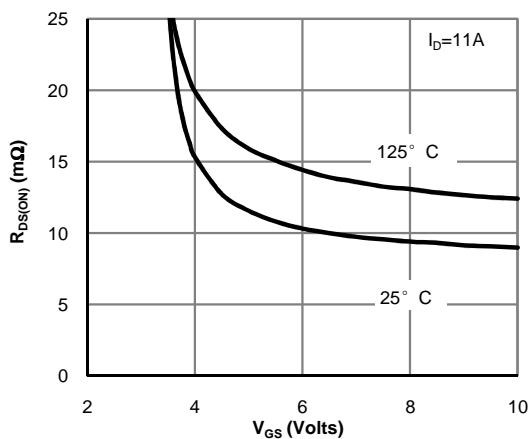


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

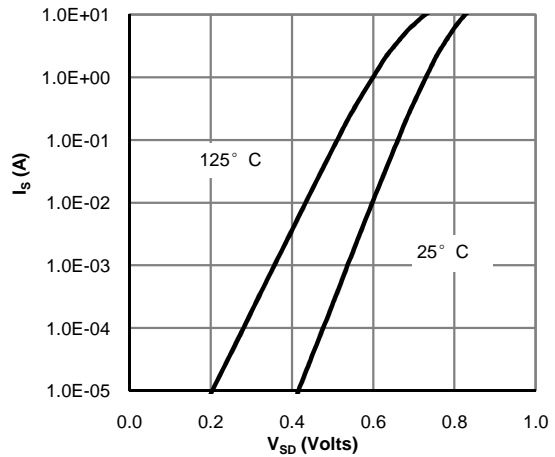


Figure 6: Body-Diode Characteristics (Note E)

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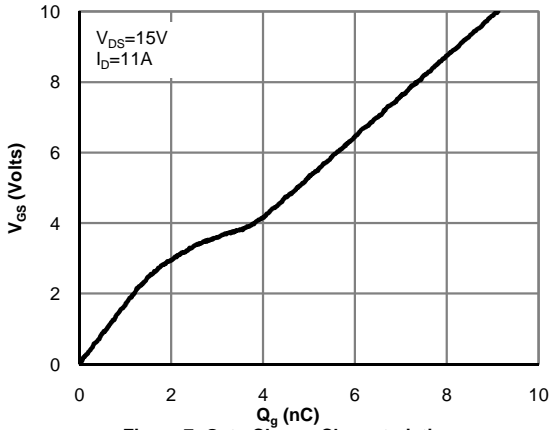


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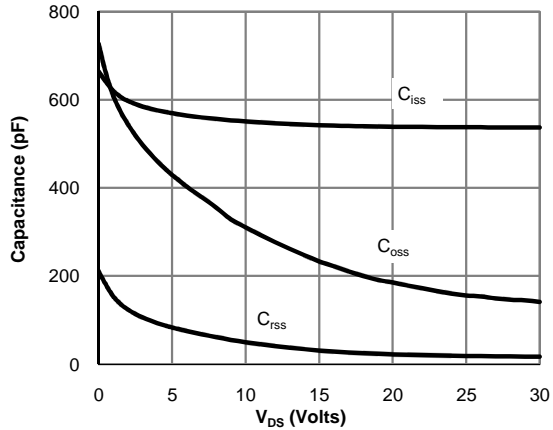


Figure 8: Capacitance Characteristics

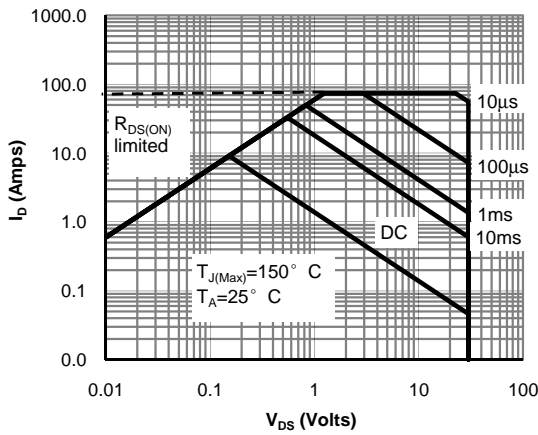


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

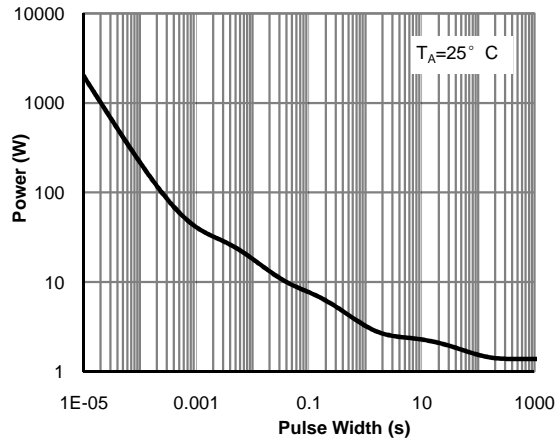


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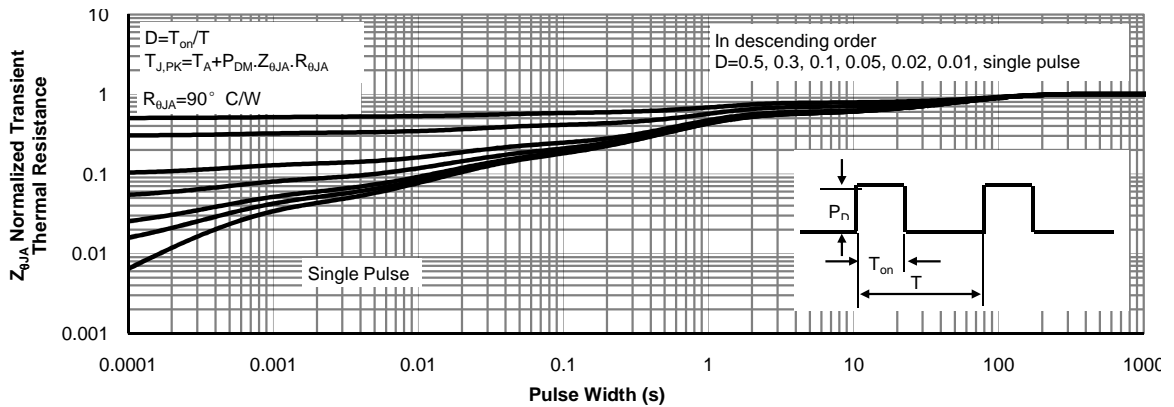
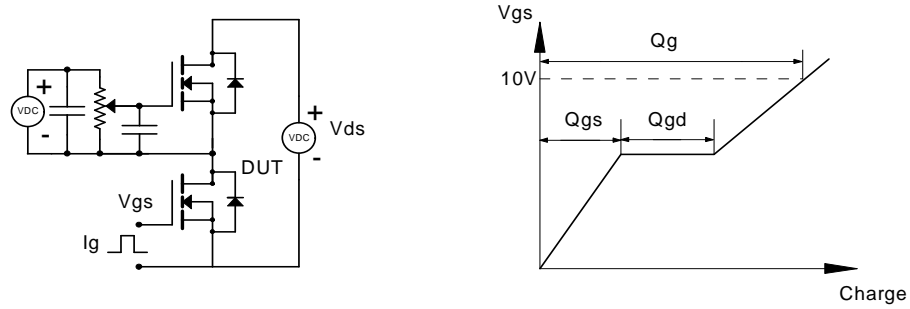
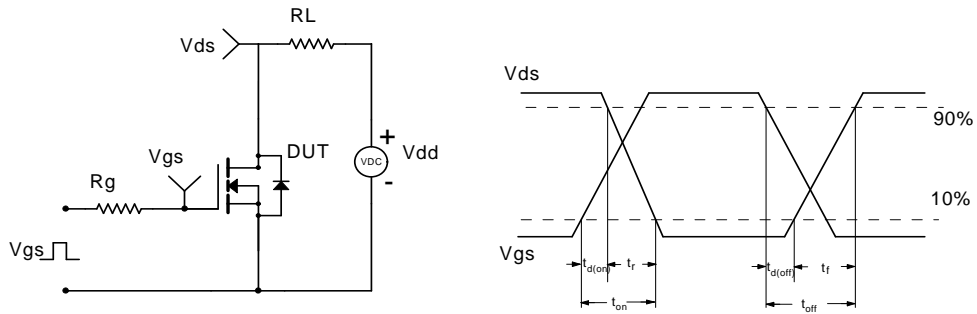


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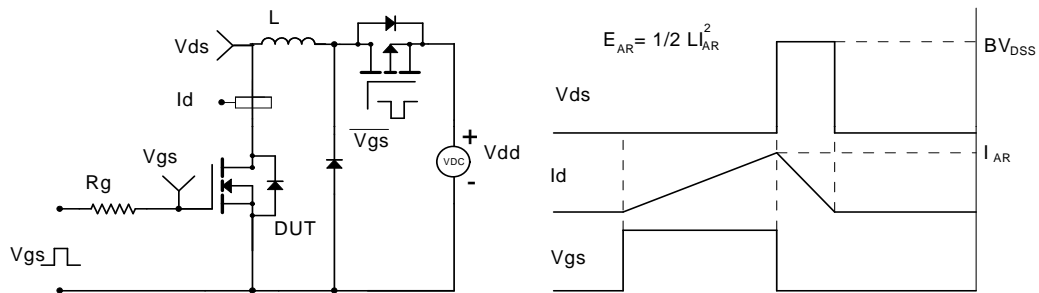
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

