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A Novel ESD Super-Clamp Structure for TVS Applications

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***Abstract*- This paper presents a new ESD clamp structure for Transient Voltage Suppressor (TVS) applications that combines the advantages of avalanche diode and bipolar transistor clamps. The device structure consists of a non-snapback avalanche diode triggered vertical NPN transistor. The avalanche diode provides the fast trigger and current conduction path at low currents, while the vertical NPN bipolar transistor turn-on provides alternate low resistance path for current conduction at high currents. The snapback in the IV characteristics is minimized by matching the avalanche diode breakdown voltage V_{BD} and the vertical NPN transistor open base collector-emitter breakdown voltage, BV_{CEO}. Measurements on fabricated devices show consistent results with the theory. The TVS has low leakage currents (<25nAmps), negligible snapback in the output characteristics (<0.5 Volts) and excellent clamping voltage at high currents (13.1 Volts @ 30 Amps of TLP current). The presence of low doped base region also results in 35% decrease in the TVS capacitance.**

I. INTRODUCTION

Transient Voltage Suppressors (TVS) are commonly used for protecting integrated circuits on system level from damages resulting from electrostatic discharge (ESD), electrical fast transients (EFT) and secondary lightning. The TVS absorbs the transient energy by diverting all the current through itself and clamping the node voltage. However, the scaling of IC technology has made the ICs more sensitive to these external disturbances and thus requires better performance from the TVS that protects it [1], [2]. In addition to absorbing the transient energy, the TVS is required to achieve fast response time, low clamping voltage at high currents, and low parasitic capacitance.

In general, there are two categories of ESD clamp structures used to make TVS. The first type includes reverse biased P-N junction diodes that undergo avalanche breakdown at voltages that are typically 10-20% higher than the absolute maximum voltage. These devices have a fast response time, no snap-back in their output characteristics and require simple fabrication process. However, these devices suffer from high clamping voltages at high currents due to higher resistivity of the lightly doped region and lack of conductivity modulation in the avalanche diode. The second type of TVS structures which are also used extensively for on-chip IO protection consist of bipolar transistors and CMOS/bipolar triggered SCR circuits[3].These devices typically have snap-back in their output characteristics resulting from bipolar/SCR turn. Minority carrier injection from bipolar turn on results in lower clamping voltages and higher current handling capabilities for these devices. However snap-back is an undesirable feature of TVS that requires the addition of current limiting resistors in the circuit that may once again increase the node clamping voltage at high currents. In addition, the fabrication of these ESD clamp circuits requires a more complex CMOS/Bi-CMOS type of process.

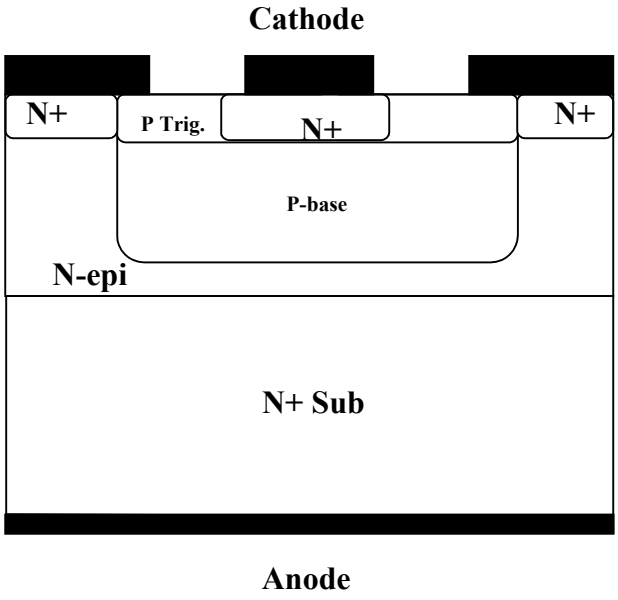

Figure 1. Cross-section of the non-snapback avalanche diode trigged bipolar transistor ESD Super-Clamp TVS

In this paper, we present a new ESD clamp structure that combines the advantages of both types of ESD clamp structures mentioned above. This ESD clamp consist of a non-snapback avalanche diode triggered bipolar transistor [4]. This

device has a single stage with avalanche triggering, thereby providing a fast response time. It also consists of bipolar transistor that turns on at high current without snap-back and provides excellent clamping at high currents. In addition, this device structure can be fabricated using a simple bipolar process.

II. DEVICE STRUCTURE AND OPERATION

Figures 1 and 2 show the cross section of the proposed ESD clamp structure and its equivalent circuit respectively. The device consists of a vertical NPN transistor, whose collector-base junction also serves as an avalanche diode used to trigger the NPN. The N+ substrate forms the emitter of the vertical NPN transistor which is the ESD clamp anode terminal. The P doped region diffused in the N-epi forms the base of the NPN

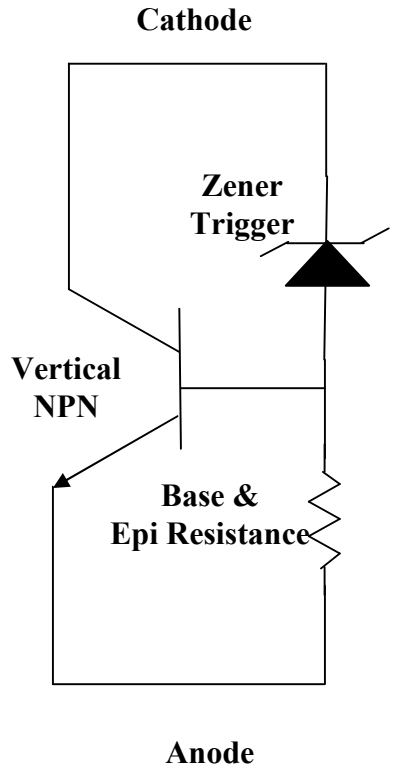

Figure 2. Equivalent Circuit of the non-snapback avalanche diode triggered bipolar transistor ESD Super-Clamp TVS

transistor as well as the anode of the avalanche diode. An ohmic contact is formed between the P body and the substrate (anode terminal) by using shallow P+ implants in the P Base region and N+ implants in N-epi and connecting the two with Metal on the top surface. The series resistance shown in the equivalent circuit consists of the P Base sheet resistance and the N-epi region series resistance. The shallow N+ region on top is the collector of the NPN transistor, as well as the cathode of the avalanche diode. This region is contacted to form the cathode terminal of the ESD clamp.

For all positive voltages less than the avalanche diode breakdown voltage ($V_{CATHODE} < V_{BD}$) the avalanche diode is reverse biased, and the vertical NPN is off; as a result of which the TVS has no path for current conduction. When the applied voltage exceeds the avalanche diode breakdown voltage ($V_{CATHODE} > V_{BD}$) the avalanche diode conducts current to the ground through the series resistance. Lateral current flowing through the P base causes potential drop across the base. The vertical NPN turns on when this potential drop is sufficient to forward bias the base-emitter junction. This will cause carrier injection into the base and vertical current flow through the NPN transistor. The bipolar turn-on provides an alternate low resistance path for current flow. This results from minority carrier injection in the lower doped base region from the N+ emitter substrate. In this mode of operation, the impact ionization current resulting from avalanche breakdown serves as the base current of this vertical NPN, and gets amplified by the vertical NPN transistor gain, β. The phenomenon of minority carrier injection & current amplification due to the vertical NPN bipolar transistor enables this device structure to achieve much lower clamping voltage as compared to an avalanche diode.

The bipolar turn-on will also cause the clamping voltage of the device to snap from the avalanche diode breakdown voltage V_{BD} to BV_{CEO} of the vertical NPN transistor at high current densities. In order to minimize snap-back of the TVS, the breakdown voltage of the avalanche diode V_{BD} must be equal to the BV_{CEO} of the vertical NPN transistor. In order to de-couple the avalanche diode breakdown voltage and the vertical NPN BV_{CEO}, a shallow P trigger implant is used as shown in figure 1. This shallow implant gives the flexibility to tune the trigger voltage independent of the vertical NPN BV_{CEO}.

For negative bias applied to the Cathode terminal, the lateral avalanche diode turns on when the applied bias exceeds ~0.7V. As in the case of the positive bias, the lateral current flow in the P Base causes a potential drop across the base, which will turn on the base emitter junction at high currents and cause vertical current flow.

III. DEVICE MEASUREMENT RESULTS

The proposed ESD clamp based TVS was fabricated using an 8 mask bipolar process. The device was rated for an operating voltage of 5 Volts, and breakdown voltage of 7 Volts. The clamp active area was 0.025 mm^2. The doping and thickness of the N- epi region and the doping profile of the P base region were chosen such that the avalanche diode V_{BD} and the vertical NPN BV_{CEO} is equal to the target breakdown voltage of the device.

Figure 3 shows the measured static IV characteristics of the TVS. The two modes of current conduction can be clearly observed in the curve. The bipolar turn-on occurs at cathode current of 46mA, and the snap-back voltage is less than 0.5

Volts. From the above discussion on device operation, the current at which the device switches from avalanche diode mode of conduction to the vertical NPN mode of conduction can be easily adjusted by tweaking series resistance show in the equivalent circuit in figure 2. Some methods to achieve this include adjusting the sheet resistance of the P body region, the distance between the cathode N+ - P trigger junction and the contact shorting the P trigger to the epi region. Another

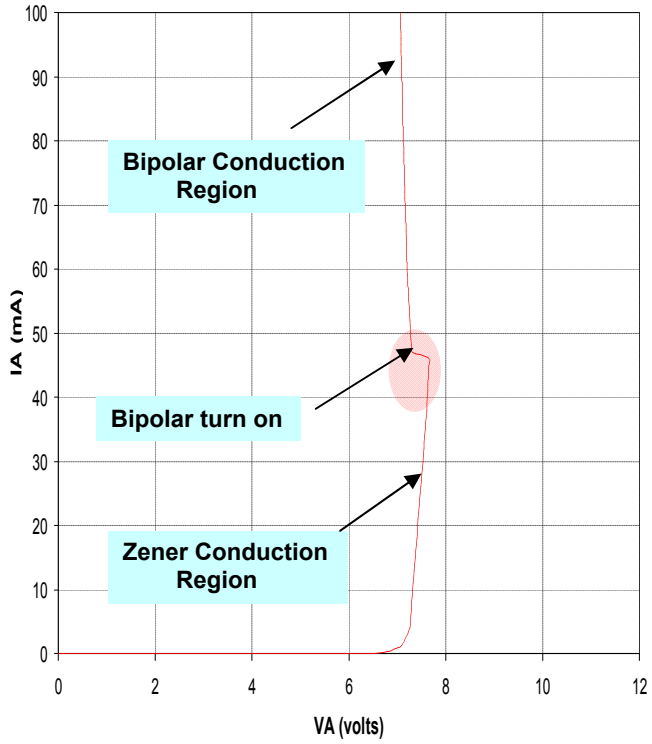

Figure 3. Measured static IV characteristics of the avalanche diode triggered bipolar transistor ESD Super-Clamp TVS

method that can be employed is to adjust the resistivity of the N- epitaxial layer in the starting wafer.

Measurements on the device leakage current and the breakdown voltages as a function of temperature are shown in figure 4. The leakage current was measured at the operating voltage of 5V. The breakdown voltage is defined as the voltage at which the device conducts 1mA of current. As shown in the figure, the device has very low leakage (< 25 n Amps) and small variation in the breakdown voltage with temperature.

Transmission line Pulse (TLP) tests were performed on the proposed clamp, and also a commercially available avalanche clamp diode based Transient Voltage Suppressor with approximately the same device area. The applied pulse was a 100ns duration square pulse with 1ns rise time. Figure 5 shows the superior clamping of the proposed clamp structure at high TLP current (13.1V vs. 25.3V @ 30Amps).

A comparison of the capacitance of the proposed ESD clamp versus an avalanche diode based structure is shown in figure 6. The device has ~35% lower capacitance as compared to the avalanche diode. This results from the presence of the lower doped P base region in this device structure, compared to the P anode in an avalanche diode. Lower doping causes a wider PN junction depletion width, thereby decreasing the junction capacitance per unit area.

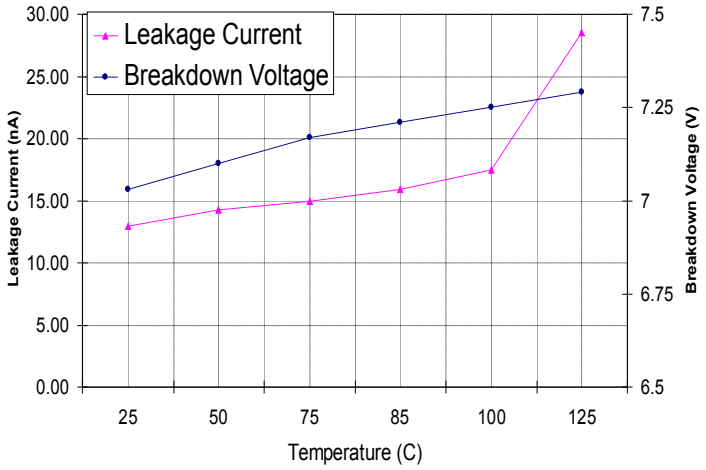

Figure 4. Measured Leakage current & Breakdown voltage as a function of temperature

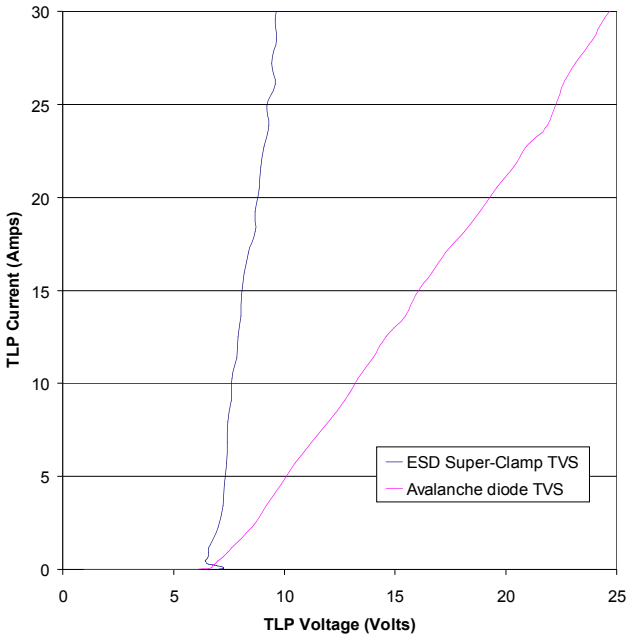

Figure 5. Comparison of measured TLP IV characteristics of the ESD Super-Clamp TVS, and a commercially available avalanche diode based clamp of approx. the same size.

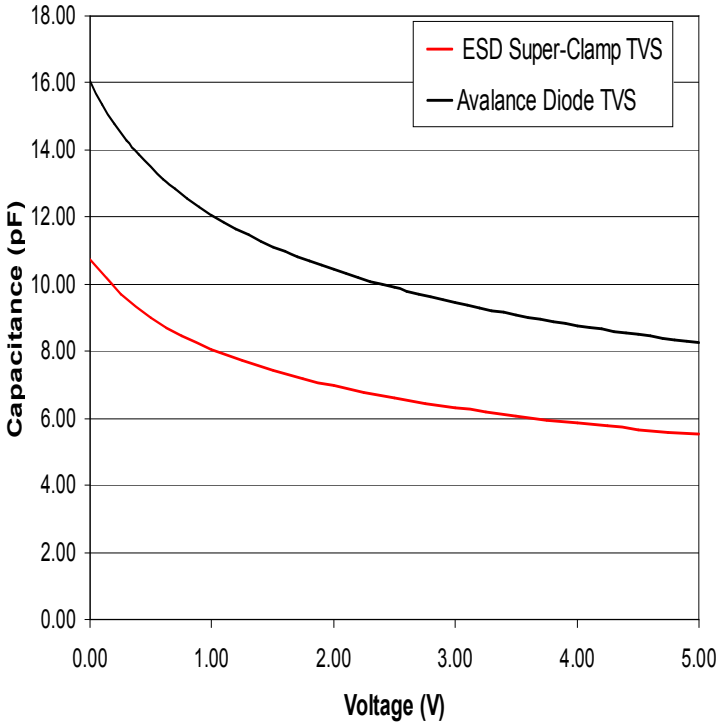

Figure 6. Comparison of measured Capacitance of the ESD Super-Clamp TVS and a commercially available avalanche diode based clamp

IV. CONCLUSIONS

A new ESD Super-Clamp structure for Transient Voltage Suppressors has been presented in this paper. The device structure consists of a vertical bipolar NPN transistor with an integrated lateral zener trigger diode. The fast response avalanche diode provides path for current conduction at low currents, and the bipolar transistor turns on and provides an alternate low resistance conduction path at high currents. Measurements on fabricated devices confirm the theory; the two modes of operation can be clearly observed in the devices IV characteristics and there is a very small snap-back (< 0.5 Volts) observed during the transition. The device also has low leakage, parasitic capacitance, and achieves excellent clamping at high currents. An improved performance in clamping voltage and lower parasitic loading makes these devices suitable for protecting portable consumer electronic devices, color LCD displays and CCD camera lines in cellular phones.

V. ACKNOWLEDGMENT

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REFERENCES

[1] J.Wu & E. Rosenbaum, "Gate Oxide Reliability Under ESD-Like Pulse Stress," *IEEE Transactions on Electron Devices*, Vol.41, Issue 9 Sept. 2004 pp 1528-1532

[2] A. Amerasekera & C. Duvvury, "The Impact of Technology Scaling on ESD Robustness and Protection Circuit Design", *IEEE Transactions on components, packaging & manufacturing*, Vol.18, No. 2 June 1995. pp 314-320

[3] S. Dabral & T. Maloney, "Basic ESD and IO Design, Chapter 2" John Wiley & Sons, Inc. 1998

[4] M.S. Shekar and M. Bobde, "Circuit Configuration and Manufacturing Processes for Vertical Transient Voltage Suppressor (TVS) and EMI Filters," US patent pending, August 2006.