Low Voltage Power MOSFET switching parameters: Testing Methods for Guaranteeing datasheet limits

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Introduction

Power MOSFET datasheets will usually show typical and min-max values for R_g, C_{iss}, C_{rss}, C_{oss}, and also show values for gate charge broken down into Q_{gs}, Q_{gd}, Q_g. It is also customary to show values for switching times during resistive switching, $t_{d(on)}$, t_{rise}, $t_{d(off)}$, t_{fall}. (For a glossary of terms, see appendix I)

It is well known that the device parameters Q_{gs}, Q_{gd}, Q_g have a one-to-one correlation with the parameters C_{iss} and C_{rss} [1]. In other words, once we measure device capacitances, we can guarantee the values of the gate charge parameters. The gate charge captures the charge needed to move the gate from 0V to the desired voltage, and integrates the non-linear capacitance over that voltage range.

The measurement of switching times are controlled by the following factors: [1,2]

- $t_{d(on)}$ – R_g, C_{iss}, V_{th}, g_m – relating to the device, and gate driver characteristics.
- t_{rise} – R_g, C_{rss}, C_{iss}, g_m, V_{th}, L_s - relating to the device, and gate driver characteristics, RL and circuit layout
- $t_{d(off)}$ - R_g, C_{iss}, V_{th}, g_m – relating to the device, and gate driver characteristics.
- t_{fall} – R_g, C_{rss}, C_{iss}, g_m, V_{th}, L_s - relating to the device, and gate driver characteristics, RL and circuit layout

Clearly, once the R_g, C_{iss}, C_{rss} for the device is measured, along with V_{th} and g_m in static testing, the switching parameters are automatically guaranteed for that device in a fixed switching circuit. The stray inductance of the packaged unit is not measured, but since it depends only on wire count and placement, the tight control of this parameter ensures very little variability in L_s.

Therefore, a measurement of R_g, C_{iss}, C_{rss} and C_{oss} is enough to guarantee the gate charge and switching time parameters for the device. Including the C_{oss}, this covers all device parameters that affect MOSFET switching losses.

Physics of dynamic parameters

A. Gate resistance

The distributed gate resistance of a power MOSFET is pictorially represented in figure 1. R_g is controlled by only a few factors for a device with a given layout

- Trench Poly sheet resistance and width and depth control
- Contact resistance between Gate metal and Poly
- Gate metal sheet resistance and width control
- Package gate wire resistance is usually a very small contributor to R_g, varies very little, and is ignored.

On each wafer, a long trench is used to monitor the resistance of a line of Poly filled trench. A four terminal Kelvin measurement is performed on the structure located in the standard process control monitor (PCM) tested on each production wafer. R_{trench} (r_t) behavior for typical AOS product is shown in figure 2.

The contact resistance between gate metal and Poly is monitored using a 4-terminal Kelvin structure. R_{gks}(R_{gk2}) is monitored in the same fashion using the PCM. R_{gks} behavior for typical AOS product is shown in figure 3.

The metal sheet resistance for a 1000um long 10um wide metal bus is monitored using a structure located in the standard process control monitor (PCM) tested on each production wafer. R_{met} behavior for typical AOS product is shown in figure 4.

It is clear that control of these parameters is excellent in AOS products.

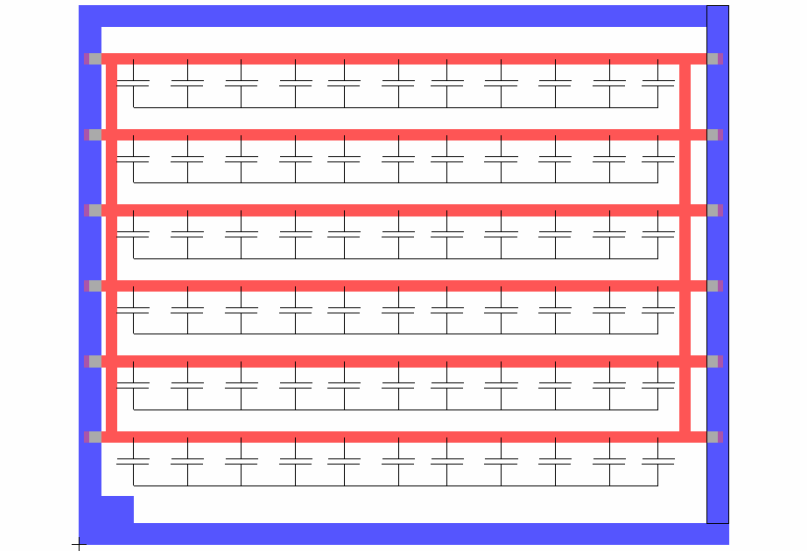


Figure 1: Model representation of the distributed gate resistance of a power MOSFET. The metal gate bus around the device is shown in blue. The gate pad is located at the corner in this case. Trenches filled with Polysilicon are shown in pink, and they contact the metal bus at the edges of the die. The distributed capacitance between the gate Polysilicon and the silicon (Source/Drain) regions is represented by the capacitors distributed along the length of the trenches.

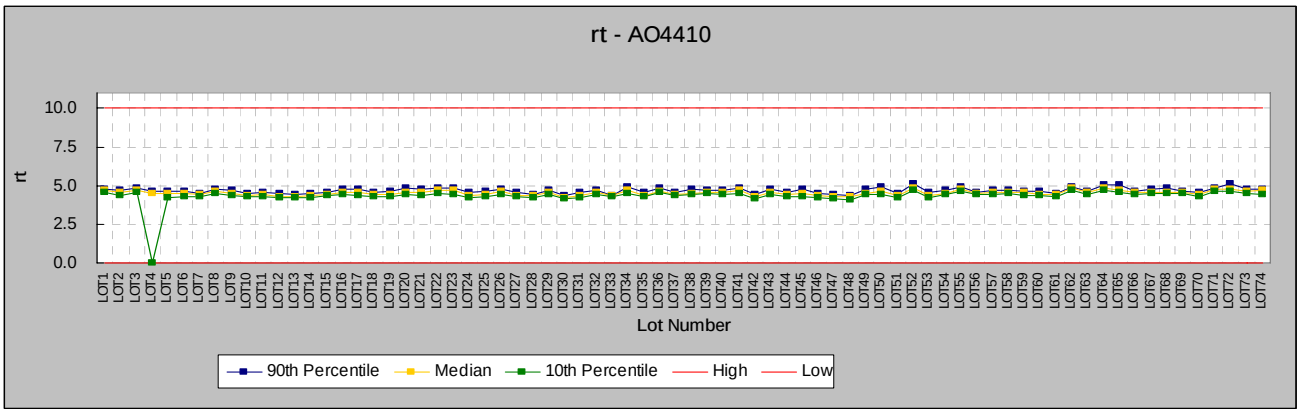


Figure 2: Trench Poly resistance monitored for AO4410, a low side optimized MOSFET. Note the median, 10th and 90th percentile lines are very close to each other, indicating tight process control. This plot covers a period from Jan-July 2006.

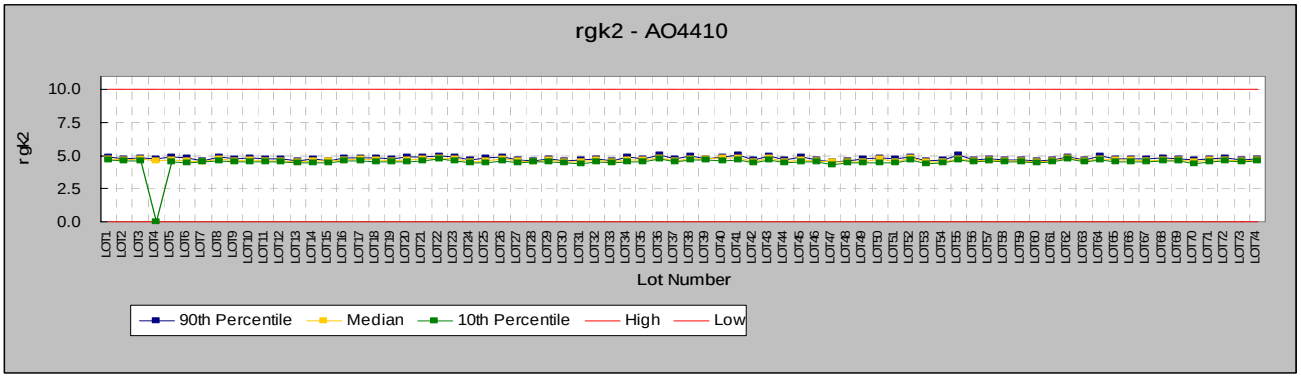


Figure 3: Gate contact resistance monitored for AO4410, a low side optimized MOSFET. Note the median, 10th and 90th percentile lines are very close to each other, indicating tight process control. This plot covers a period from Jan-July 2006.

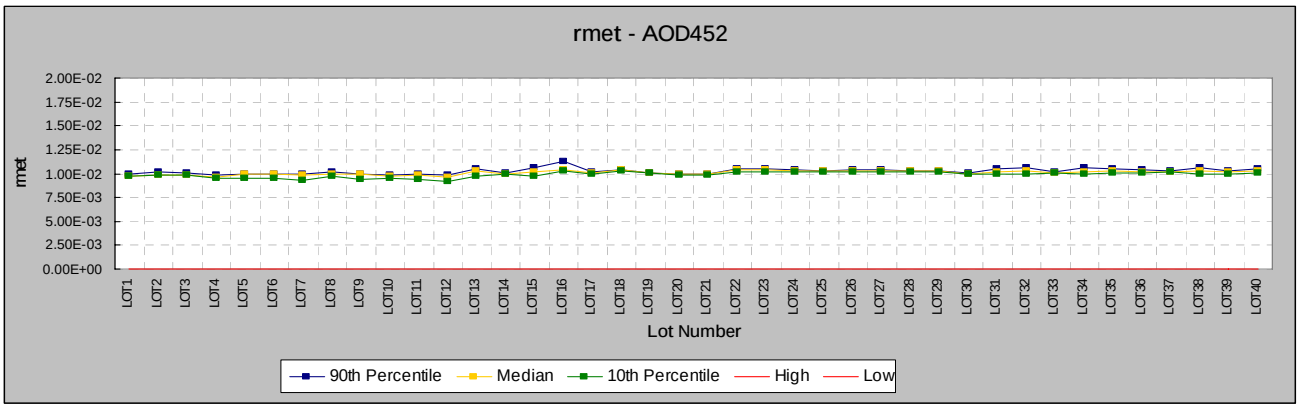


Figure 4: Resistance of a 1000um long 10um wide metal line monitored for AOD452, a high side optimized MOSFET. Note the median, 10th and 90th percentile lines are very close to each other, indicating tight process control over metal resistivity, line width and film thickness. This plot covers a period from Jan-July 2006.

Now consider the distributed nature of the MOSFET R_g as shown in figure 1. If any one contact is not completely open, or a small area has a high $R_{trench}(r_t)$, it will have little or no effect on R_g or the device, because the gate signal will re-route itself through the many parallel paths in close proximity. All AOS layouts are done with this in mind.

If the entire device has a problem with R_{trench}, R_{met} or R_{gks}, it can occur only if the wafer, or a section of the wafer has a problem with that parameter. By locating PCMs at the center and wafer edges, much of this can be monitored.

In any case, it is now clear from the nature of the device and the parameters that control R_g, that R_g for devices meeting static parameter limits doe not vary much from device to device on a wafer, and can be expected to show some wafer level patterns depending on process capability. If a device passing all DC tests fails R_g, then devices in it's vicinity on the wafer, or the entire wafer will show devices that also fail.

Another way to state this is to say that R_g cannot change abruptly on a wafer from die to die, and exhibits a distributed pattern on a wafer. *For these reasons, a wafer level sampling technique is enough to 100% guarantee the Rg on that wafer, provided the sample is large enough and encompasses the whole wafer.*

Measurement of R_g at the wafer level has traditionally been thought to be quite difficult for power MOSFETs designed for low R_g. This is true, so testing is often done 100% at the Final test station using one of the handler sites. AOS has developed proprietary techniques to accurately test R_g of our devices at the wafer level, and simultaneously test the biased Ciss, C_{rss}, C_{oss} and static parameters. This technique is applied to a 200 site sample on the wafer to guarantee 100% R_g, Ciss, C_{rss} and C_{oss} parameters o the datasheet. By extension, the gate charge and switching time parameters are 100% guaranteed.

Figure 5 shows typical distribution of R_g on a wafer. Figure 6 shows a typical wafer map. Most of the variation in R_g, though small, is actually known to come for limitations of the tester. Figure 7 compares the test results between wafer probing and packaged device testing for the same device.

Figure 8 shows the lot to lot variation over time in the form of a control chart a typical high volume AOS products. Most of the guardband in R_g specification is applied to handle test capability issues and not due to actual wafer process capability.

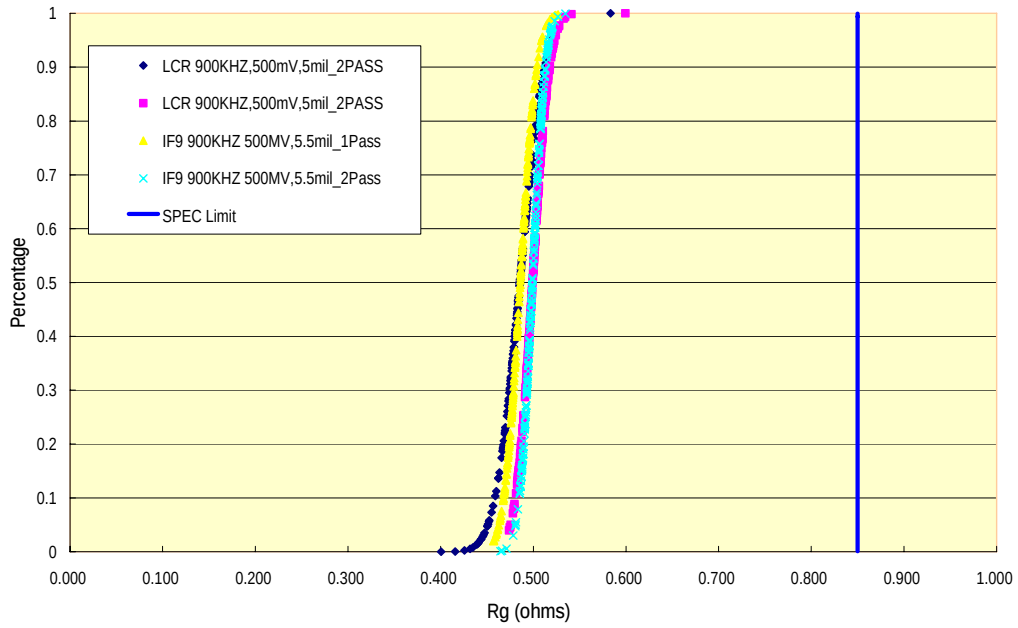


Figure 5: R_g distribution for 200 sites on a wafer taken on a Trench FET. First two passes are made with a direct connection to the LCR meter manually to obtain the most accurate readings. Next, two passes are made using the multiplexer unit in automatic probing mode. Excellent Cpk and repeatability are observed.

RG Y/X	10	17	24	31	38	45	51	58	65	72	79	86	93	100	107
16					0.47	0.47	0.46	0.46	0.46	0.47	0.47				
28				0.46	0.46	0.46	0.46	0.46	0.46	0.46	0.46	0.46			
39			0.46	0.46	0.46	0.45	0.45	0.45	0.45	0.45	0.46	0.46	0.46		
51		0.46	0.46	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.46	
62	0.46	0.46	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.46	0.46	0.47
74	0.46	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.46	0.46
85	0.46	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.46
97	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
108	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
120	0.45	0.45	0.45	0.44	0.44	0.44	0.44	0.45	0.44	0.45	0.44	0.45	0.45	0.45	0.45
131	0.46	0.45	0.45	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.45	0.45	0.45	0.45
143	0.46	0.45	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.45	0.45	0.46
154		0.45	0.44	0.45	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.45	
166			0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.45		
177				0.45	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44			
189					0.45	0.44	0.44	0.44	0.44	0.45	0.45				

Figure 6: Typical Wafer Map of Rg distribution. Probed column and row numbers shown in bold italics. Actual values shown on the wafermap. The values are very tightly distributed.

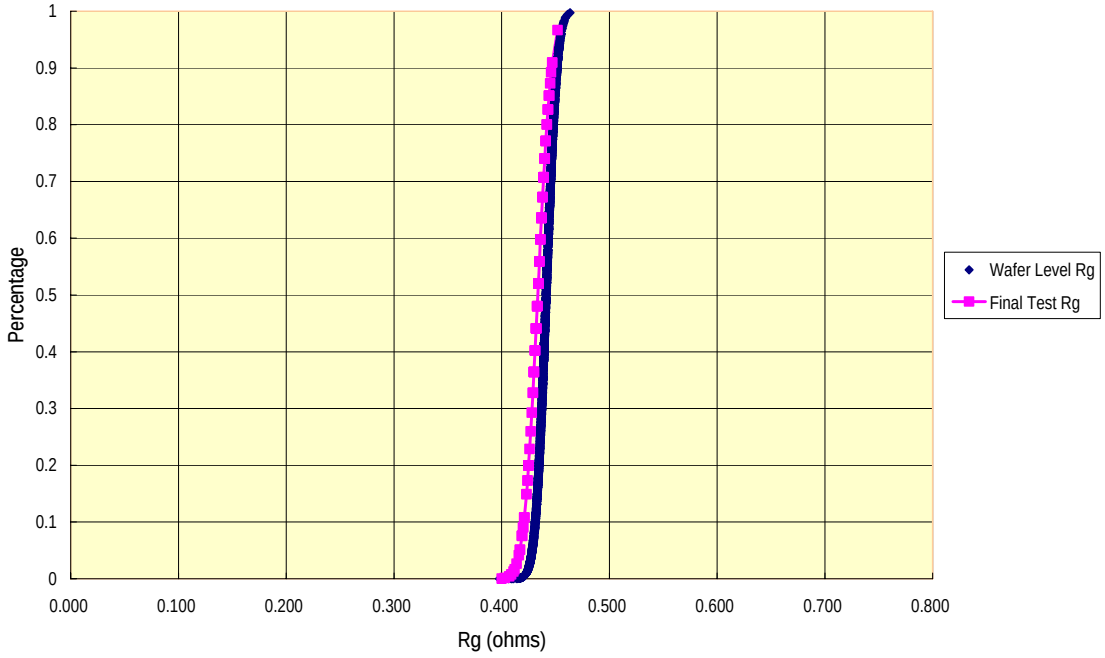


Figure 7: Comparison of wafer level and package level Rg measurements. Excellent agreement is obtained.

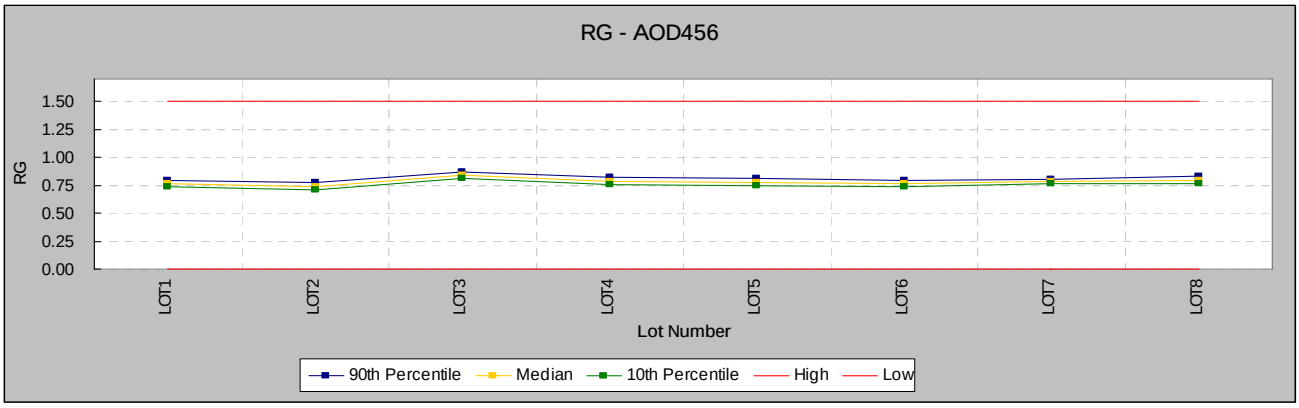


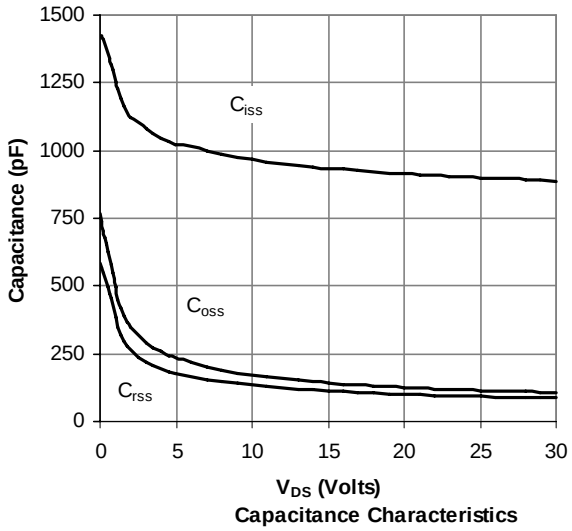
Figure 8: Lot by Lot trench chart of RG for a typical low side MOSFET AOD456. Note the tight 10th to 90th percentile lines, grouped right near the median line.

Device Capacitances

The datasheet capacitances are defined in terms of the structural capacitances as follows:
$C_{iss} = C_{gs} + C_{gd}$
$C_{rss} = C_{gd}$
$C_{oss} = C_{gd} + C_{ds}$

The C_{iss} for a trench MOSFET is determined by

- layout parameters like channel width, trench width
- gate oxide thickness and uniformity
- trench depth and shape
- Source-Body-Epi doping profiles
- Gate Poly doping is usually not a factor, since it is degenerately doped



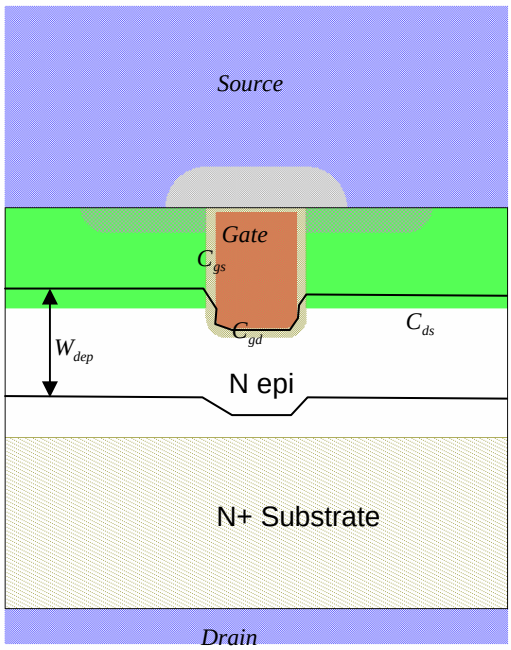


Figure 9: Device capacitances of the basic trench power MOSFET.

This parameter is dominated by the capacitance between the gate Poly and the source-channel regions, which is not bias sensitive and very repeatable.

The C_{rss} for a trench MOSFET is determined by

- layout parameters like channel width, trench width
- gate oxide thickness and uniformity
- trench depth below the body and shape, and so depends on trench depth control
- Body-Epi doping profiles
- Gate Poly doping is usually not a factor, since it is degenerately doped

This parameter is dominated by the sensitive to the depth of the trench below the body junction, and the epi (Drain) layer doping profile.

The C_{oss} for a trench MOSFET is determined by

- All parameters that affect C_{rss}, since it is part of C_{oss} and
- gate oxide thickness and uniformity
- Body diode p-n junction area and doping profile

Figure 10 shows the typical distribution for these parameters on a wafer. Figure 11 shows the wafer map for the same distribution. A trend can be seen with high C_{iss} at the wafer edge, which can be correlated to factors like trench depth and Poly etch depth.

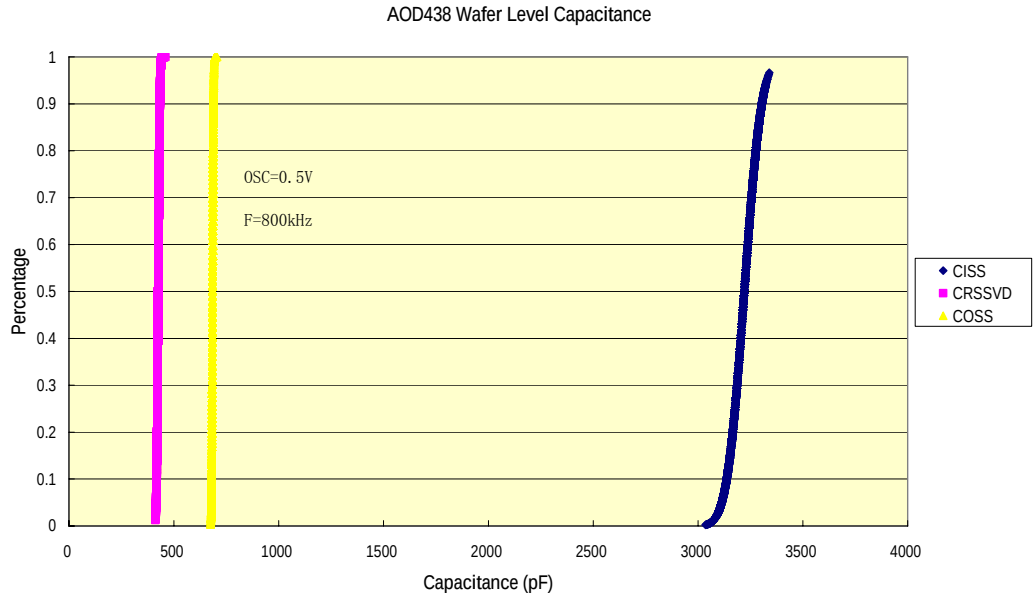


Figure 10: Distribution of Ciss, Crss, Coss for the 200 sites tested on a wafer (AOD438). Excellent process control leads to the a very tight parameter distribution.

Y/X	10	17	24	31	38	45	51	58	65	72	79	86	93	100	107
16					8.9E-10	8.9E-10	8.9E-10	8.9E-10	9.0E-10	8.9E-10	8.9E-10				
28				8.9E-10	9.0E-10	9.0E-10	9.1E-10	9.1E-10	9.1E-10	9.1E-10	9.0E-10	9.0E-10			
39			9.0E-10	9.0E-10	9.1E-10	9.2E-10	9.2E-10	9.2E-10	9.2E-10	9.2E-10	9.1E-10	9.1E-10	9.0E-10		
51		9.0E-10	9.1E-10	9.1E-10	9.2E-10	9.2E-10	9.2E-10	9.2E-10	9.2E-10	9.2E-10	9.2E-10	9.2E-10	9.1E-10	9.0E-10	
62	8.9E-10	9.1E-10	9.1E-10	9.2E-10	9.2E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.2E-10	9.2E-10	9.1E-10	9.0E-10
74	9.0E-10	9.1E-10	9.2E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.2E-10	9.2E-10	9.2E-10	9.0E-10
85	9.1E-10	9.2E-10	9.2E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.2E-10	9.1E-10
97	9.1E-10	9.2E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.3E-10	9.2E-10	9.1E-10
108	9.1E-10	9.2E-10	9.3E-10	9.3E-10	9.4E-10	9.4E-10	9.3E-10	9.3E-10	9.4E-10	9.4E-10	9.4E-10	9.3E-10	9.3E-10	9.2E-10	9.2E-10
120	9.1E-10	9.2E-10	9.3E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.3E-10	9.3E-10	9.2E-10
131	9.1E-10	9.2E-10	9.3E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.3E-10	9.3E-10	9.2E-10
143	9.1E-10	9.2E-10	9.3E-10	9.4E-10	9.5E-10	9.5E-10	9.5E-10	9.4E-10	9.5E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.3E-10	9.1E-10
154		9.2E-10			9.5E-10	9.5E-10	9.5E-10	9.5E-10	9.5E-10	9.4E-10	9.4E-10	9.4E-10	9.3E-10	9.2E-10	
166			9.3E-10	9.4E-10	9.4E-10	9.5E-10	9.5E-10	9.5E-10	9.5E-10	9.4E-10	9.4E-10	9.3E-10			
177				9.3E-10	9.4E-10	9.4E-10	9.5E-10	9.5E-10	9.5E-10	9.5E-10	9.4E-10				
189					9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.4E-10	9.3E-10				

Figure 11: Wafermap of C_{iss} data showing the tight distribution of C_{iss} across the wafer. C_{iss} is seen to be somewhat lower across the top, left and right edges of the wafer.

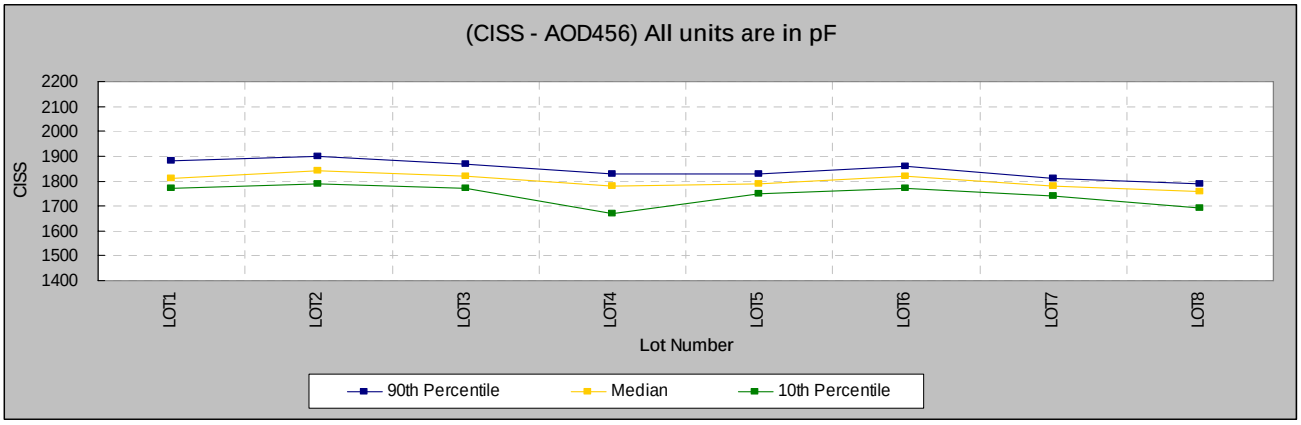


Figure 12: Lot to Lot variation in C_{iss} for AOD456. Note the tight 10^{th} to 90^{th} percentile lines, grouped right near the median line.

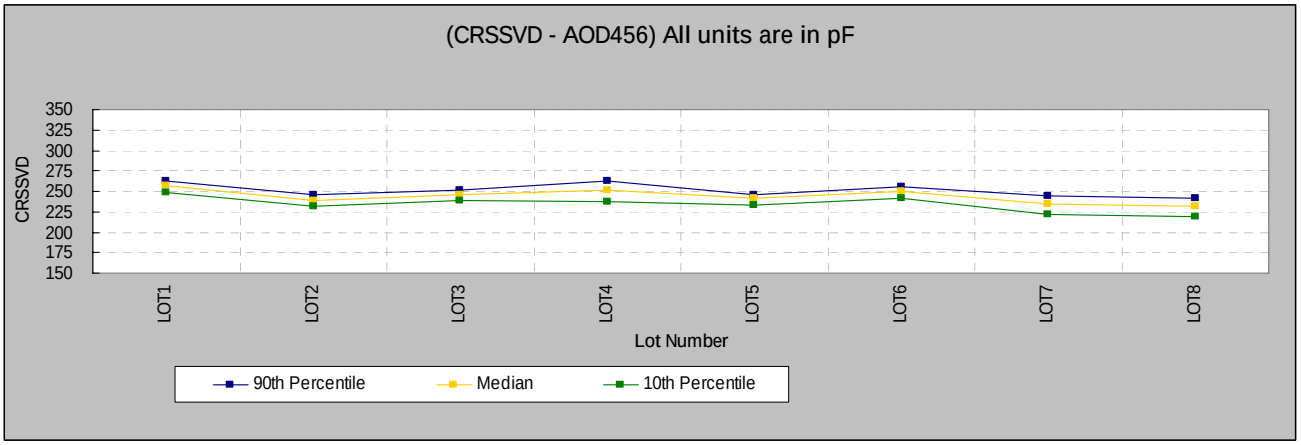


Figure 13: Lot to Lot variation in C_{rss} for AOD456. Note the tight 10^{th} to 90^{th} percentile lines, grouped right near the median line.

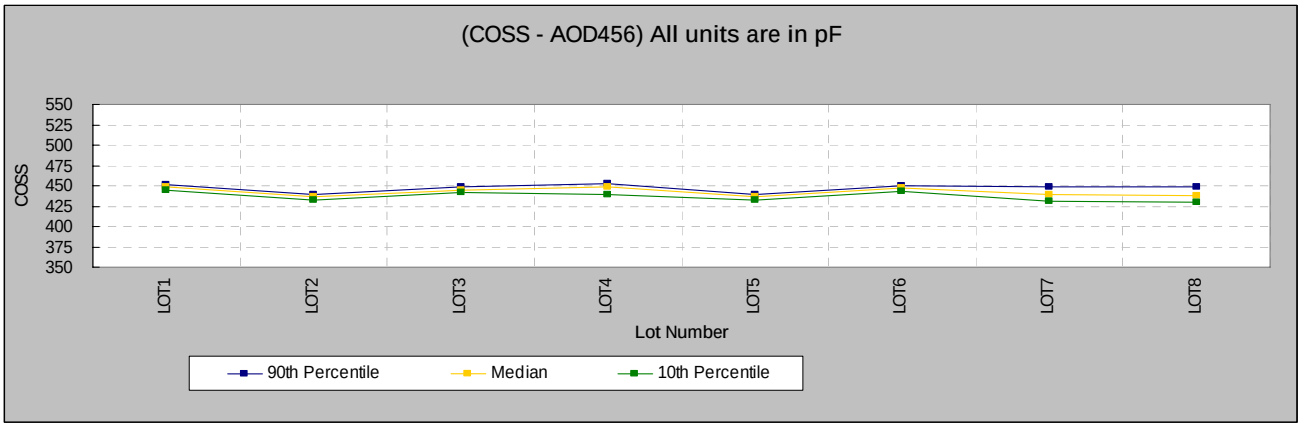


Figure 14: Lot to Lot variation in C_{oss} for AOD456. Note the tight 10th to 90th percentile lines, grouped right near the median line.

Figures 12, 13 and 14 shows the lot to lot variation over time in the form of a control chart for two high volume AOS products. Note the tight control over the process this demonstrates.

The subtle changes in these capacitances together with the static parameter data for BV_{DSS}, R_{ds} and wafer map patterns help to determine whether incoming material, trench depth control or some other factor is at work influencing the AC parameters, and provides a powerful tool for continuous improvement.

Conclusion

We have shown how a wafer level sample measurement of the MOSFET parameters R_g, C_{rss}, C_{iss} and C_{oss} is sufficient to 100% guarantee all the switching parameters of the device. (Q_{gs}, Q_{gd}, Q_g, $t_{d(on)}$, t_{rise}, $t_{d(off)}$, t_{fall}). Extensive measurements are used to show the accuracy and effectiveness of this wafer level testing schemeTrend charts of both process level structural parameters and actual measurements of R_g and capacitances are both shown. Excellent process control is shown to lead to excellent control over R_g and device capacitances for AOS MOSFETs. . Even though wafer level measurement of Rg is accurate enough, AOS also implement 100% Rg testing at part level before shipping to customer.

Appendix I: Glossary of Terms

Q_g: Total gate charge to bring the MOSFET from V_{gs}=0V to a specified final value, e.g. 10V.
Q_{gs}: Gate-source charge. Portion of Q_g needed to charge the gate to its plateau voltage.
Q_{gd}: Portion of Q_g during which the Miller capacitance is charged.
R_g: Equivalent Series Resistance or Gate resistance of the MOSFET, measured between gate and source.
C_{iss}: Input capacitance at the gate.
C_{rss}: Reverse transfer capacitance.
C_{oss}: Output capacitance at the Drain.
V_{th}: MOSFET threshold voltage
g_m: transconductance
$t_{d(on)}$: turn on delay time
t_{rise}: Turn on current rise time
$t_{d(off)}$: turn off delay time
t_{fall}: turn of current fall time
L_s: Source Inductance

REFERENCES

[1] Modern Power Devices, B.J. Baliga, John Wiley and Sons, 1987.
[2] Power MOSFETs: Theory and Applications, D.A. Grant and J. Gowar, John Wiley and Sons, 1989.

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