

General Description

- Trench Power MOSFET technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- Excellent Thermal Performance
- RoHS and Halogen-Free Compliant

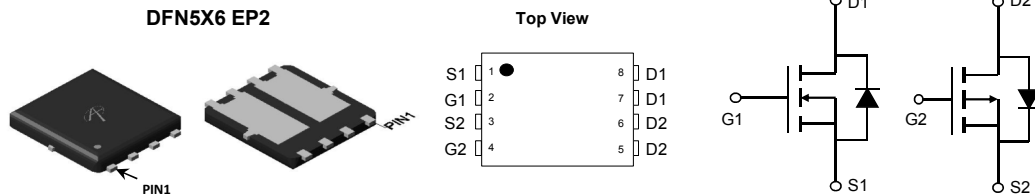
Applications

- Pch+Nch Complementary MOSFET for DC-FAN

Product Summary

	Q1	Q2
V_{DS}	30V	-30V
I_D (at $V_{GS}=10V$)	16A	-16A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 25m Ω	< 22m Ω
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 35m Ω	< 35m Ω

100% UIS Tested
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AON6667	DFN 5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^G	I_D	16	-16	A
$T_C=100^\circ\text{C}$		10.5	-12.5	
Pulsed Drain Current ^C	I_{DM}	35	-65	
Continuous Drain Current	I_{DSM}	9.5	11	A
$T_A=70^\circ\text{C}$		7.5	-8.5	
Avalanche Current ^C	I_{AS}	12	-27	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}	7	36	mJ
V_{DS} Spike	V_{SPIKE}	36	-36	V
Power Dissipation ^B	P_D	10	20	W
		4	8	
Power Dissipation ^A	P_{DSM}	3.1	4.1	W
		2	2.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	30	20	40	30	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D}		Steady-State	55	48	70	65
Maximum Junction-to-Case	$R_{\theta JC}$	9	5	12	6	$^\circ\text{C/W}$

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.5	2.1	2.6	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =10A T _J =125°C		18.5	25	mΩ
		V _{GS} =4.5V, I _D =5A		27	35	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =10A		17		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				10	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		373		pF
C _{oss}	Output Capacitance			67		pF
C _{rss}	Reverse Transfer Capacitance			41		pF
R _g	Gate resistance	f=1MHz	0.6	1.8	2.8	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =10A		7.1	15	nC
Q _g (4.5V)	Total Gate Charge			3.5	7	nC
Q _{gs}	Gate Source Charge			1.2		nC
Q _{gd}	Gate Drain Charge			1.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =1.5Ω, R _{GEN} =3Ω		4.3		ns
t _r	Turn-On Rise Time			2.8		ns
t _{D(off)}	Turn-Off DelayTime			15.8		ns
t _f	Turn-Off Fall Time			3.0		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =10A, di/dt=500A/μs		6.0		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =10A, di/dt=500A/μs		6.6		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

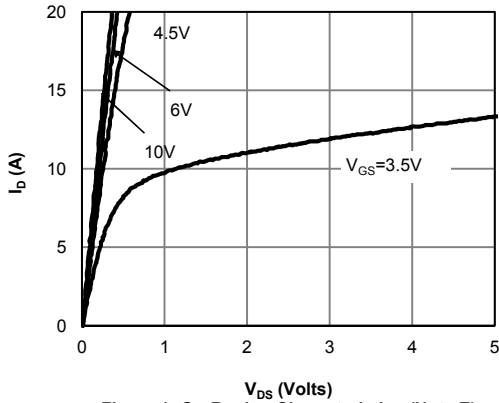


Figure 1: On-Region Characteristics (Note E)

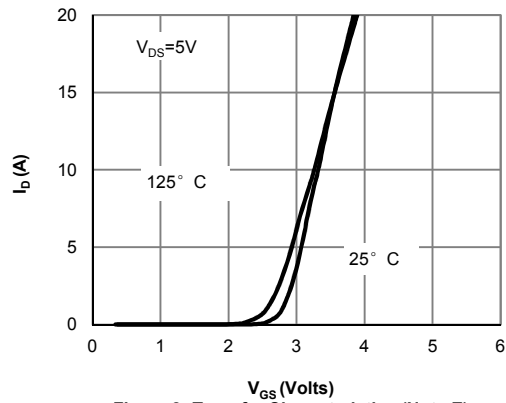


Figure 2: Transfer Characteristics (Note E)

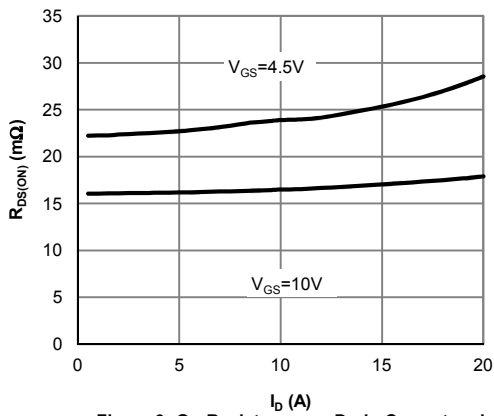


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

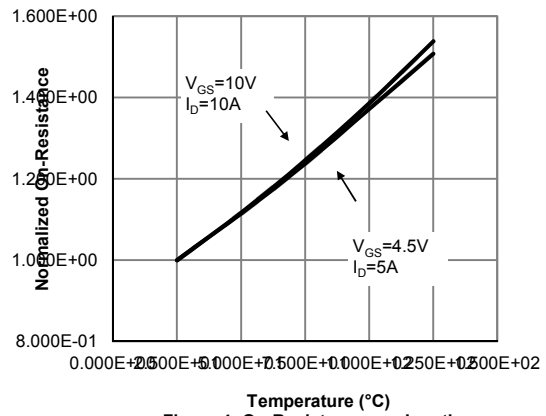


Figure 4: On-Resistance vs. Junction Temperature (Note E)

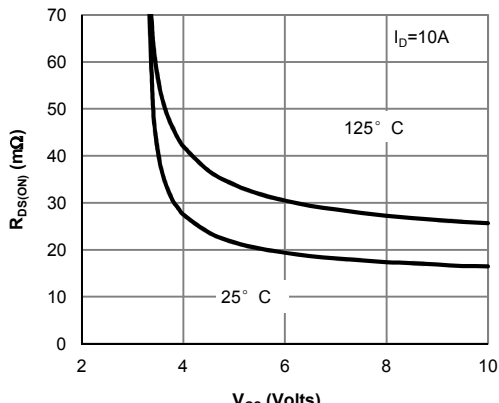


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

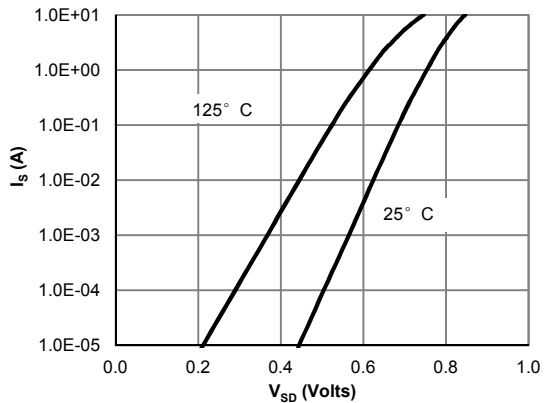


Figure 6: Body-Diode Characteristics (Note E)

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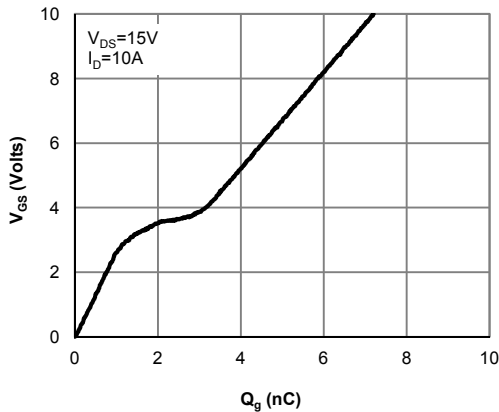


Figure 7: Gate-Charge Characteristics

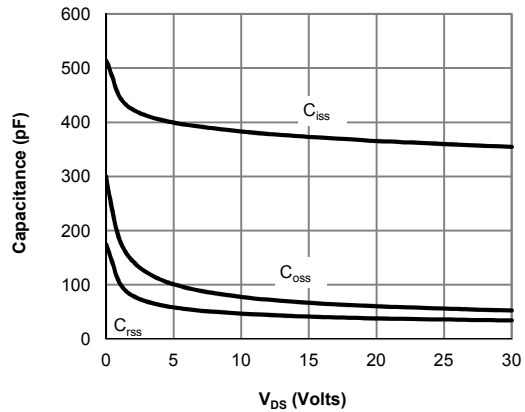


Figure 8: Capacitance Characteristics

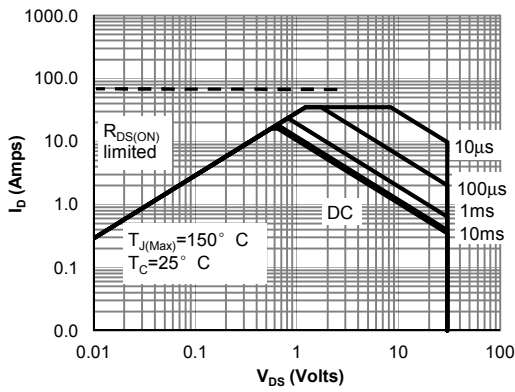


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

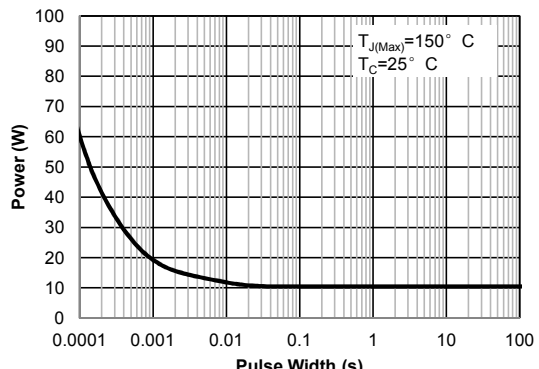


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

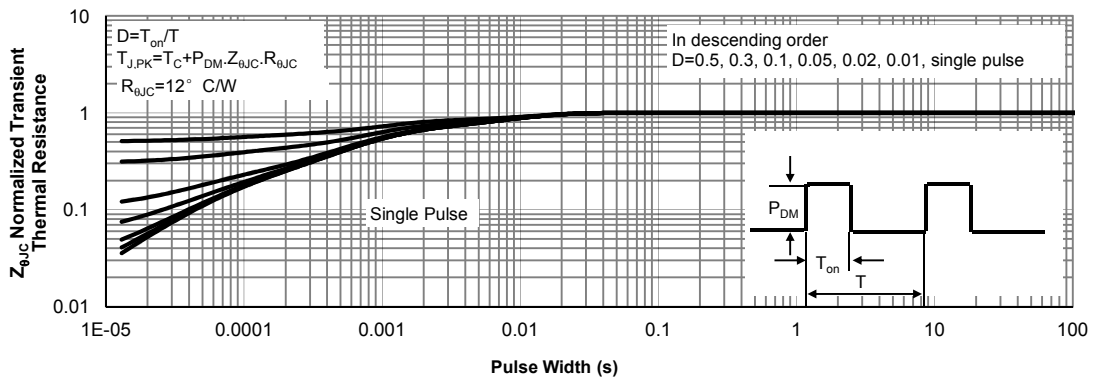


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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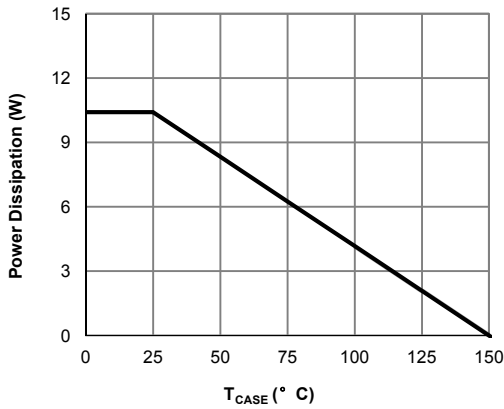


Figure 12: Power De-rating (Note F)

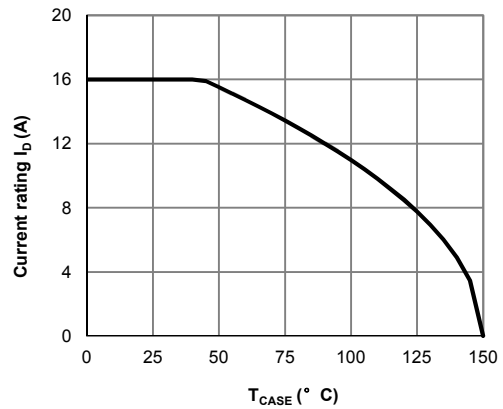


Figure 13: Current De-rating (Note F)

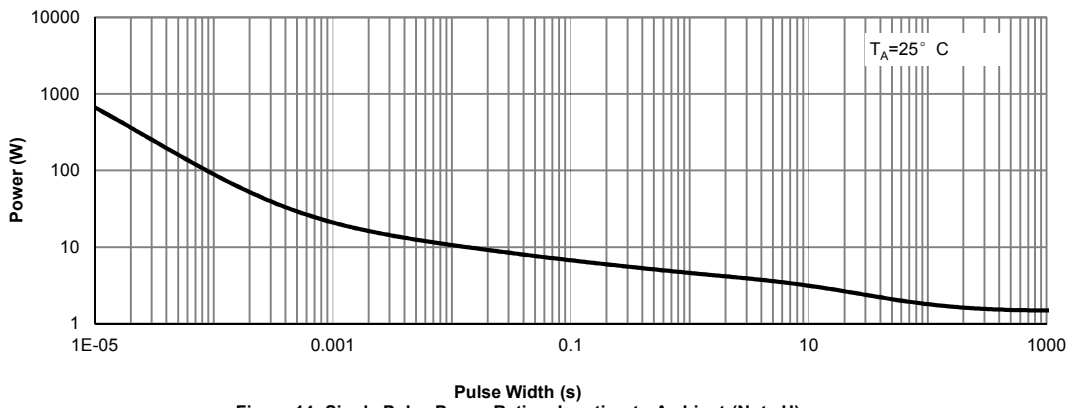


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

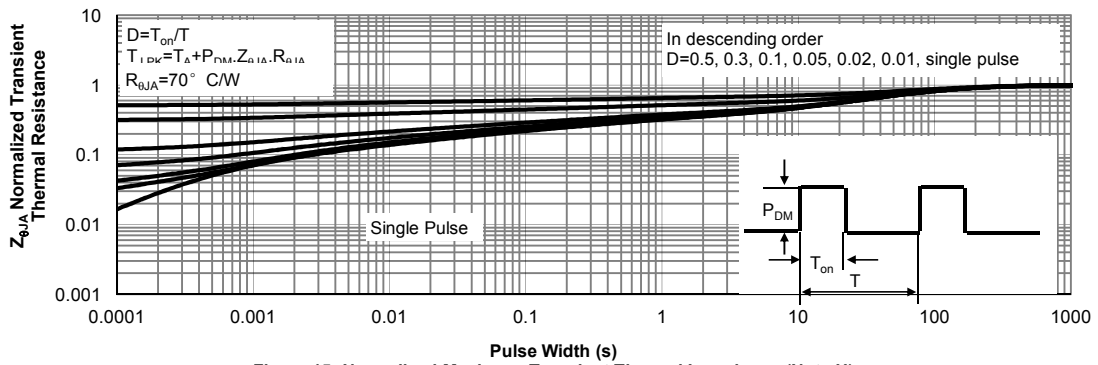


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.5	-2.0	-2.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-9.7A T _J =125°C		16.5	22	mΩ
		V _{GS} =-4.5V, I _D =-7A		24	32	
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-9.7A		27		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.75	-1	V
I _S	Maximum Body-Diode Continuous Current ^G				-16	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		1040		pF
C _{oss}	Output Capacitance			180		pF
C _{riss}	Reverse Transfer Capacitance			125		pF
R _g	Gate resistance	f=1MHz	2	4	6	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-9.7A		19	30	nC
Q _g (4.5V)	Total Gate Charge			9.6	15	nC
Q _{gs}	Gate Source Charge			3.6		nC
Q _{gd}	Gate Drain Charge			4.6		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =1.5Ω, R _{GEN} =3Ω		10		ns
t _r	Turn-On Rise Time			5.5		ns
t _{D(off)}	Turn-Off DelayTime			26.0		ns
t _f	Turn-Off Fall Time			9		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-9.7A, dI/dt=500A/μs		11.5		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-9.7A, dI/dt=500A/μs		25		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

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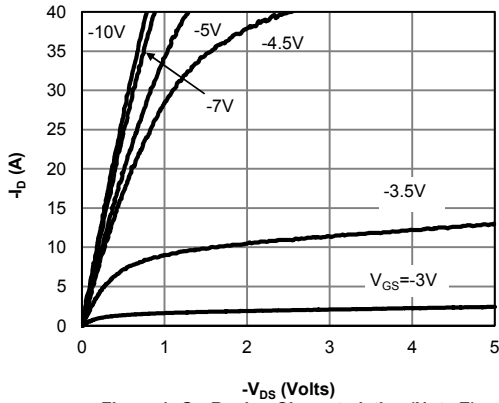


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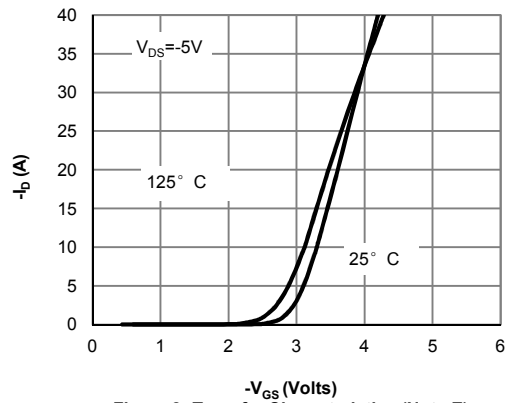


Figure 2: Transfer Characteristics (Note E)

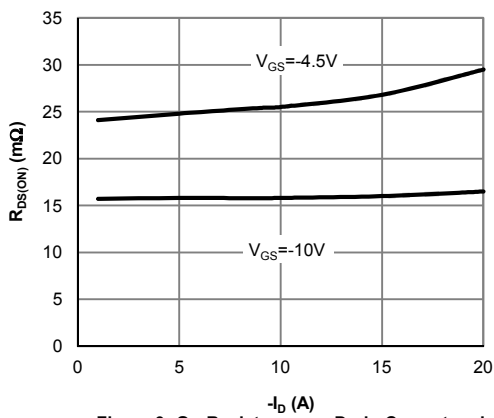


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

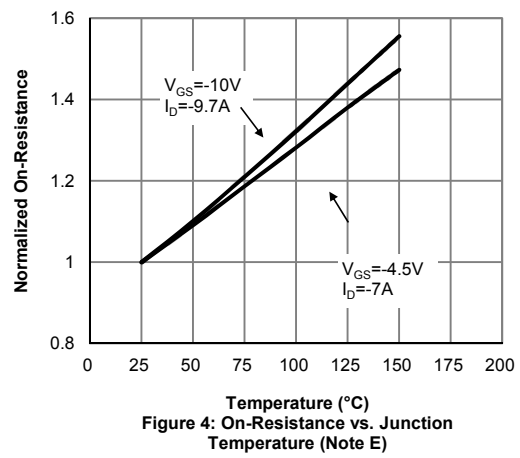


Figure 4: On-Resistance vs. Junction Temperature (Note E)

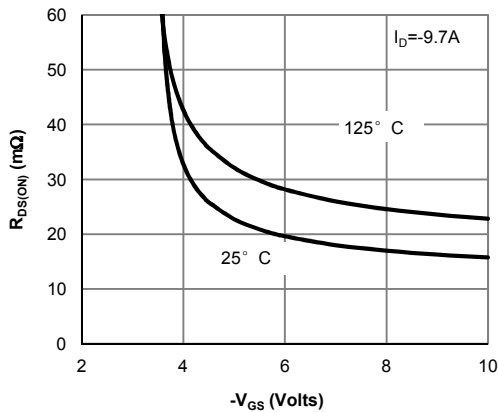


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

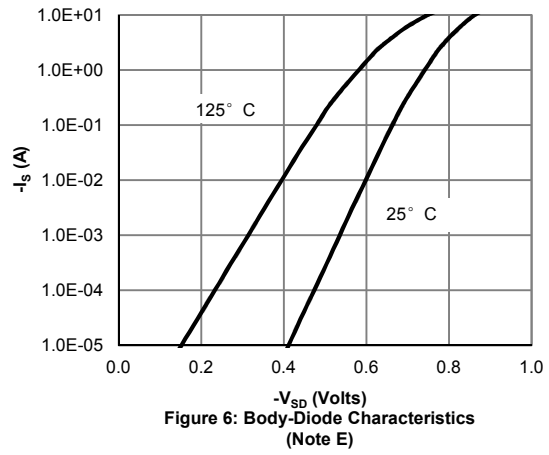


Figure 6: Body-Diode Characteristics (Note E)

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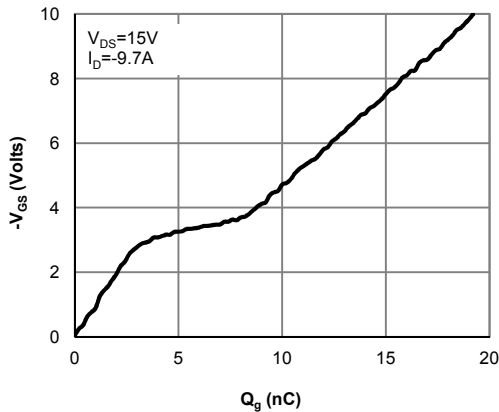


Figure 7: Gate-Charge Characteristics

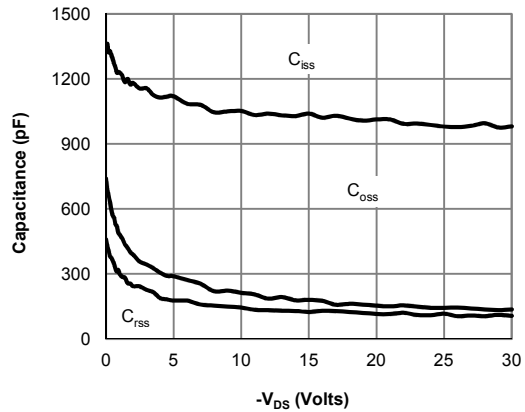


Figure 8: Capacitance Characteristics

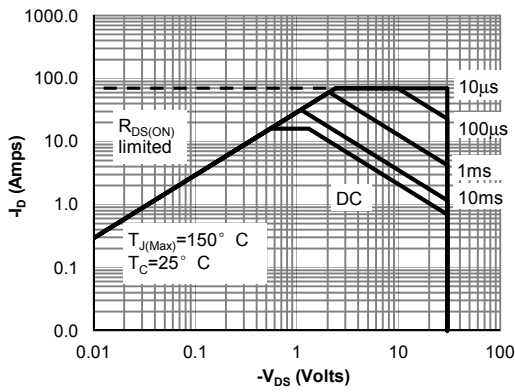


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

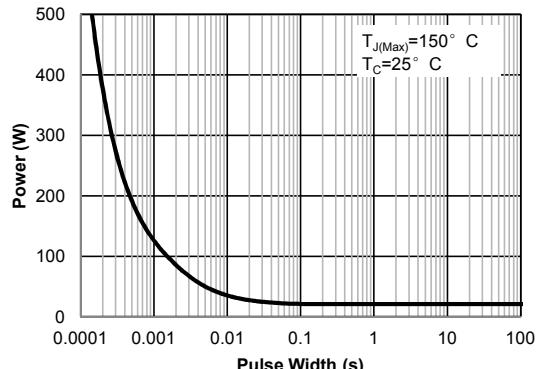


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

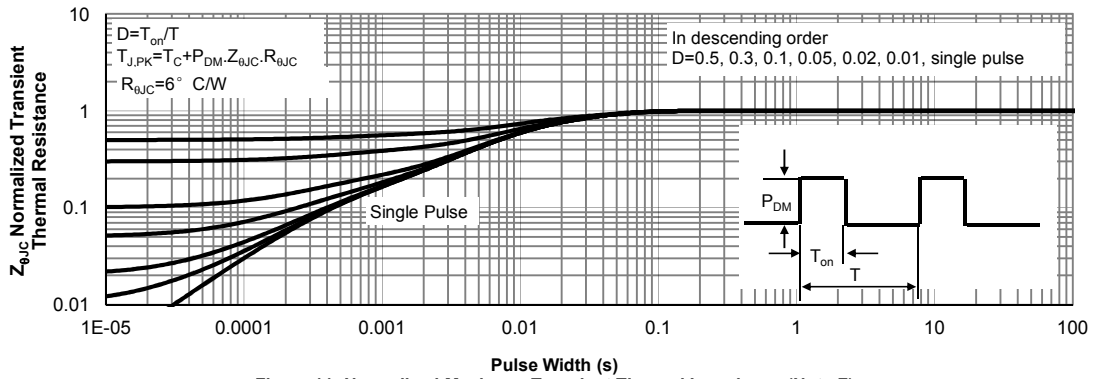


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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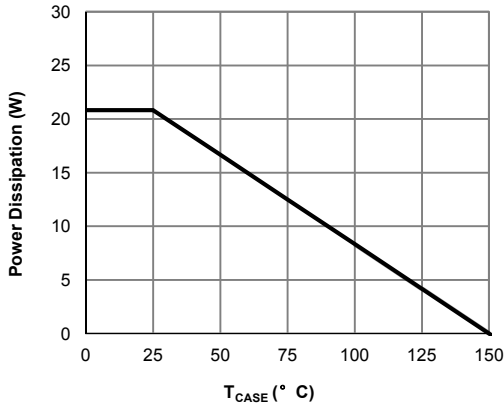


Figure 12: Power De-rating (Note F)

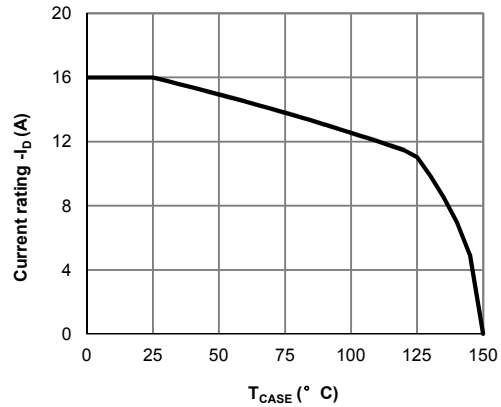


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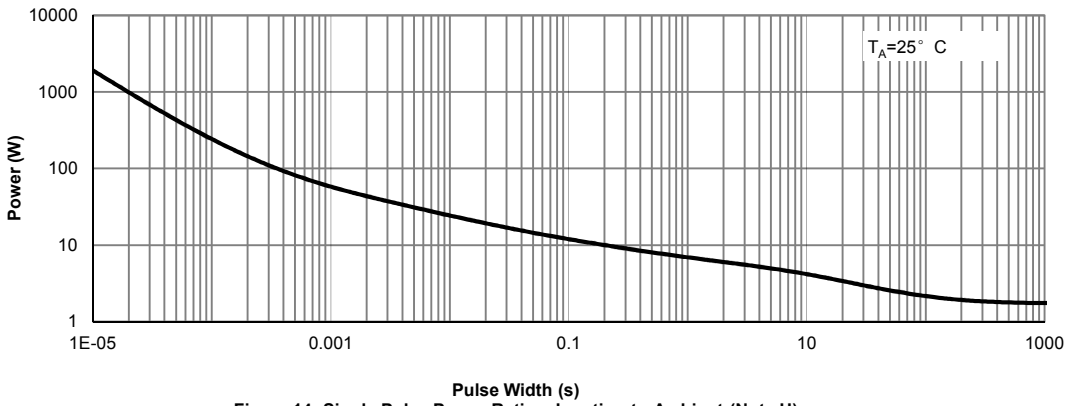


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

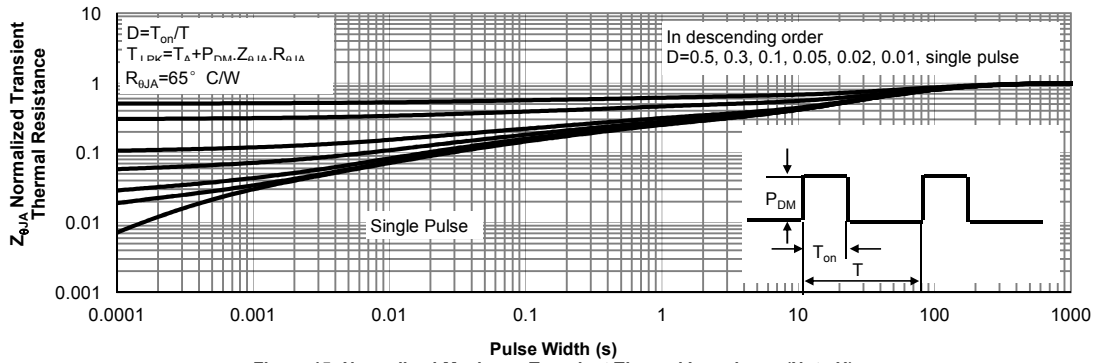


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

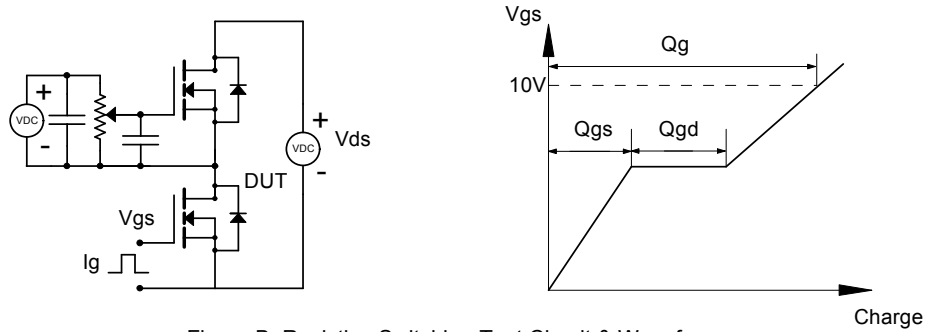


Figure B: Resistive Switching Test Circuit & Waveforms

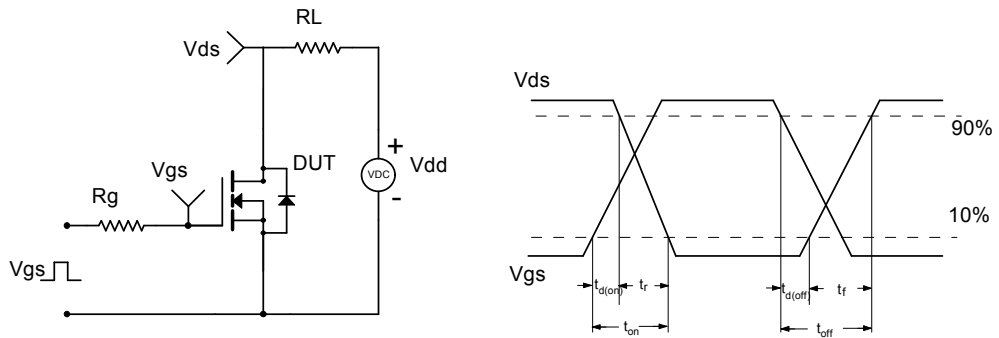


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

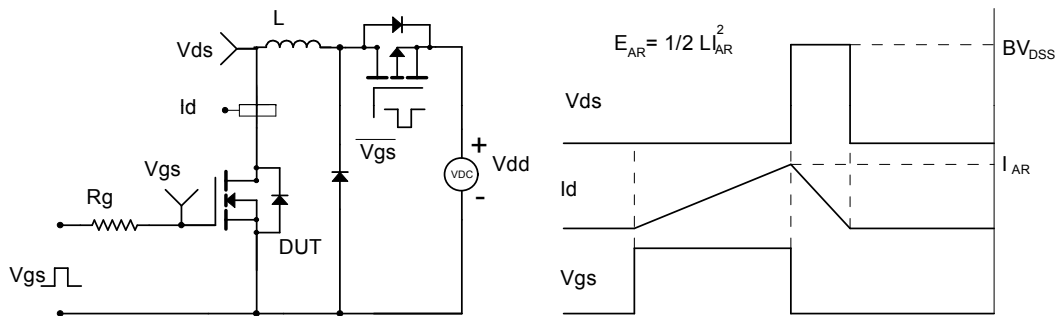
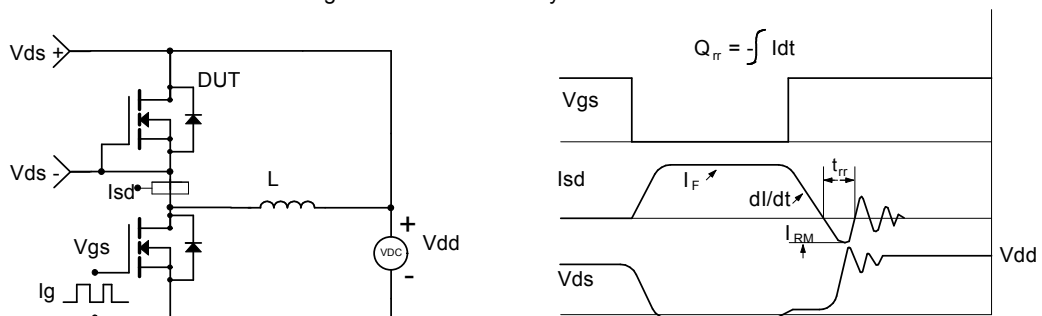
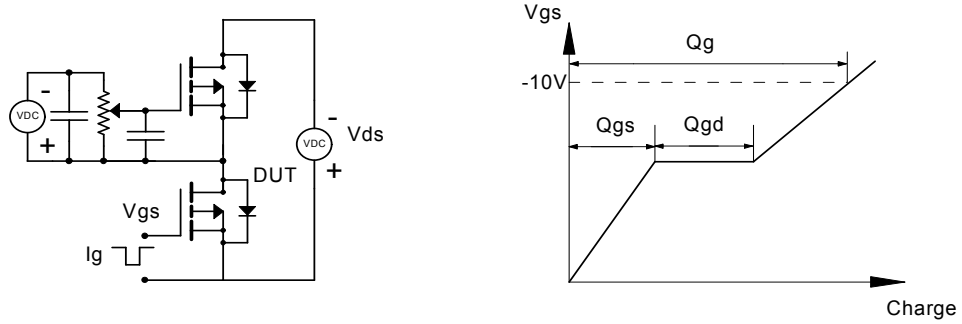


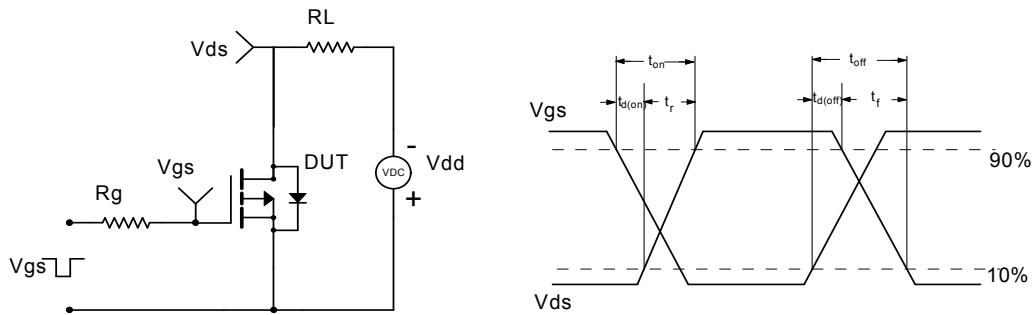
Figure D: Diode Recovery Test Circuit & Waveforms



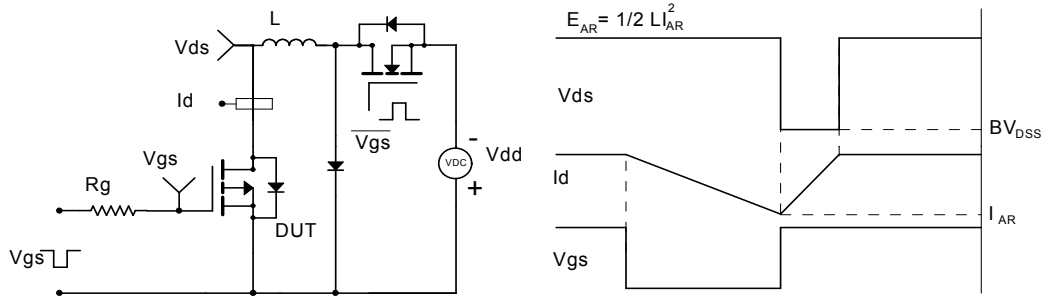
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

