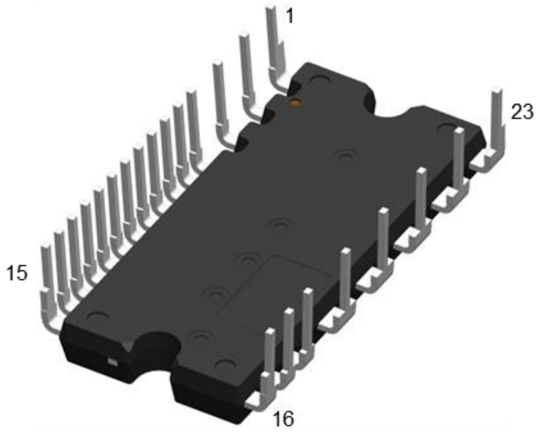
ALPHA & OMEGA
SEMICONDUCTOR

AIM5D05K060Q8S

Dual-In-Line Package Intelligent Power Module

External View



Size: 33.4 x 15 x 3.6 mm

GREEN
Product

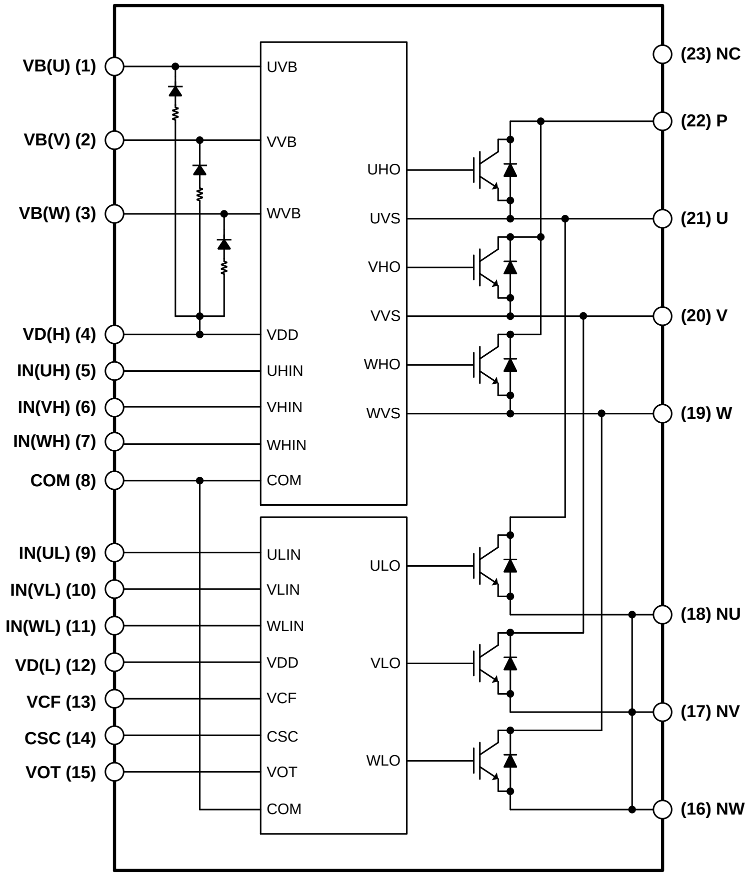
Features

- 600V-5A (Trench Shielded Planar Gate IGBT)
- 3 phase inverter module including HVIC drivers
- Built-in bootstrap diodes with integrated current-limiting resistor
- Control supply under-voltage lockout protection (UVLO)
- Over-temperature (OT) protection
- Temperature monitoring (VOT) – 10kΩ resistor connection
- Short-circuit current protection (CSC)
- Controllable fault out signal (VCF) corresponding to SC, UV and OT fault
- Wide input interface (3-18V), Schmitt trigger receiver circuit (Active High)
- Isolation ratings of 2000Vrms/min

Applications

- AC 100-240Vrms class low power motor drives
- Refrigerators, Dishwashers, Fan motors and Washing machines

Internal Equivalent Circuit / Pin Configuration



Ordering Information

Part Number	Package	Pin Length Description
AIM5D05K060Q8S	IPM-5A	Short

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Description

Pin Number	Pin Name	Pin Function
1	VB(U)	High-Side Bias Voltage for U-Phase IGBT Driving
2	VB(V)	High-Side Bias Voltage for V-Phase IGBT Driving
3	VB(W)	High-Side Bias Voltage for W-Phase IGBT Driving
4	VD(H)	High-Side Common Bias Voltage for IC and IGBTs Driving
5	IN(UH)	Signal Input for High-Side U-Phase
6	IN(VH)	Signal Input for High-Side V-Phase
7	IN(WH)	Signal Input for High-Side W-Phase
8	COM	Common Supply Ground
9	IN(UL)	Signal Input for Low-Side U-Phase
10	IN(VL)	Signal Input for Low-Side V-Phase
11	IN(WL)	Signal Input for Low-Side W-Phase
12	VD(L)	Low-Side Common Bias Voltage for IC and IGBTs Driving
13	VCF	Fault Output
14	CSC	Capacitor (Low-Pass Filter) for Short-circuit Current Detection Input
15	VOT	Voltage Output of LVIC Temperature
16	NW	Negative DC-Link Input for W-Phase
17	NV	Negative DC-Link Input for V-Phase
18	NU	Negative DC-Link Input for U-Phase
19	W	Output for W-Phase
20	V	Output for V-Phase
21	U	Output for U-Phase
22	P	Positive DC-Link Input (Built-in wire fuse)
23	NC	No Connection

Absolute Maximum Ratings

T_J = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Ratings	Units
Inverter				
V_{PN}	Supply Voltage	Between P - NU,NV,NW	450	V
$V_{PN(surge)}$	Supply Voltage (surge)	Between P - NU,NV,NW	500	V
V_{CES}	Collector-emitter Voltage		600	V
I_C	Output Phase Current	T_C=25°C, T_J<150°C	5	A
		T_C=100°C, T_J<150°C	3	A
$\pm I_{PK}$	Output Peak Phase Current	T_C=25°C, less than 1ms pulse width	10	A
P_C	Collector Dissipation	T_C=25°C, per chip	18.9	W
T_J	Operating Junction Temperature		-40 to 150	°C
Control (Protection)				
V_{DD}	Control Supply Voltage	Between VD(H)-COM, VD(L)-COM	25	V
V_{BS}	High-Side Control Bias Voltage	Between VB(U)-U, VB(V)-V, VB(W)-W	25	V
V_{IN}	Input Voltage	Between IN(UH), IN(VH), IN(WH), IN(UL), IN(VL), IN(WL)-COM	-0.3 ~ V_{DD}+0.5	V
V_{CF}	Fault Output Supply Voltage	Between VCF-COM	-0.3 ~ 5.5	V
I_{FO}	Fault Output Current	Sink current at VCF terminal	1	mA
V_{SC}	Current Sensing Input Voltage	Between CSC-COM	-0.3 ~ 5.5	V
V_{OT}	Temperature Output	Between VOT-COM	-0.3 ~ 5.5	V
Total System				
$V_{PN(PROT)}$	Self-protection Supply Voltage Limit (Short-circuit protection capability)	V_{DD}=13.5-16.5V, Inverter part Non-repetitive, less than 2µs	400	V
T_C	Module Case Operation Temperature	Measurement point of T_C is provided in Figure 1	-30 to 125	°C
T_{STG}	Storage Temperature		-40 to 125	°C
V_{ISO}	Isolation Voltage	60Hz, sinusoidal, AC 1min, between connected all pins and heat sink plate	2000	V_{rms}

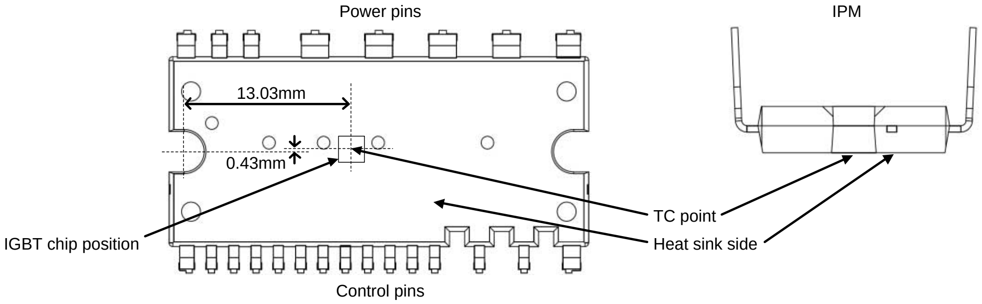


Figure 1. T_C Measurement Point

Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 1)	Inverter IGBT (per 1/6 module)	-	-	6.6	K/W
$R_{th(j-c)F}$		Inverter FWD (per 1/6 module)	-	-	8.5	K/W

Note:

1. For the measurement point of case temperature (T_C), please refer to Figure 1.

Electrical Characteristics

T_J = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Inverter							
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	V_{DD}=V_{BS}=15V, V_{IN}=5V	I_C=2.5A, T_J=25°C	-	1.48	1.85	V
			I_C=2.5A, T_J=125°C	-	1.69	-	V
V_F	FWD Forward Voltage	V_{IN}=0	I_F=2.5A, T_J=25°C	-	1.40	1.75	V
t_{ON}	Switching Times	V_{PN}=300V, V_{DD}=V_{BS}=15V I_C=2.5A, T_J=25°C, V_{IN}=0V ↔ 5V Inductive load (high-side)		-	0.80	-	µs
$t_{C(ON)}$				-	0.10	-	µs
t_{OFF}				-	0.85	-	µs
$t_{C(OFF)}$				-	0.12	-	µs
t_{rr}				-	0.13	-	µs
I_{CES}	Collector-Emitter Leakage Current	V_{CE}=V_{CES}	T_J=25°C	-	-	1	mA
			T_J=125°C	-	-	10	mA
Control (Protection)							
I_{QDH}	Quiescent V_{DD} Supply Current	$V_{D(H)}$=15V, $V_{IN(xH)}$=0V	VD(H) - COM	-	-	0.1	mA
I_{QDL}		$V_{D(L)}$=15V, $V_{IN(xL)}$=0V	VD(L) - COM	-	-	2.1	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS}=15V, $V_{IN(xH)}$=0V	VB(U)-U, VB(V)- V, VB(W)- W	-	-	0.3	mA
$V_{SC(REF)}$	Short-Circuit Trip Level	V_{DD}=15V (Note 2)		0.45	0.48	0.51	V
UV_{DDT}	Supply Circuit Under- Voltage Protection	Trip Level		10.3	11.4	12.5	V
UV_{DDR}		Reset Level		10.8	11.9	13.0	V
UV_{BST}		Trip Level		8.5	9.5	10.5	V
UV_{BSR}		Reset Level		9.5	10.5	11.5	V
V_{OT}	Temperature to Output Voltage (Note 3)	R_{PD}=10kΩ	LVIC Temperature=80°C	2.36	2.45	2.55	V
			LVIC Temperature=25°C	0.77	1.00	1.25	V
T_{OT}	Over-Temperature Protection (Note 4)	V_{DD}=15V	Trip Level	110	130	150	°C
$T_{OT(HYS)}$			Hysteresis of Trip Reset	-	30	-	°C
V_{CFH}	Fault Output Voltage	V_{SC}=0V, V_{CF} Circuit: 10kΩ to 5V pull-up		4.9	-	-	V
V_{CFL}		V_{SC}=1V, V_{CF} Circuit: 10kΩ to 5V pull-up		-	-	0.5	V
V_{CF+}	CF Positive Going Threshold			-	1.9	2.2	V
V_{CF-}	CF Negative Going Threshold			0.8	1.1	-	V
t_{FO}	Fault Output Pulse Width	(Note 5)		20	-	-	µs
I_{IN}	Input Bias Current	$V_{IN(xH)}$= $V_{IN(xL)}$=5V		-	1.0	-	mA
$V_{TH(ON)}$	ON Threshold Voltage	Between IN(UH), IN(VH), IN(WH), IN(UL), IN(VL), IN(WL) – COM			2.3	2.7	V
$V_{TH(OFF)}$	OFF Threshold Voltage			0.8	1.2		V
$V_{TH(HYS)}$	ON/OFF Threshold Hysteresis Voltage			-	1.1	-	V
$V_{F(BSD)}$	Bootstrap Diode Forward Voltage	I_F=10mA Including Voltage Drop by Limiting Resistor		-	0.8	-	V
R_{BSD}	Bootstrap Diode Equivalent Resistance			-	80	-	Ω

Notes:

2. Please select the external shunt resistance such that short-circuit trip-level is less than 1.7 times of the current rating.
3. The IPM does not shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that the user defined, the controller (MCU) should stop the IPM. Temperature of LVIC vs. V_{OT} output characteristics is described in Figure 4.
4. When the LVIC temperature exceeds OT Trip temperature level (T_{OT}), OT protection is triggered and fault outputs.
5. Fault signal (V_{CF}) outputs when SC, UV or OT protection is triggered. V_{CF} pulse width is different for each protection mode. At SC failure, V_{CF} pulse width is a fixed width (minimum 20µs), but at UV or OT failure, V_{CF} outputs continuously until recovering from UV or OT state.

Mechanical Characteristics and Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Mounting torque	Mounting Screw: M3	(Note 6)	0.59	0.69	0.78	N m
Weight			-	5.25	-	g
Flatness	Refer to Figure 2		-50	-	100	µm

Note:

6. Plain washers (ISO 7089-7094) are recommended.

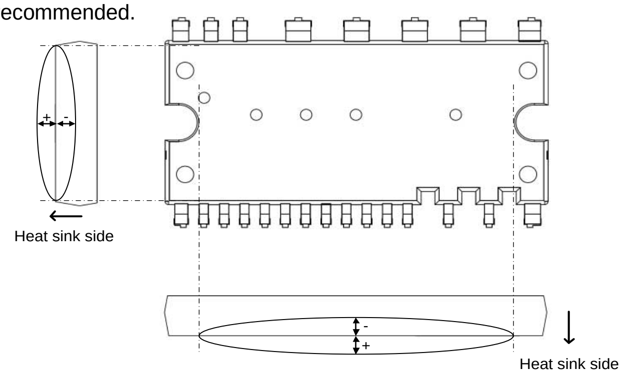


Figure 2. Flatness Measurement Positions

Recommended Operation Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{PN}	Supply Voltage	Between P-NU, NV, NW	0	300	400	V
V_{DD}	Control Supply Voltage	Between VD(H) – COM, VD(L) - COM	13.5	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Between VB(U)-U, VB(V)-V, VB(W)-W	13.5	15.0	18.5	V
dV_{DD}/dt, dV_{BS}/dt	Control Supply Variation		-1	-	1	V/µs
t_{dead}	Arm Shoot-Through Blocking Time	For each input signal	1.5	-	-	µs
f_{PWM}	PWM Input Frequency	-40°C < T_J < 150°C	-	-	20	kHz
$PW_{IN(ON)}$	Minimum Input Pulse Width (Note 7)		0.5	-	-	µs
$PW_{IN(OFF)}$			0.5	-	-	µs
COM	COM Variation	Between COM - NU, NV, NW (including surge)	-5.0	-	5.0	V

Note:

7. IPM may not respond if the input pulse width is less than $PW_{IN(ON)}$, $PW_{IN(OFF)}$.

Functional Descriptions

OT (Over temperature) Protection and Monitoring Circuit

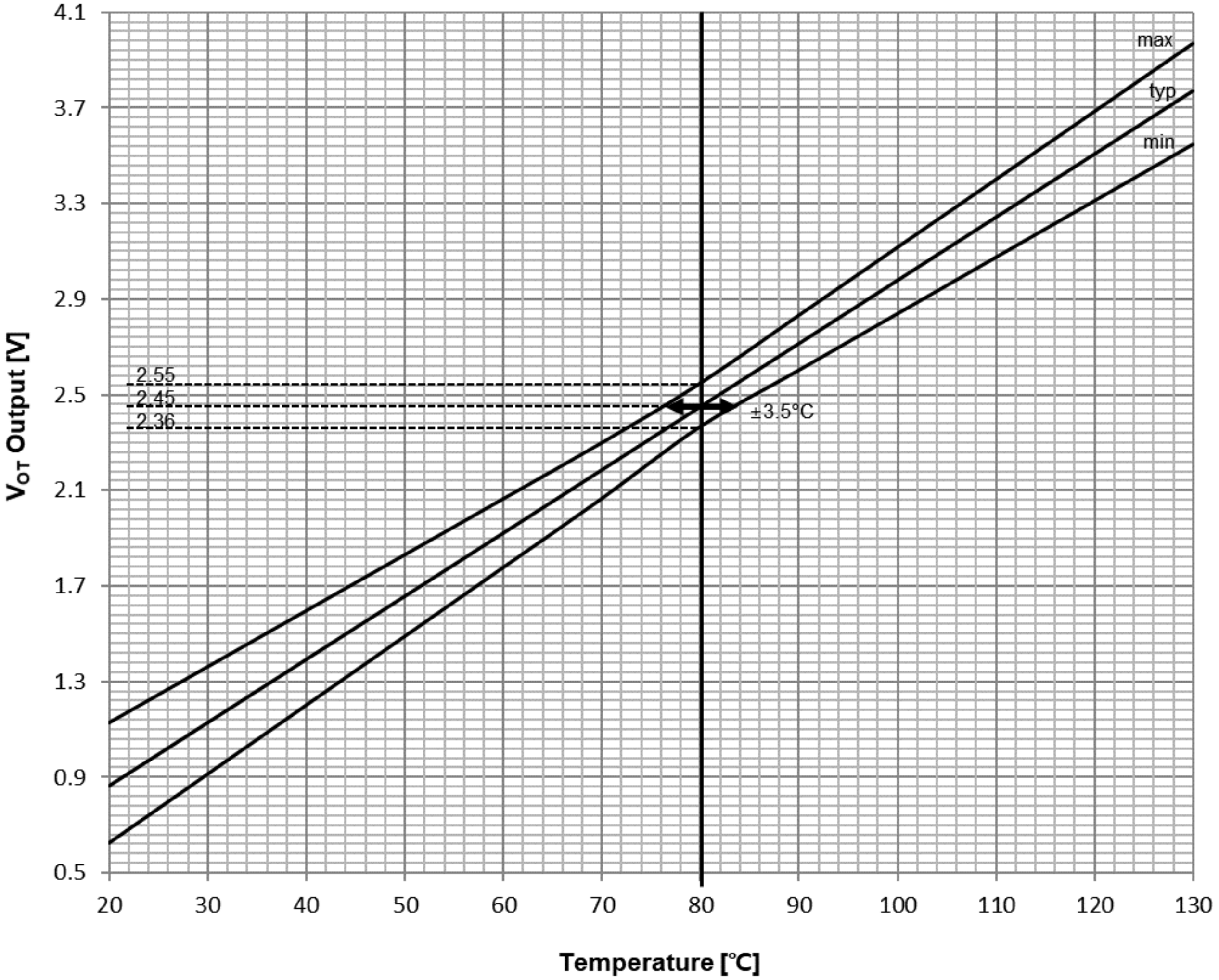


Figure 3. Temperature of LVIC vs. V_{OT} Output Characteristics

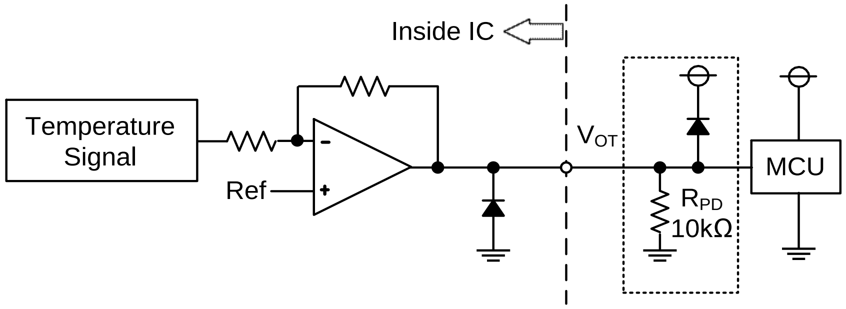


Figure 4. VOT Output Circuit

VOT configuration	Internal OT	Monitoring VOT
Adding external resistor	Disable	Enable
Open	Enable	Enable

(1) Both VOT function and OT (Over temperature) protection are simultaneously enabled without the pull-down resistor.

(2) If pull-down resistor (10kΩ) is connected to VOT pin, the temperature monitoring function is only used with disabling OT protection.

(3) Not to use VOT, leave VOT output with no-connection.

(4) When connecting VOT to MCU powered with e.g, 3.3V, V_{OT} output could exceed MCU supply voltage as temperature rises excessively. To prevent V_{OT} exceeding MCU supply voltage, it is recommended to insert a clamp diode between control supply of the controller and VOT output for preventing over voltage destruction.

Depending on temperature, V_{OT} will be out as shown in Figure 3.

Controllable Fault Output Circuit

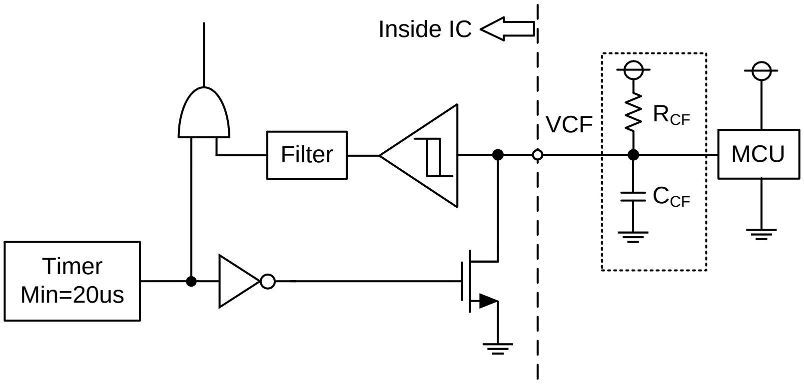


Figure 5. VCF Output Circuit

(1) The VCF pin combines three functions in one pin: Fixed fault out, Controllable fault out pulse width based on RC network, and Enable input.

(2) The VCF pin provides an enable functionality able to shut down the all low-side IGBTs. When the VCF pin is in the high state, the IPM operates normally. If the VCF pin is in a low state, the low-side IGBTs are turned off until the enable condition is restored. In addition, the VCF pin can provide the fault output signal with the fixed or controlled fault out pulse width.

(3) If a pull-up resistor (10kΩ) only is connected to the VCF pin, the fault output pulse width is fixed at minimum 20us.

(4) If VCF connects with a capacitor (C_{CF}) and a pull-up resistor (R_{CF}) together, the fault output pulse width t_{FO} can be controlled depending on time constant of R_{CF} and C_{CF}. The length of fault output pulse width is determined by the following equation;

$$t_{FO} = -(R_{CF} \cdot C_{CF}) \cdot \ln\left(1 - \frac{V_{CF+}}{V_{REF}}\right) + 20usec$$

For example, circuits configuration of typ V_{CF+}=1.9V, V_{REF}=5V, R_{CF}=2.2MΩ, C_{CF}=1nF will provide t_{FO} of approx. 1.07ms. In practical design, it is recommended that C_{CF} is 1nF or less and R_{CF} is 0.1M to 2.2MΩ.

Short-Circuit (SC) Protection and Time Chart

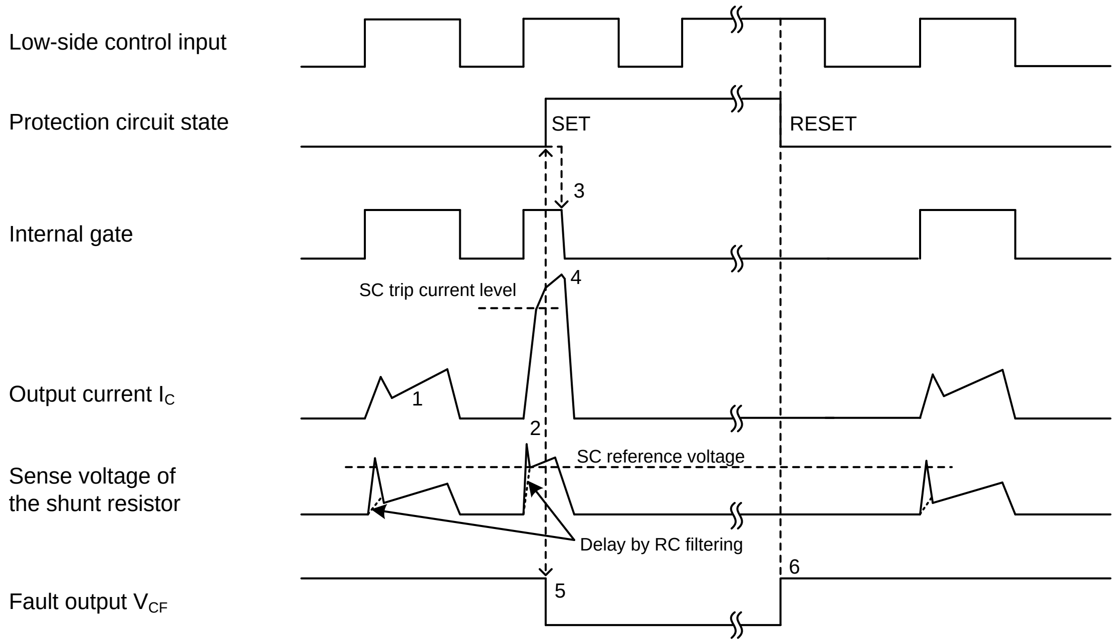


Figure 6. Short-Circuit Protection
(Low-side Operation Only with the External Shunt Resistor and RC Filter)

(1) Normal operation: IGBT turns on and output current.
(2) Short-circuit current detection (SC triggered).
(3) All low-side IGBTs' gate is turned off.
(4) Accordingly, all low-side IGBTs are turned off.
(5) Fault signal outputs. F_O duration time (t_{FO}) is minimum 20µs.
(6) Fault output finishes. Normal operation starts according to the input signal.

VDD Under-voltage Lock-out (UVLO) Protection and Time Chart

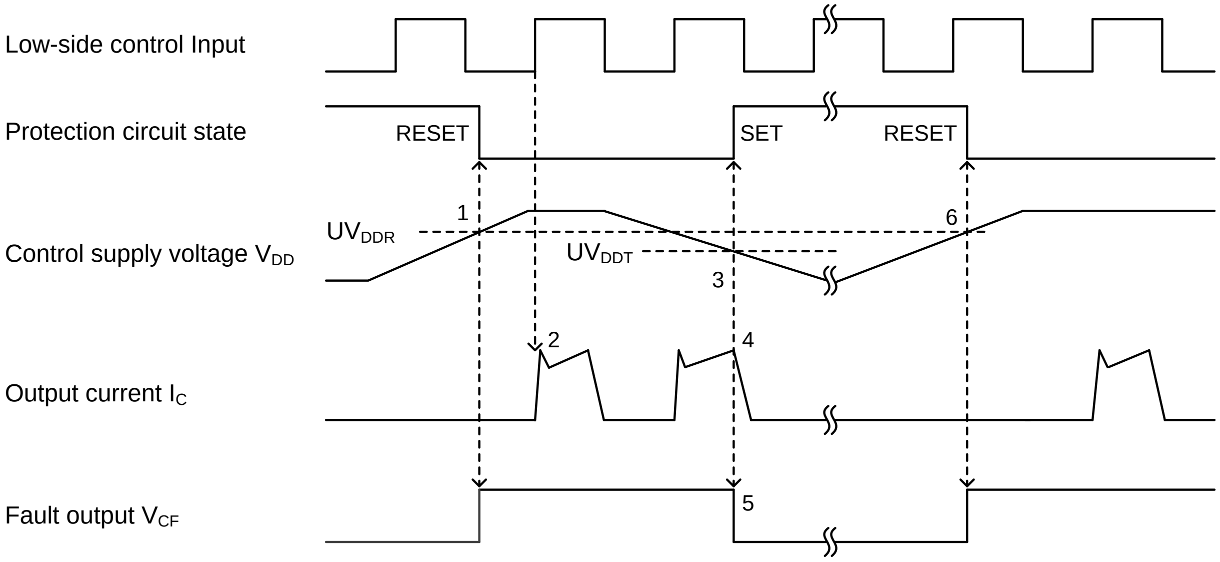


Figure 7. Under-Voltage Protection (Low-side, VDD)

(1) Supply voltage V_{DD} becomes higher than under-voltage reset level (UV_{DDR}), and IGBTs are turned at ON signal.

(2) Normal operation: IGBTs turn-on and output current.

(3) V_{DD} level drops to under-voltage trip level (UV_{DDT}).

(4) All low-side IGBTs are turned off regardless of control input condition.

(5) V_{CF} output is generated, and V_{CF} stays low as long as V_{DD} is below UV_{DDR}.

(6) V_{DD} level reaches UV_{DDR}. Normal operation starts according to the input signal.

VBS Under-voltage Lock-out (UVLO) Protection and Time Chart

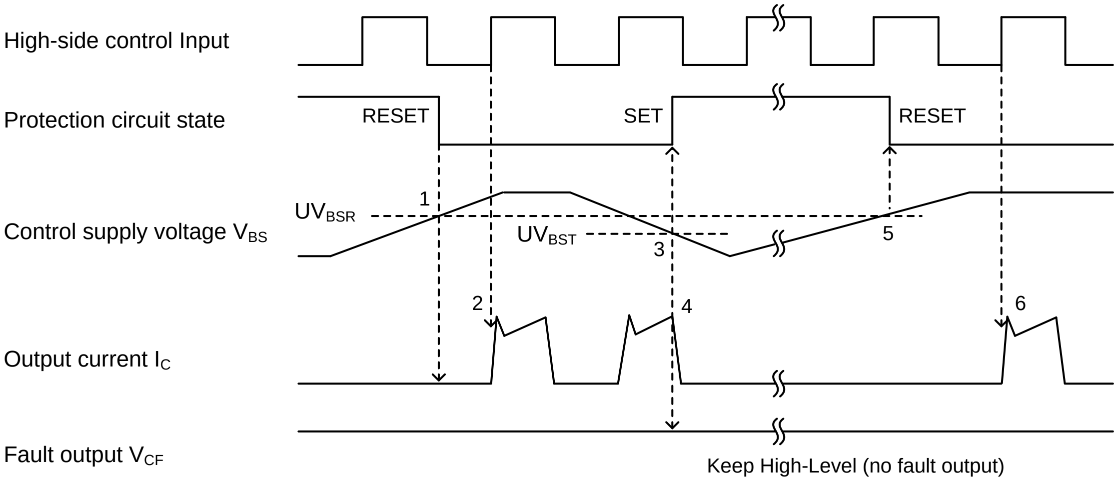


Figure 8. Under-Voltage Protection (High-side, V_{BS})

(1) Control supply voltage V_{BS} rises. After the voltage reaches under-voltage reset level (UV_{BSR}), IGBTs are turned on by the next ON signal.

(2) Normal operation: IGBTs turn on and output current.

(3) V_{BS} level drops to under-voltage trip level (UV_{BST}).

(4) All high-side IGBTs are turned off regardless of control input condition.

(5) V_{BS} level reaches UV_{BSR}.

(6) Normal operation starts according to the input signal.

Over Temperature (OT) Protection and Time Chart

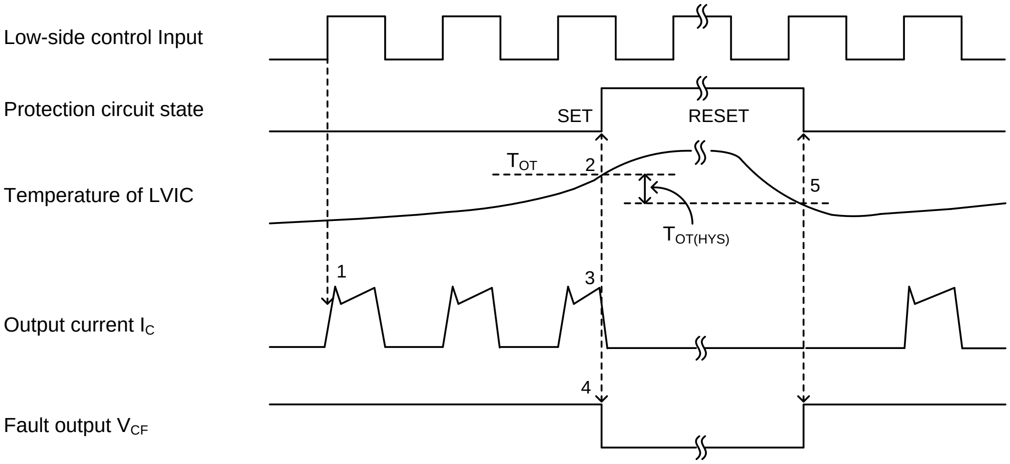
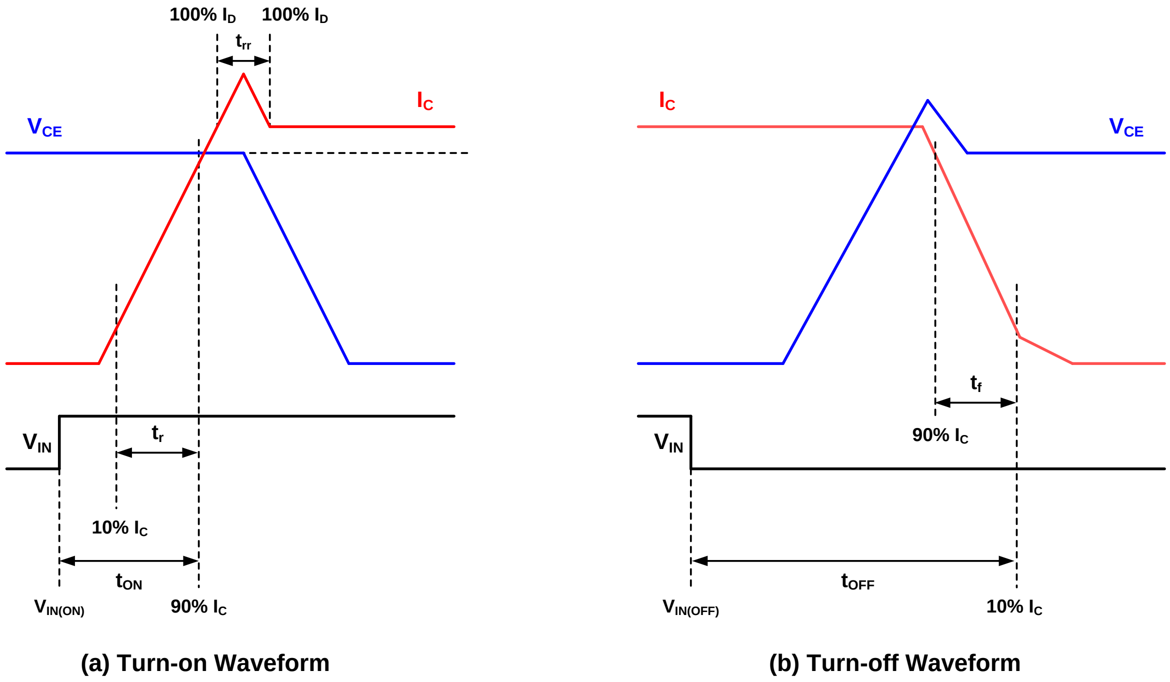


Figure 9. OT Protection (Low-side, Detecting LVIC Temperature)

(1) Normal operation: IGBTs turn on and output current.
(2) LVIC temperature exceeds over-temperature trip level (T_{OT}).
(3) All low-side IGBTs are turned off regardless of control input condition.
(4) VCF output is generated, and VCF stays low as long as LVIC temperature is over T_{OT}.
(5) LVIC temperature drops to over-temperature reset level (T_{OT}-$T_{OT(HYS)}$). Normal operation starts according to the input signal.

Switching Time Definition

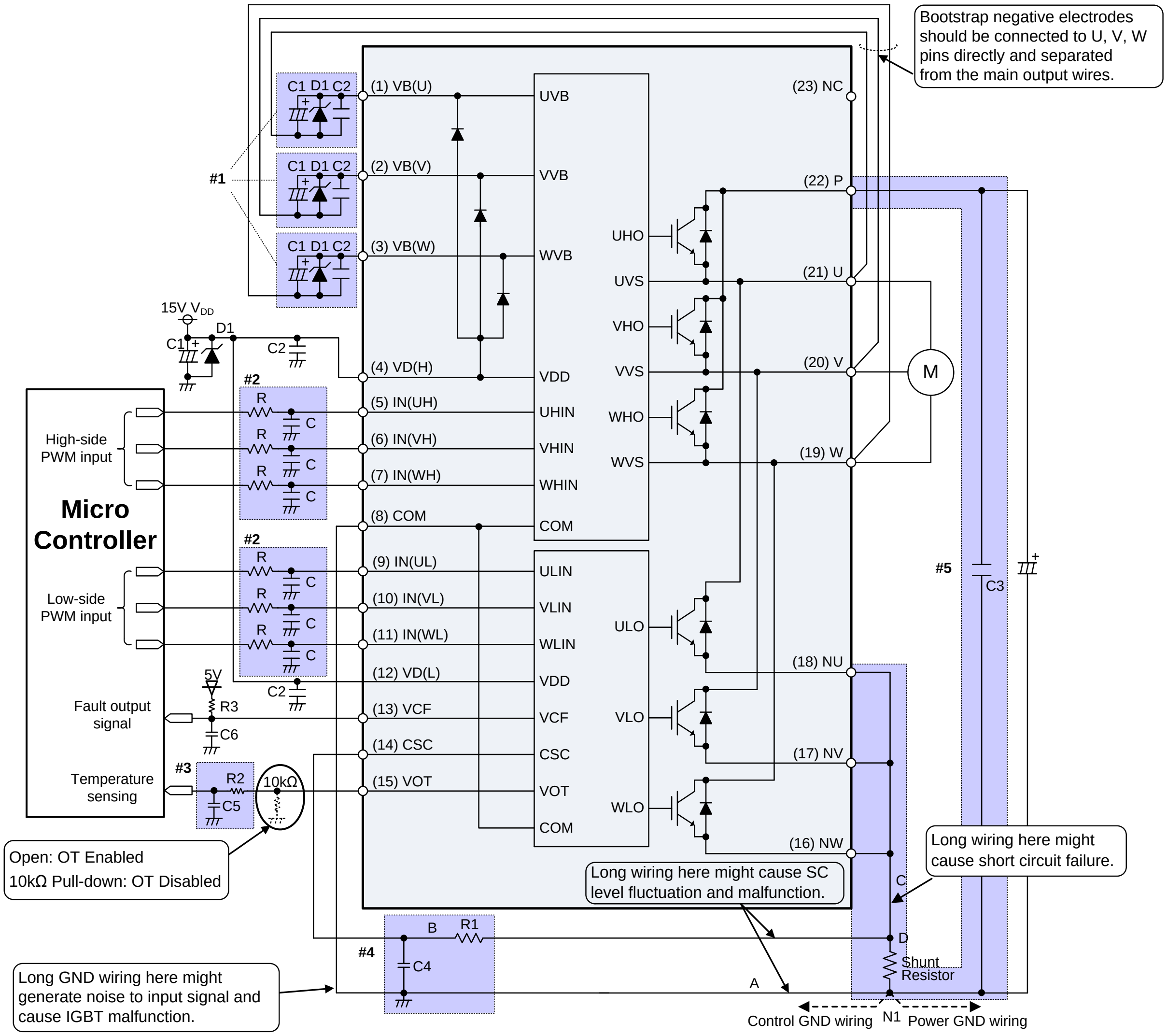


(a) Turn-on Waveform

(b) Turn-off Waveform

Figure 10. Switching Times Definition

Example of Application Circuit



Bootstrap negative electrodes should be connected to U, V, W pins directly and separated from the main output wires.

Open: OT Enabled
10kΩ Pull-down: OT Disabled

Long wiring here might cause SC level fluctuation and malfunction.

Long wiring here might cause short circuit failure.

Long GND wiring here might generate noise to input signal and cause IGBT malfunction.

Recommended Component Values:

(#1) C1:1~3.3µF, C2:100nF, D1:20V
(#2) R:100Ω, C:1nF
(#3) R2:2kΩ, C5:10nF
(#4) R1:1kΩ, C4:2nF
(#5) C3:0.1~0.22µF

(1) If the control GND is connected with the power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect the control GND and power GND at a single point (N1), near the terminal of the shunt resistor.

(2) A zener diode D1 (24V/1W) is recommended between each pair of control supply pins to prevent surge destruction.

(3) Prevention of surge destruction can further be improved by placing the bus capacitor as close to pins P and N1 as possible. Generally a 0.1-0.22µF snubber capacitor C3 between the P-N1 terminals is recommended.

(4) Selection of the R1*C4 filter components for short-circuit protection is recommended to have tight tolerance, and is temperature-compensated type. The R1*C4 time constant should be set such that SC current is shut down within 2µs; (typically 1.5-2µs). R1 and C4 should be placed as close as possible to the C_{SC} pin. SC interrupting time may vary with layout patterns and components selections, therefore thorough evaluation in the system is necessary.

(5) Tight tolerance, and temperature-compensated components are also recommended when selecting the R2*C5 filter for V_{OT}. The R2*C5 time constant should be set such that V_{OT} is immune to noise. Recommended values of R2 and C5 are 2kΩ and 10nF.

(6) To prevent malfunction, traces A, B, and C should be as short as possible.

(7) It is recommended that all capacitors are mounted as close to the IPM as possible. (C1: electrolytic type with good temperature and frequency characteristics. C2: ceramic type with 0.1-2µF, good temperature, frequency and DC bias characteristics.)

(8) Input drives are active-high. There is a minimum 3.5kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the layout to each input should be as short as possible. When using RC coupling circuit, make sure the input signal levels meet the required turn-on and turn-off threshold voltages.

(9) V_{CF} output is open drain type. It should be pulled up to MCU or control power supply (max= 5±0.5V), limiting the current (I_{FO}) to no more than 1mA. I_{FO} is estimated roughly by the formula of control power supply voltage divided by pull-up resistor R3. For example, if control supply is 5V, a 10kΩ (over 5kΩ) pull-up resistor R3 is recommended.

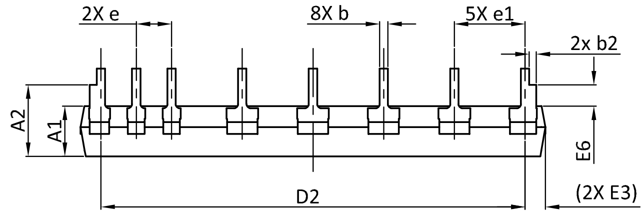
(10) If only a pull-up resistor R3 of 10kΩ connected to V_{CF} pin, the fault output pulse width is fixed at minimum 20us. If a capacitor C6 is connected with a pull-up resistor R3, the fault output pulse width can be controlled according to the resistor value and capacitor value. For the design guide, please refer to the Figure 4.

(11) Direct drive of the IPM from the MCU is possible without having to use opto-coupler or isolation transformer.

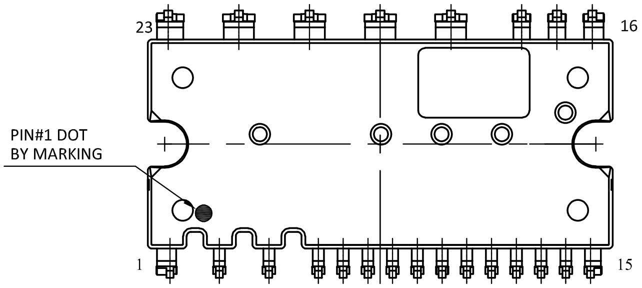
(12) The IPM may malfunction and erroneous operations may occur if high frequency noise is superimposed to the supply line. To avoid such problems, line ripple voltage is recommended to have dV/dt ≤ ±1V/µs, and Vripple ≤ 2Vp-p.

(13) It is not recommended to use the IPM to drive the same load in parallel with another IPM or inverter types.

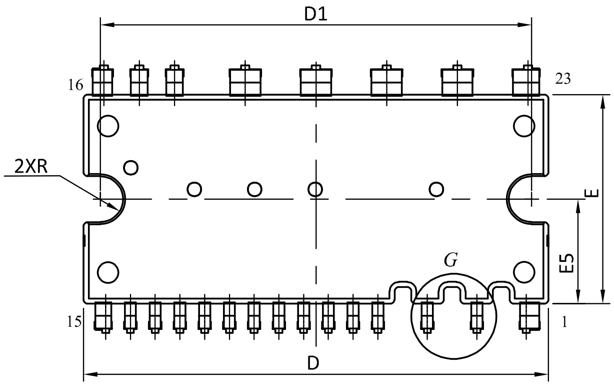
Package Dimensions, IPM-5A



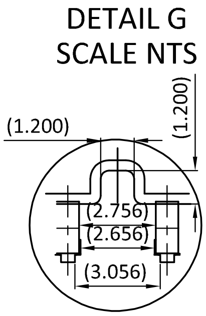
SIDE VIEW

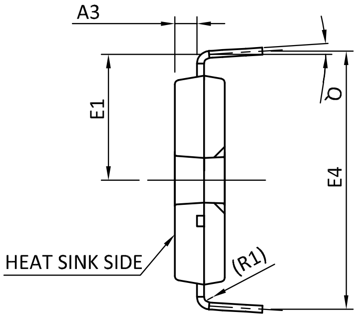


BOTTOM VIEW

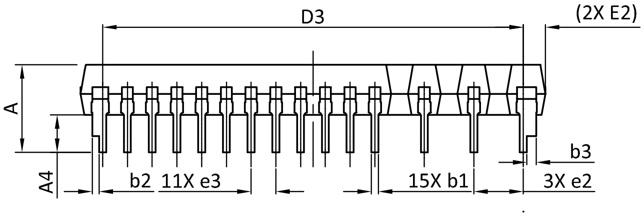


TOP VIEW



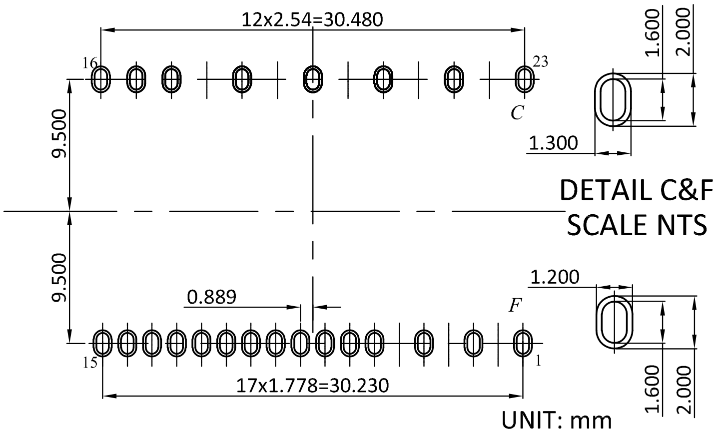


SIDE VIEW



SIDE VIEW

LAND PATTERN RECOMMENDATIONS



SYMBOLS	DIMENSION IN MILLIMETRES			DIMENSION IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	5.900	6.300	6.700	0.232	0.248	0.264
A1	3.400	3.600	3.800	0.134	0.142	0.150
A2	4.700	5.100	5.500	0.185	0.201	0.217
A3	1.500	1.600	1.700	0.059	0.063	0.067
A4	2.500	2.700	2.900	0.098	0.106	0.114
B	0.400	0.500	0.600	0.016	0.020	0.024
b	0.500	0.600	0.700	0.020	0.024	0.028
b1	0.400	0.500	0.600	0.016	0.020	0.024
b2	0.400	0.500	0.600	0.016	0.020	0.024
b3	0.600	0.700	0.800	0.024	0.028	0.031
D	33.100	33.400	33.700	1.303	1.315	1.327
D1	30.800	31.000	31.200	1.213	1.220	1.228
D2	30.180	30.480	30.780	1.188	1.200	1.212
D3	29.930	30.230	30.530	1.178	1.190	1.202
E	14.700	15.000	15.300	0.579	0.591	0.602
E1	8.600	9.000	9.400	0.339	0.354	0.370
E2	1.600REF			0.063REF		
E3	1.500REF			0.059REF		
E4	18.120	18.520	18.920	0.713	0.729	0.745
E5	7.300	7.500	7.700	0.287	0.295	0.303
E6	1.100	1.500	1.900	0.043	0.059	0.075
e	2.340	2.540	2.740	0.092	0.100	0.108
e1	4.880	5.080	5.280	0.192	0.200	0.208
e2	3.356	3.556	3.756	0.132	0.140	0.148
e3	1.578	1.778	1.978	0.062	0.070	0.078
R	1.500	1.600	1.700	0.059	0.063	0.067
R1	0.400REF			0.016REF		
Q	2° - 6°			2° - 6°		

NOTES
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS, MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
4. ( ) IS REFERENCE.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.