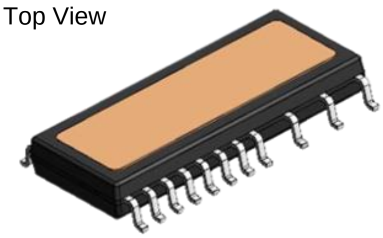
# AIM7DT1AR60V3

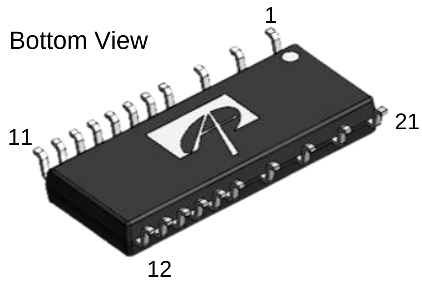
*Intelligent Power Module*

## External View

Top View



Bottom View




Size: 17.9 x 7.5 x 2.5 mm

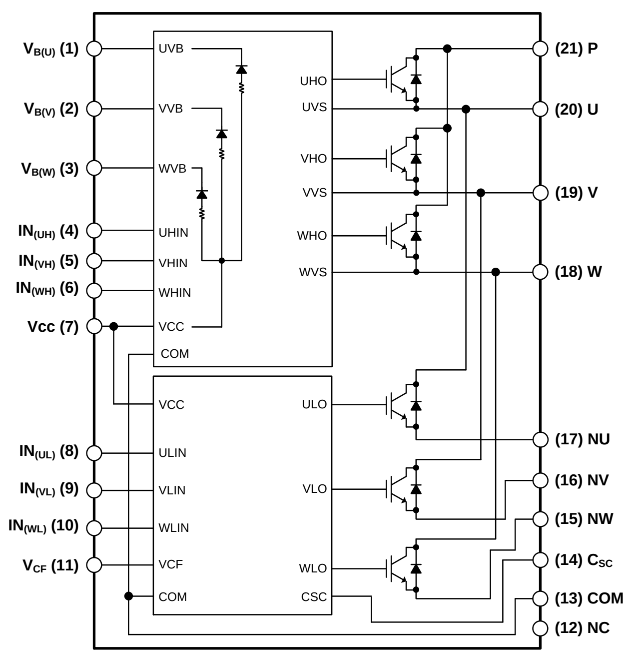
## Features

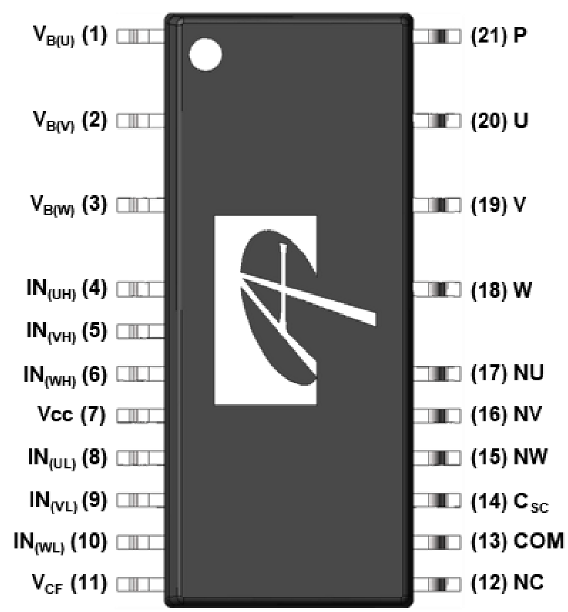
- 600V-1A
- Fully functional 3-phase IGBT-IPM
- Reverse conducting IGBT with monolithic body diode
- DBC-embedded SMD type
- Wide input interface (3-18V) with schmitt-trigger input circuit
- Built-in bootstrap diodes with current-limiting resistor
- Control supply under-voltage lockout protection (UVLO)
- Over-temperature (OT) protection
- Short-circuit current protection ($C_{SC}$)
- Controllable fault out signal ($V_{CF}$) corresponding to SC, UV, OT fault
- Isolation ratings of 1500Vrms/min

## Applications

- AC 100~240Vrms class low power motor drives
- Refrigerators, Dishwashers, Drain Pumps and Fan Motors

## Internal Equivalent Circuit / Pin Configuration



## Ordering Information

| Part Number | Package | Description |
|---|---|---|
| AIM7DT1AR60V3 | IPM-7DA | N/A |

RoHS Compliant

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1 | $V_{B(U)}$ | High-Side Bias Voltage for U-phase IGBT Driving |
| 2 | $V_{B(V)}$ | High-Side Bias Voltage for V-phase IGBT Driving |
| 3 | $V_{B(W)}$ | High-Side Bias Voltage for W-phase IGBT Driving |
| 4 | $IN_{(UH)}$ | Signal Input for High-Side U-phase |
| 5 | $IN_{(VH)}$ | Signal Input for High-Side V-phase |
| 6 | $IN_{(WH)}$ | Signal Input for High-Side W-phase |
| 7 | $V_{CC}$ | Control Supply Voltage |
| 8 | $IN_{(UL)}$ | Signal Input for Low-Side U-phase |
| 9 | $IN_{(VL)}$ | Signal Input for Low-Side V-phase |
| 10 | $IN_{(WL)}$ | Signal Input for Low-Side W-phase |
| 11 | $V_{CF}$ | Controllable Fault Output |
| 12 | NC | No connection |
| 13 | COM | Common Supply Ground |
| 14 | $C_{SC}$ | Capacitor (Low-Pass Filter) for Short-Circuit Current Detection Input |
| 15 | NW | Negative DC-Link Input for W-Phase |
| 16 | NV | Negative DC-Link Input for V-Phase |
| 17 | NU | Negative DC-Link Input for U-Phase |
| 18 | W | Output for W-phase |
| 19 | V | Output for V-phase |
| 20 | U | Output for U-phase |
| 21 | P | Positive DC-Link Input |

## Absolute Maximum Ratings ($T_J$=25°C, unless otherwise specified)

| Symbol | Parameter | Conditions | Ratings | Units |
|---|---|---|---|---|
| **Inverter** | | | | |
| $BV_{CES}$ | IGBT Breakdown Voltage | $T_J$=25°C | 600 | V |
| $I_C$ | IGBT Collector Current (Continuous) | $T_C$=25°C | 1 | A |
| | | $T_C$=80°C | 0.5 | A |
| $I_{CP}$ | IGBT Collector Current (Pulsed) | $T_C$=25°C, <100µs pulse width | 1.5 | A |
| $P_D$ | Maximum Power Dissipation | $T_C$=25°C | 35.7 | W |
| $T_J$ | Operating Junction Temperature | | -40 to 150 | °C |
| **Control (Protection)** | | | | |
| $V_{CC}$ | Control Supply Voltage | Applied between $V_{CC}$-COM | -0.3 ~ 20 | V |
| $V_{BS}$ | High-Side Control Bias Voltage | Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W | -0.3 ~ 20 | V |
| $V_{IN}$ | Input Voltage | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$-COM | -0.3 ~ $V_{CC}$+0.5 | V |
| $V_{CF}$ | Fault Output Supply Voltage | Applied between $V_{CF}$-COM | -0.3 ~ 5.5 | V |
| **Thermal Resistance** | | | | |
| $R_{th(j-c)Q}$ | Junction to Case Thermal Resistance | Single RC-IGBT | 2.8 | °C/W |
| $R_{th(j-c)F}$ | | Single Diode | 4 | °C/W |
| **Total System** | | | | |
| $T_C$ | Module Case Operation Temperature | | -30 to 125 | °C |
| $T_{STG}$ | Storage Temperature | | -40 to 150 | °C |
| $V_{ISO}$ | Isolation Voltage | 60Hz, sinusoidal, AC 1min, between connected all pins and heat sink plate | 1500 | $V_{rms}$ |

## Recommended Operation Conditions

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $V_{PN}$ | Bus Supply Voltage | Applied between P-N | 0 | 300 | 450 | V |
| $V_{CC}$ | Control Supply Voltage | Applied between $V_{CC}$-COM | 13.5 | 15.0 | 16.5 | V |
| $V_{BS}$ | High-Side Bias Voltage | Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W | 13.5 | 15.0 | 16.5 | V |
| $dV_{CC}/dt$, $dV_{BS}/dt$ | Control Supply Variation | | -1 | - | 1 | V/us |
| $t_{dead}$ | Arm Shoot-Through Blocking Time | For each input signal | 1.5 | - | - | µs |
| $f_{PWM}$ | PWM Input Frequency | -40°C < $T_J$ < 150°C | - | 16 | - | kHz |
| $PW_{IN(ON)}$ | Minimum Input Pulse Width | (Note 1) | 0.7 | - | - | µs |
| $PW_{IN(OFF)}$ | | | 0.7 | - | - | µs |

**Note:**

1. IPM may not respond if the input pulse width is less than $PW_{IN(ON)}$, $PW_{IN(OFF)}$.

## Electrical Characteristics ($T_J$=25°C, unless otherwise specified)

| Symbol | Parameter | Conditions | | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|---|
| **Inverter** | | | | | | | |
| $V_{CE(SAT)}$ | Collector-Emitter Saturation Voltage | $V_{CC}$=$V_{BS}$=15V, $V_{IN}$=5V | $I_C$=1A | - | 2.0 | 2.6 | V |
| $V_F$ | Emitter-Collector Forward Voltage | $V_{CC}$=$V_{BS}$=15V, $V_{IN}$=0 | $I_C$=1A | - | 2.4 | 2.9 | V |
| $t_{OFF}$ | Switching Times | $V_{PN}$=300V, $V_{CC}$=$V_{BS}$=15V<br>$I_C$=1A, $V_{IN}$=0V↔5V<br>Inductive load (high-side) | | - | 1000 | - | ns |
| $t_f$ | | | | - | 90 | - | ns |
| $t_{ON}$ | | | | - | 600 | - | ns |
| $t_r$ | | | | - | 50 | - | ns |
| $t_{rr}$ | | | | - | 210 | - | ns |
| $I_{CES}$ | Collector-Emitter Leakage Current | $V_{IN}$=0V, $V_{CE}$=600V | | - | - | 1 | mA |
| **Control (Protection)** | | | | | | | |
| $I_{QCC}$ | Quiescent $V_{CC}$ Supply Current | $V_{CC}$=15V, $IN_{(UL, VL, WL)}$=0V | $V_{CC}$-COM | - | - | 1.5 | mA |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | $V_{BS}$=15V, $IN_{(UH, VH, WH)}$=0V | $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W | - | - | 0.3 | mA |
| $UV_{CCT}$ | Supply Circuit Under- Voltage Protection | Trip Level | | 10.3 | 11.4 | 12.5 | V |
| $UV_{CCR}$ | | Reset Level | | 10.8 | 11.9 | 13.0 | V |
| $UV_{BST}$ | | Trip Level | | 9.0 | 10.0 | 11.0 | V |
| $UV_{BSR}$ | | Reset Level | | 10.0 | 11.0 | 12.0 | V |
| $V_{SC}$ | Short-Circuit Trip Level | $V_{CC}$=15V | | 0.45 | 0.48 | 0.51 | V |
| $OT_T$ | Over-Temperature Protection | $V_{CC}$=15V | Trip Level | 110 | 130 | 150 | °C |
| $OT_{HYS}$ | | | Hysteresis | - | 30 | - | °C |
| $V_{CFH}$ | Fault Output Voltage | $V_N$=0V | | 4.9 | - | - | V |
| $V_{CFL}$ | | $V_N$=1V | | - | - | 0.5 | V |
| $V_{CF+}$ | CF positive going threshold | | | - | 1.9 | 2.2 | V |
| $V_{CF-}$ | CF negative going threshold | | | 0.8 | 1.1 | - | V |
| $t_{FO}$ | Fault Output Pulse Width (Note 2) | | | 20 | - | - | µs |
| $I_{IN}$ | Input Current | $V_{IN}$=5V | | - | 650 | - | µA |
| $V_{TH(ON)}$ | ON Threshold Voltage | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ –COM | | - | - | 2.5 | V |
| $V_{TH(OFF)}$ | OFF Threshold Voltage | | | 0.8 | - | - | V |
| **Bootstrap Diode** | | | | | | | |
| $V_{F(BSD)}$ | Bootstrap Diode Forward Voltage | $I_F$=10mA including voltage drop by limiting resistor | | - | 3.6 | - | V |
| $R_{BSD}$ | Bootstrap Diode Equivalent Resistance | | | - | 360 | - | Ω |

**Note:**

2. Fault output signal $V_{CF}$ becomes low when one of protections OT, SC or UVLO is triggered. When failures happen like UV or OT, $V_{CF}$ keeps low continuously until recovering from UV or OT state. 20µs indicates min. fault output duration time without pull-down capacitor. It can be controlled by the capacitor value as shown in Figure 1.

# Functional Description

## Controllable Fault Output Circuit

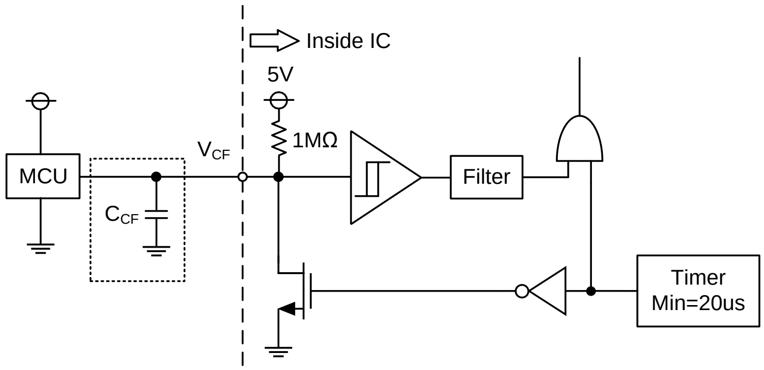



**Figure 1. $V_{CF}$ Output Circuit**

$V_{CF}$ pin provides an enable functionality that enables to shut down all low side IGBTs, besides it can be controlled with external MCU. When $V_{CF}$ is in the high state, the IPM is able to operate normally. Meanwhile, $V_{CF}$ is in a low state, the low-side IGBTs are turned off until $V_{CF}$ recovers to the high state. In addition, the $V_{CF}$ pin provides fixed or adjustable pulse width of fault output signal using external capacitor. If $V_{CF}$ pin is left, the fault output pulse width $t_{FO}$ is maintained as the low state for minimum 20us. If a capacitor is connected, the pulse width can be increased depending on to the capacitance.

The pulse width can be determined by the following formula;

$$t_{FO} = -(1M\Omega \cdot C_{CF}) \cdot ln\left(1 - \frac{V_{CF+}}{5V}\right) + 20usec$$

$$\approx 478k \cdot C_{CF} + 20usec$$

for example, adding $C_{CF}$=1nF, $t_{FO}$≈500us.

## Short-Circuit (SC) Protection and Time Chart

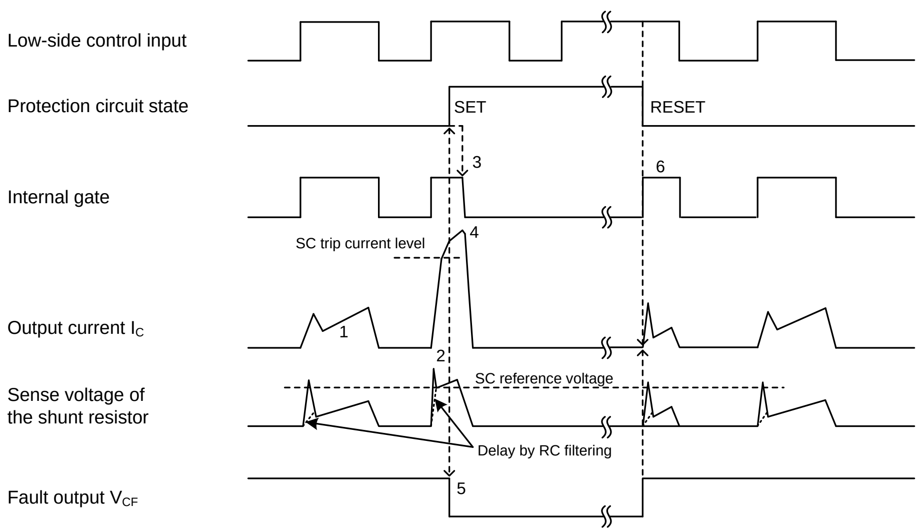



**Figure 2. Short-Circuit Protection**

**(Low-side Operation Only with External Shunt Resistor and RC Filter)**

(1) Normal operation: IGBT turns on and output current.
(2) Short-circuit current detection (SC triggered).
(3) All low-side IGBTs' gate are turned off.
(4) Accordingly, all low-side IGBTs are turned off.
(5) Fault signal outputs. $F_O$ duration time ($t_{FO}$) is minimum 20μs.
(6) Fault output finishes. Normal operation starts according to the input signal.

### $V_{CC}$ Under-voltage Lock-out (UVLO) Protection and Time Chart

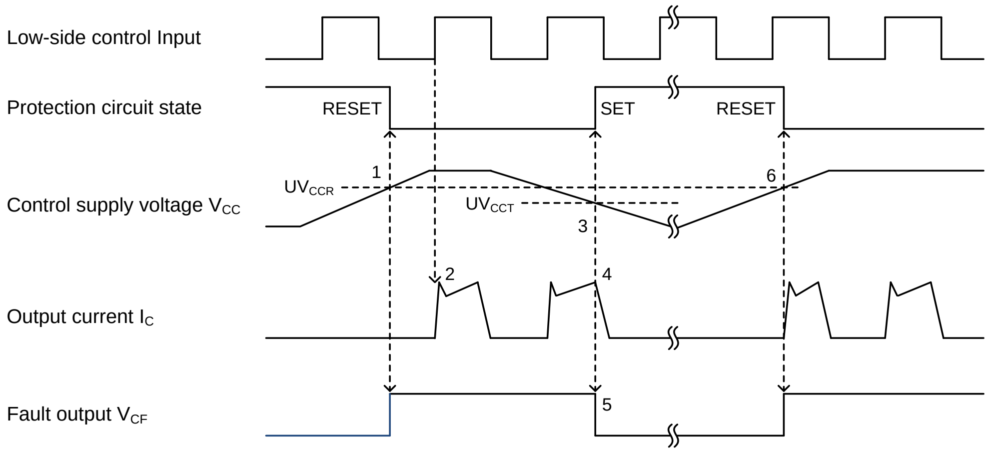



**Figure 3. Under-Voltage Protection (Low-side, $V_{CC}$)**

(1) Supply voltage $V_{CC}$ becomes higher than under-voltage reset level ($UV_{CCR}$), and IGBTs are turned at ON signal.
(2) Normal operation: IGBTs turn-on and output current.
(3) $V_{CC}$ level drops to under-voltage trip level ($UV_{CCT}$).
(4) All low-side IGBTs are turned off regardless of control input condition.
(5) $F_O$ output is generated, and $F_O$ stays low as long as $V_{CC}$ is below $UV_{CCR}$.
(6) $V_{CC}$ level reaches $UV_{CCR}$. Normal operation starts according to the input signal.

### $V_{BS}$ Under-voltage Lock-out (UVLO) Protection and Time Chart

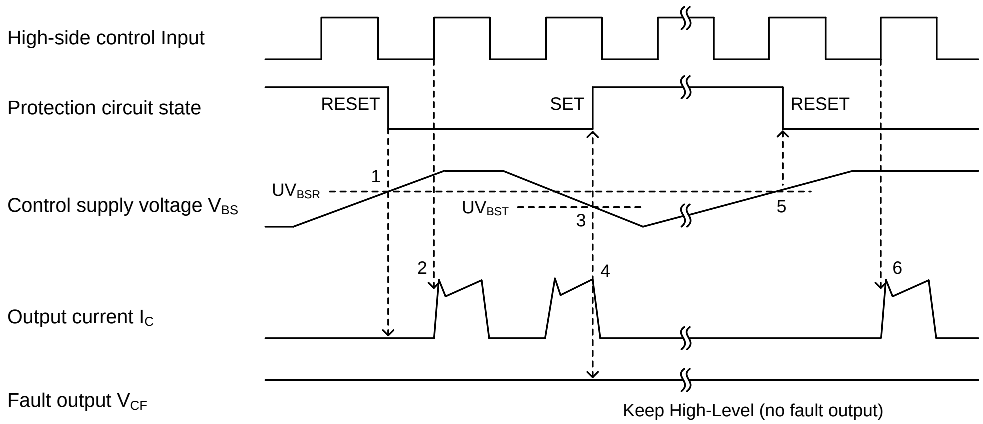



**Figure 4. Under-Voltage Protection (High-side, $V_{BS}$)**

(1) Control supply voltage $V_{BS}$ rises. After the voltage reaches under-voltage reset level ($UV_{BSR}$), IGBTs are turned on by the next ON signal.

(2) Normal operation: IGBTs turn on and output current.

(3) $V_{BS}$ level drops to under-voltage trip level ($UV_{BST}$).

(4) All high-side IGBTs are turned off regardless of control input condition.

(5) $V_{BS}$ level reaches $UV_{BSR}$.

(6) Normal operation starts according to the input signal.

## Over Temperature (OT) Protection and Time Chart

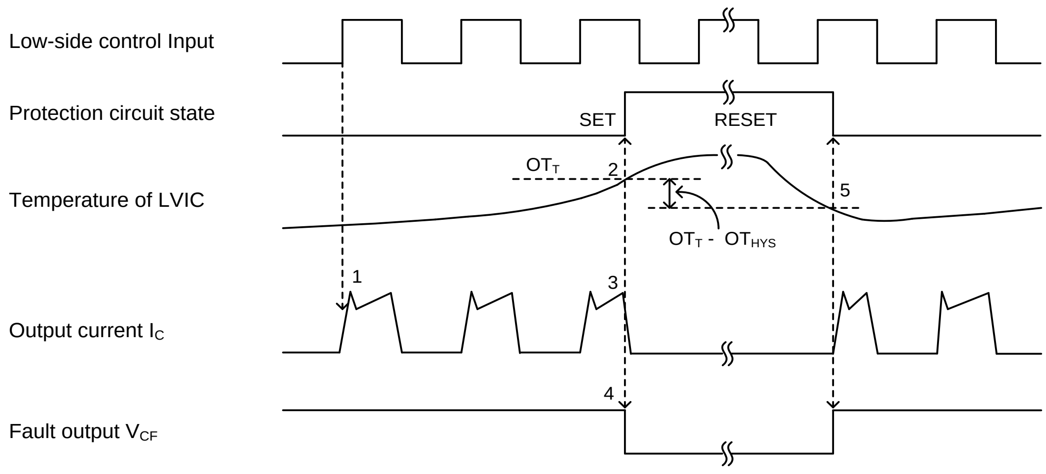



**Figure 5. Over-Temperature Protection (Low-side, Detecting LVIC Temperature)**

(1) Normal operation: IGBTs turn on and output current.

(2) LVIC temperature exceeds over-temperature trip level ($OT_T$).

(3) All low-side IGBTs are turned off regardless of control input condition.

(4) $F_O$ output is generated, and $F_O$ stays low as long as LVIC temperature is over $OT_T$.

(5) LVIC temperature drops to over-temperature reset level ($OT_T$-$OT_{HYS}$). Normal operation starts according to the input signal.

## Switching Time Definition

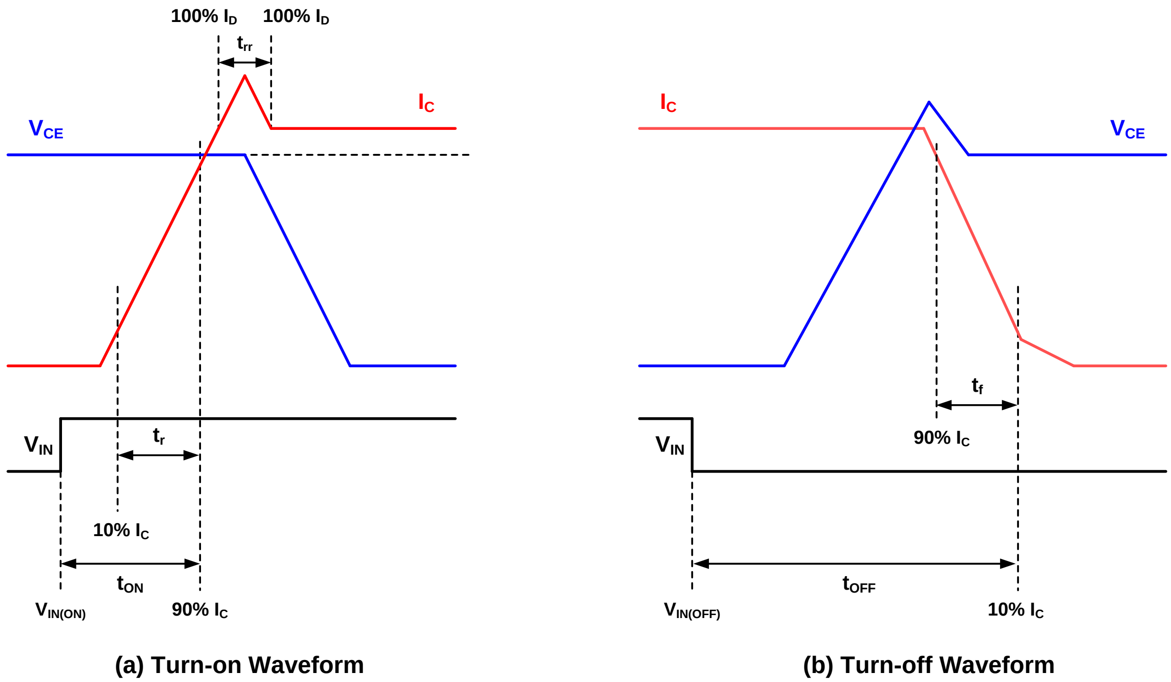
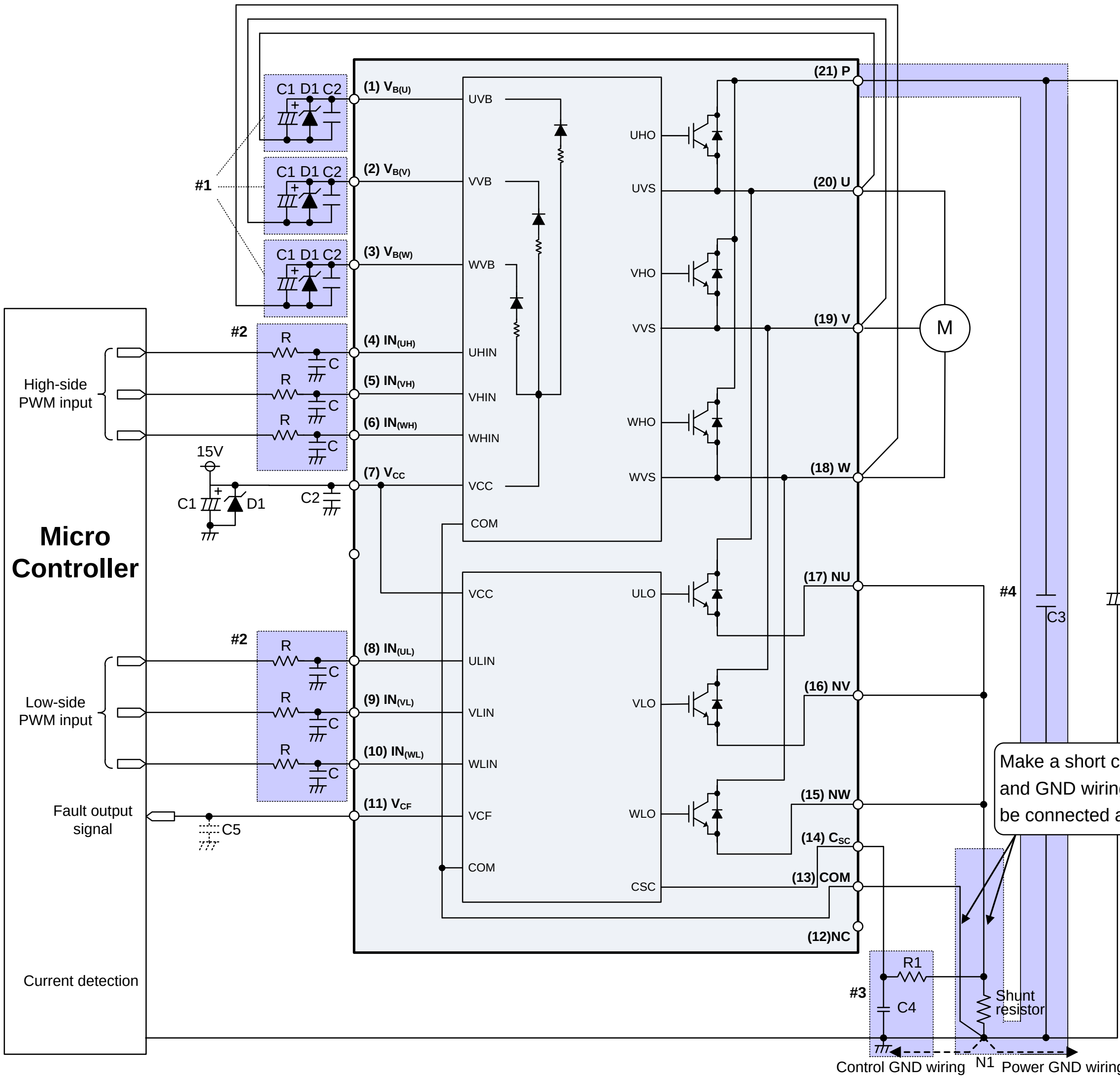



**Figure 6. Switching Times Definition**

## Example of Application Circuit




Recommended Component Values:

| | |
|---|---|
| (#1) C1:1~3.3µF, C2:100nF, D1:20V | (#2) R:100Ω, C:1nF |
| (#3) R1:1kΩ, C4:2nF | (#4) C3:0.1~0.22µF |

(1) If the control GND is connected with the power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect the control GND and power GND at a point (N1), near the terminal of shunt resistor.

(2) A zener diode D1 (20V/1W) is recommended between each pair of control supply pins to prevent surge destruction.

(3) Prevention of surge destruction can further be improved by placing the bus capacitor as close to pin P and N1 as possible. Generally a 0.1~0.22µF snubber capacitor C3 between the P-N1 terminals is recommended.

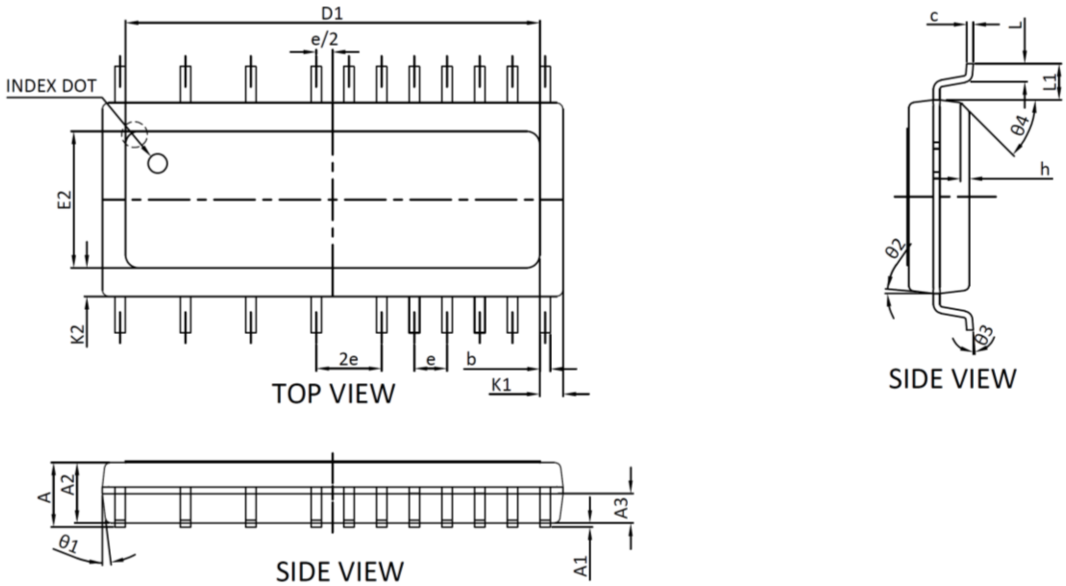
(4) Selection of the R1*C4 filter components for short-circuit protection is recommended to have tight tolerance, and is temperature-compensated type. The R1*C4 time constant should be set such that SC current is shut down within 2µs; (typically 1.5-2µs). R1 and C4 should be placed as close as possible to the $C_{SC}$ pin. SC interrupting time may vary with layout patterns and components selections, therefore thorough evaluation in the system is necessary.

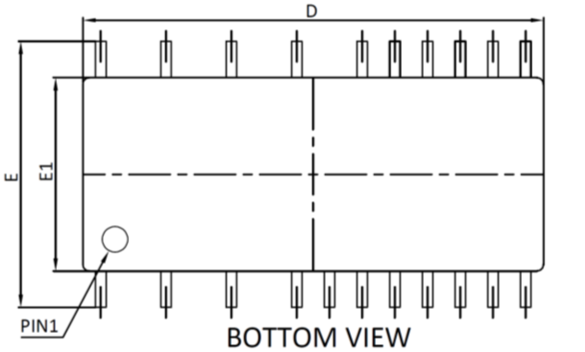
(5) It is recommended that all capacitors are mounted as close to the IPM as possible. (C1: electrolytic type with good temperature and frequency characteristics. C2: ceramic type with 0.1µF, good temperature, frequency and DC bias characteristics).

(6) To prevent malfunction, the layout to each input should be as short as possible. When using the RC coupling circuit (R: 100Ω, C: 1nF), place it as close to the IPM input pins as possible, and make sure the input signal levels meet the required turn-on and turn-off threshold voltages.

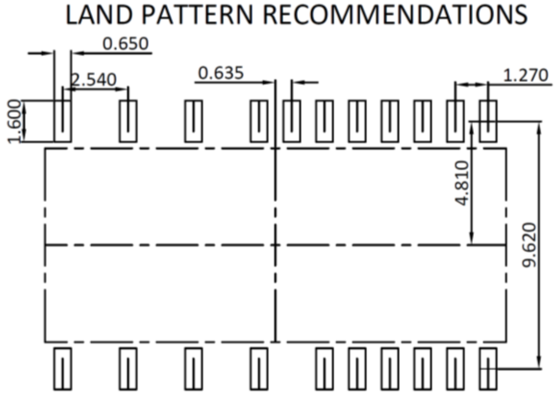
(7) The $V_{CF}$ pin can provide the fault output signal with the fixed or adjustable pulse width. If the $V_{CF}$ pin is left, the pulse width is fixed at minimum 20us. If a capacitor C5 is connected, the pulse width can be adjusted according to the capacitor value. For the design guide, please refer to the Figure 1.

## Package Dimensions, IPM-7DA




LAND PATTERN RECOMMENDATIONS




| SYMBOLS | DIMENSION IN MILLIMETRES | | | DIMENSION IN INCHS | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 2.304 | 2.504 | 2.704 | 0.091 | 0.099 | 0.106 |
| A1 | 0.050 | 0.150 | 0.250 | 0.002 | 0.006 | 0.010 |
| A2 | 2.254 | 2.354 | 2.454 | 0.089 | 0.093 | 0.097 |
| A3 | 1.050 | 1.150 | 1.250 | 0.041 | 0.045 | 0.049 |
| D | 17.800 | 17.900 | 18.000 | 0.701 | 0.705 | 0.709 |
| D1 | 16.000 | 16.100 | 16.200 | 0.630 | 0.634 | 0.638 |
| E | 10.140 | 10.340 | 10.540 | 0.399 | 0.407 | 0.415 |
| E1 | 7.420 | 7.520 | 7.620 | 0.292 | 0.296 | 0.300 |
| E2 | 5.200 | 5.300 | 5.400 | 0.205 | 0.209 | 0.213 |
| L | 0.505 | 0.705 | 0.905 | 0.020 | 0.028 | 0.036 |
| L1 | 1.210 | 1.410 | 1.610 | 0.048 | 0.056 | 0.063 |
| K1 | 0.700 | 0.900 | 1.100 | 0.028 | 0.035 | 0.043 |
| K2 | 0.910 | 1.110 | 1.310 | 0.036 | 0.044 | 0.052 |
| e | 1.270TYP. | | | 0.050TYP. | | |
| b | 0.410TYP. | | | 0.016TYP. | | |
| c | 0.254TYP. | | | 0.010TYP. | | |
| θ1 | 7°TYP. | | | 7°TYP. | | |
| θ2 | 7°TYP. | | | 7°TYP. | | |
| θ3 | 0° | --- | 8° | 0° | --- | 8° |
| θ4 | 45°TYP. | | | 45°TYP. | | |
| h | 0.381TYP. | | | 0.015TYP. | | |

UNIT: mm

NOTES

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS, MOLD FLASH SHOULD BE LESS THAN 6 MIL.
2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
3. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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