

### General Description

The AO4606 uses advanced trench technology MOSFETs to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

### Product Summary

#### N-Channel

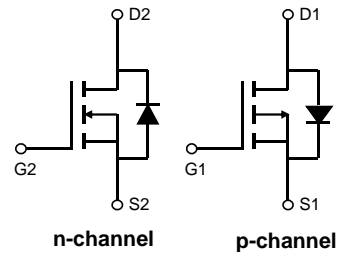
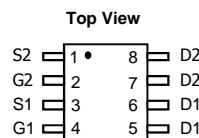
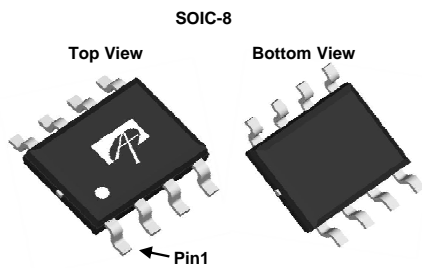
$V_{DS} = 30V$   
 $I_D = 6A$  ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 30m\Omega$  ( $V_{GS} = 10V$ )  
 $< 42m\Omega$  ( $V_{GS} = 4.5V$ )

100% UIS Tested  
 100%  $R_g$  Tested

#### P-Channel

$-30V$   
 $-6.5A$  ( $V_{GS} = -10V$ )  
 $R_{DS(ON)} < 28m\Omega$  ( $V_{GS} = -10V$ )  
 $< 44m\Omega$  ( $V_{GS} = -4.5V$ )

100% UIS Tested  
 100%  $R_g$  Tested



### Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	$V_{DS}$	30	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_A = 25^\circ C$	6	-6.5
		$T_A = 70^\circ C$	5	-5.3
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	30	-30	A
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	10	23	A
Avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AS}, E_{AR}$	5	26	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_A = 25^\circ C$	2	2
		$T_A = 70^\circ C$	1.3	1.3
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	48	62.5	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	74	90
Maximum Junction-to-Lead	$R_{\theta JL}$	32	40	$^\circ C/W$









**P-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.3	-1.85	-2.4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-6.5A T <sub>J</sub> =125°C		22 32	28 40	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5A		34	44	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-6.5A		18		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.8	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-2.5	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz		760		pF
C <sub>oss</sub>	Output Capacitance			140		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			95		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1.5	3.2	5	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-6.5A		13.6	16	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			6.7	8	nC
Q <sub>gs</sub>	Gate Source Charge			2.5		nC
Q <sub>gd</sub>	Gate Drain Charge			3.2		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =2.3Ω, R <sub>GEN</sub> =3Ω		8		ns
t <sub>r</sub>	Turn-On Rise Time			6		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			17		ns
t <sub>f</sub>	Turn-Off Fall Time			5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-6.5A, dI/dt=100A/μs		15		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-6.5A, dI/dt=100A/μs		9.7		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

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P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

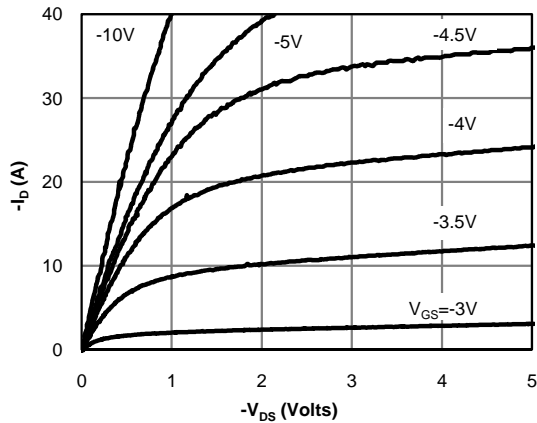


Fig 1: On-Region Characteristics (Note E)

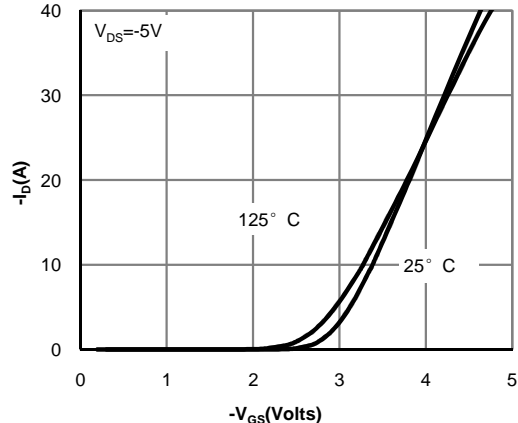


Figure 2: Transfer Characteristics (Note E)

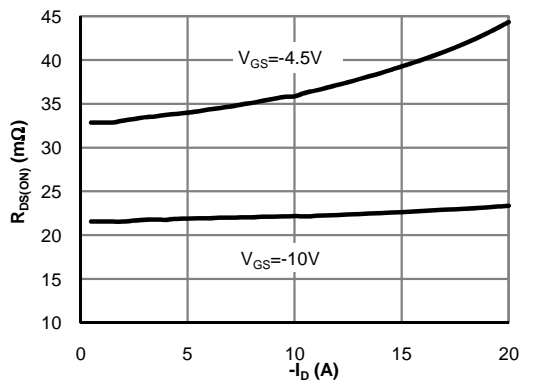


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

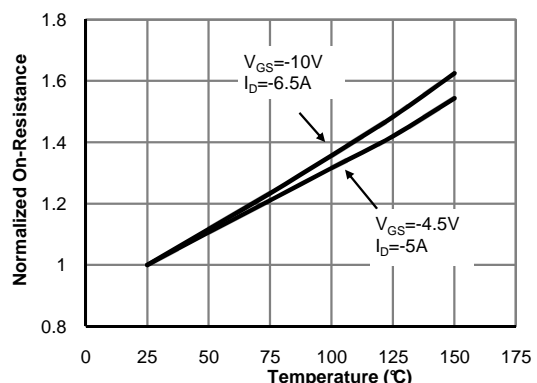


Figure 4: On-Resistance vs. Junction Temperature (Note E)

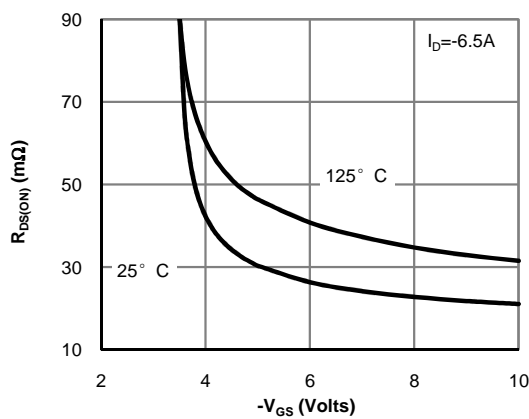


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

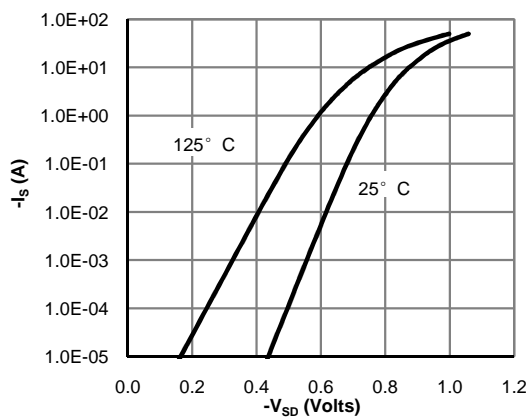


Figure 6: Body-Diode Characteristics (Note E)

P-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

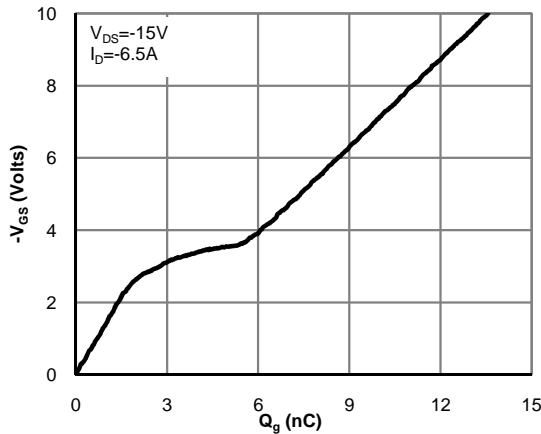


Figure 7: Gate-Charge Characteristics

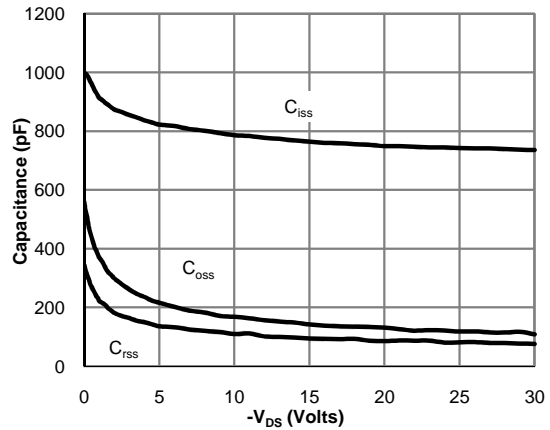


Figure 8: Capacitance Characteristics

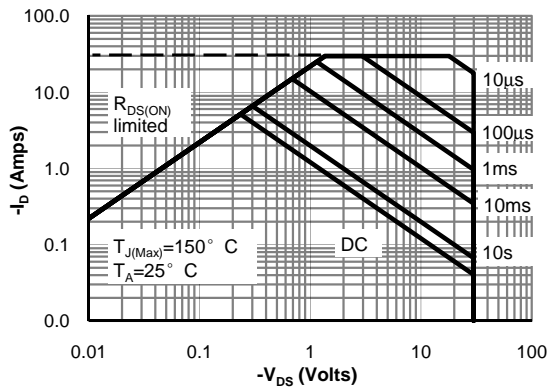


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

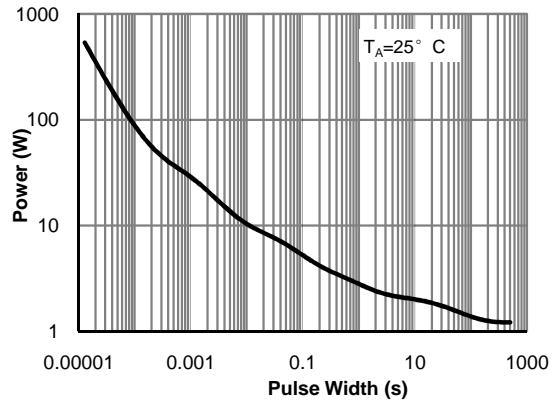


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

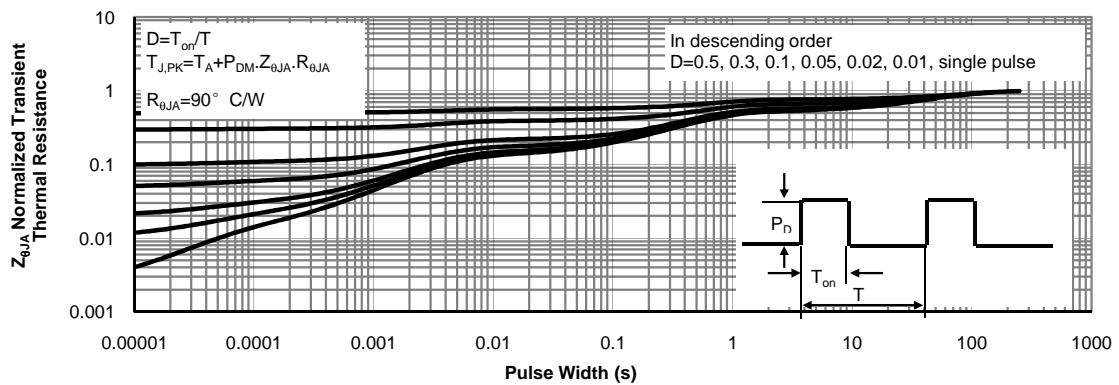
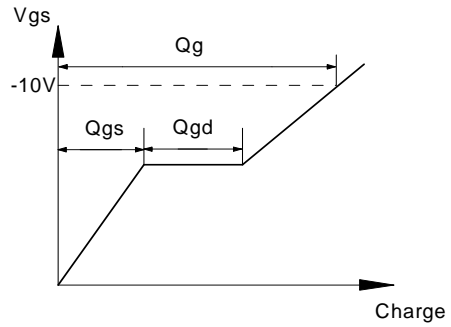
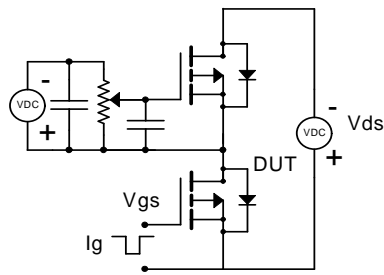


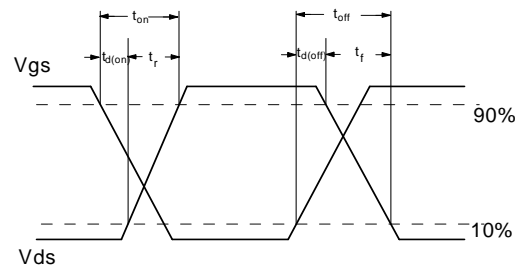
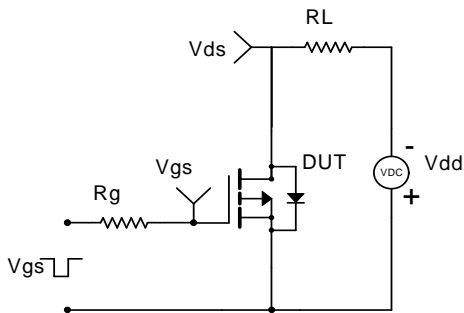
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



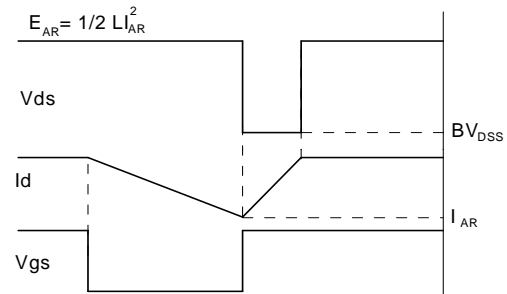
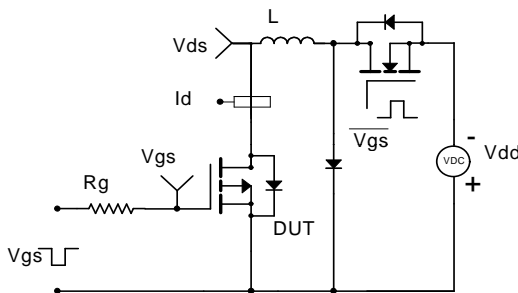
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

