

AOD417

P-Channel Enhancement Mode Field Effect Transistor

General Description

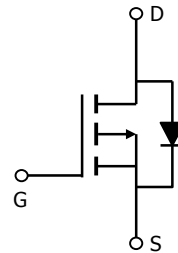
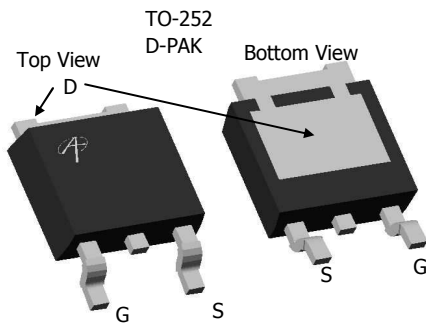
The AOD417 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications.

- RoHS Compliant
- Halogen Free*

Features

V_{DS} (V) = -30V
 I_D = -25A (V_{GS} = -10V)
 $R_{DS(ON)}$ < 34m Ω (V_{GS} = -10V)
 $R_{DS(ON)}$ < 55m Ω (V_{GS} = -4.5V)

100% UIS Tested!
100% Rg Tested!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|---|----------------|-------------------------------------|------------------|
| Drain-Source Voltage | V_{DS} | -30 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current ^{B,G} | I_D | $T_A=25^\circ\text{C}$ ^G | -25 |
| | | $T_A=100^\circ\text{C}$ | -20 |
| Pulsed Drain Current ^C | I_{DM} | -60 | A |
| Avalanche Current ^C | I_{AR} | -14 | A |
| Repetitive avalanche energy $L=0.3\text{mH}$ ^C | E_{AR} | 30 | mJ |
| Power Dissipation ^B | P_D | $T_C=25^\circ\text{C}$ | 50 |
| | | $T_C=100^\circ\text{C}$ | 25 |
| Power Dissipation ^A | P_{DSM} | $T_A=25^\circ\text{C}$ | 2.5 |
| | | $T_A=70^\circ\text{C}$ | 1.6 |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 175 | $^\circ\text{C}$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|--|-----------------|--------------|-----|--------------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | 16.7 | 25 | $^\circ\text{C/W}$ |
| Maximum Junction-to-Ambient ^A | | Steady-State | 40 | 50 |
| Maximum Junction-to-Case ^D | $R_{\theta JC}$ | 2.5 | 3 | $^\circ\text{C/W}$ |

Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|-----|-------|------|-------|
| STATIC PARAMETERS | | | | | | |
| B _V DSS | Drain-Source Breakdown Voltage | I _D =-250μA, V _{GS} =0V | -30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =-24V, V _{GS} =0V | | | -1 | μA |
| | | T _J =55°C | | | -5 | |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} =±20V | | | ±100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} I _D =-250μA | -1 | -1.9 | -3 | V |
| I _{D(ON)} | On state drain current | V _{GS} =-10V, V _{DS} =-5V | -60 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =-10V, I _D =-20A | | 27 | 34 | mΩ |
| | | T _J =125°C | | 36 | | |
| | | V _{GS} =-4.5V, I _D =-7A | | 40 | 55 | mΩ |
| g _{FS} | Forward Transconductance | V _{DS} =-5V, I _D =-20A | | 18 | | S |
| V _{SD} | Diode Forward Voltage | I _S =-1A, V _{GS} =0V | | -0.75 | -1 | V |
| I _S | Maximum Body-Diode Continuous Current | | | | -6 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =-15V, f=1MHz | | 920 | | pF |
| C _{oss} | Output Capacitance | | | 140 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 90 | | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | | 6 | 9 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _{g(10V)} | Total Gate Charge (10V) | V _{GS} =-10V, V _{DS} =-15V, I _D =-20A | | 16.2 | | nC |
| Q _{g(4.5V)} | Total Gate Charge (4.5V) | | | 8.2 | | nC |
| Q _{gs} | Gate Source Charge | | | 2.9 | | nC |
| Q _{gd} | Gate Drain Charge | | | 3.6 | | nC |
| t _{D(on)} | Turn-On DelayTime | | | 8 | | ns |
| t _r | Turn-On Rise Time | V _{GS} =-10V, V _{DS} =-15V, R _L =0.75Ω, | | 30 | | ns |
| t _{D(off)} | Turn-Off DelayTime | R _{GEN} =0.75Ω | | 22 | | ns |
| t _f | Turn-Off Fall Time | | | 26 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =-20A, dI/dt=100A/μs | | 23 | | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =-20A, dI/dt=100A/μs | | 14 | | nC |

A: The value of R_{θJA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} (<10s) and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev1: Sep. 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

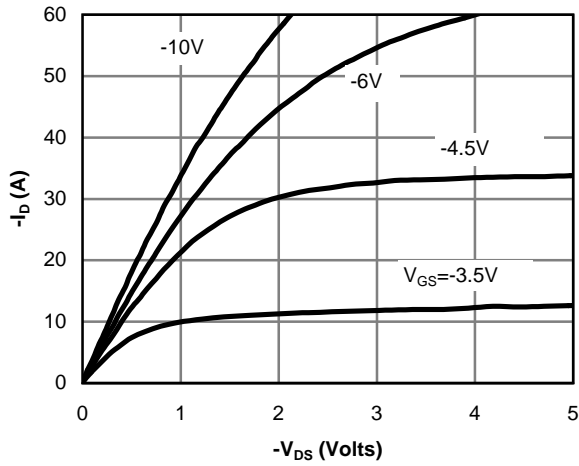


Figure 1: On-Region Characteristics

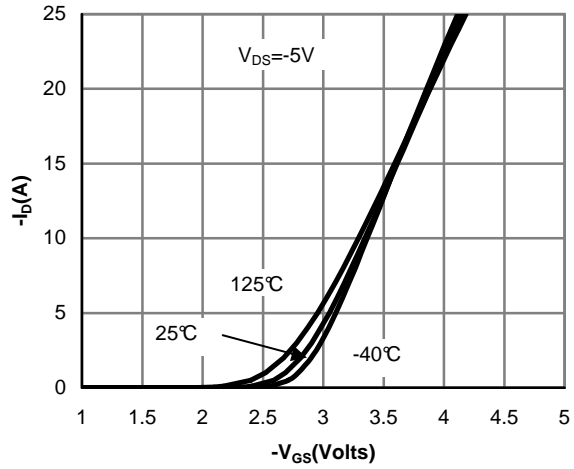


Figure 2: Transfer Characteristics

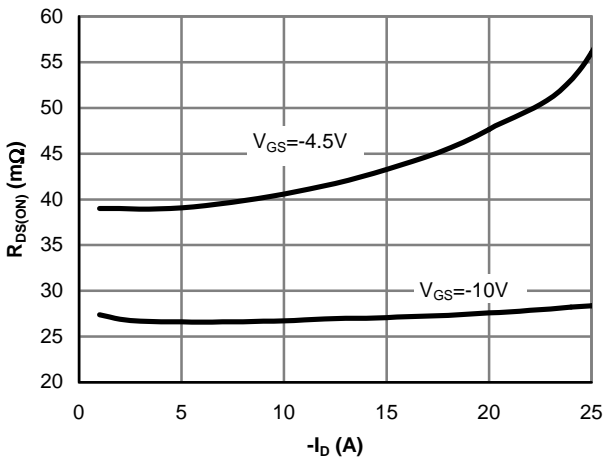


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

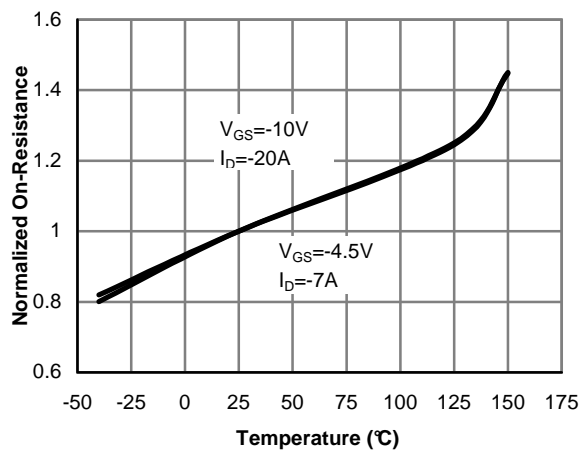


Figure 4: On-Resistance vs. Junction Temperature

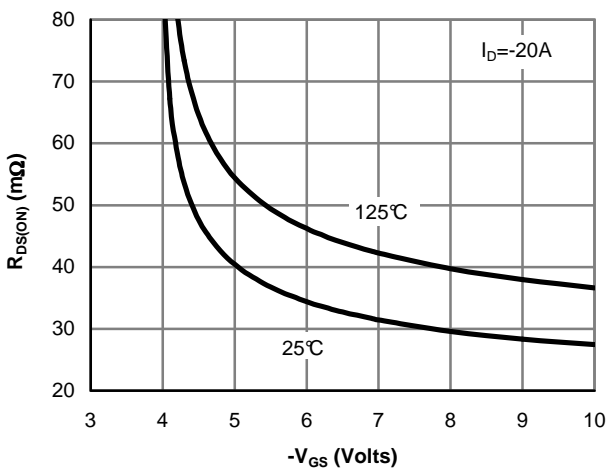


Figure 5: On-Resistance vs. Gate-Source Voltage

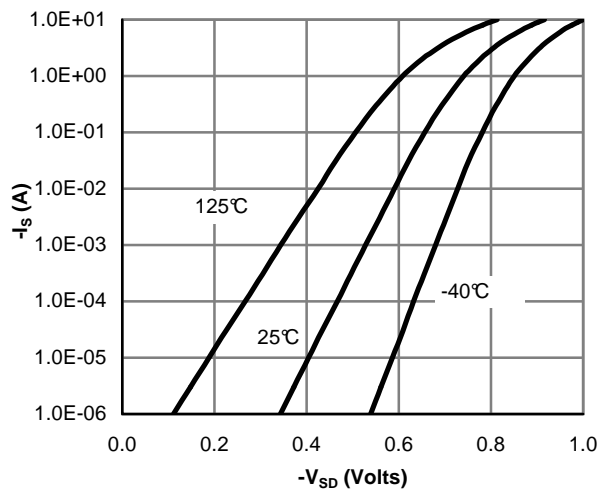


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

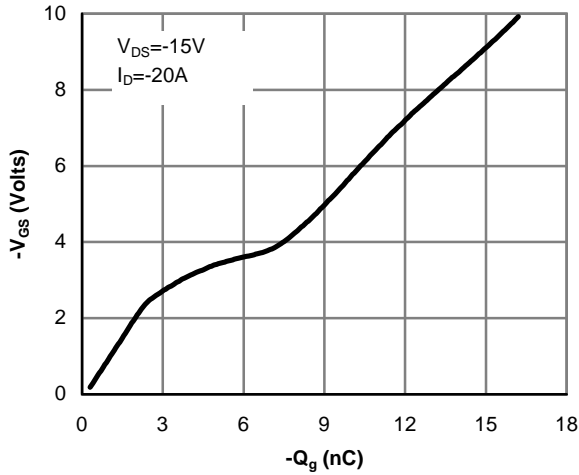


Figure 7: Gate-Charge Characteristics

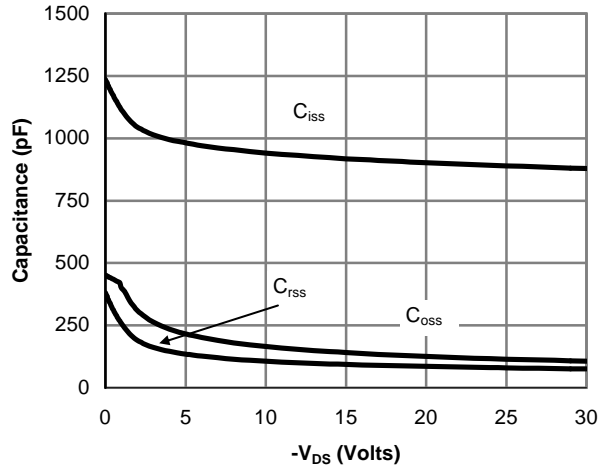


Figure 8: Capacitance Characteristics

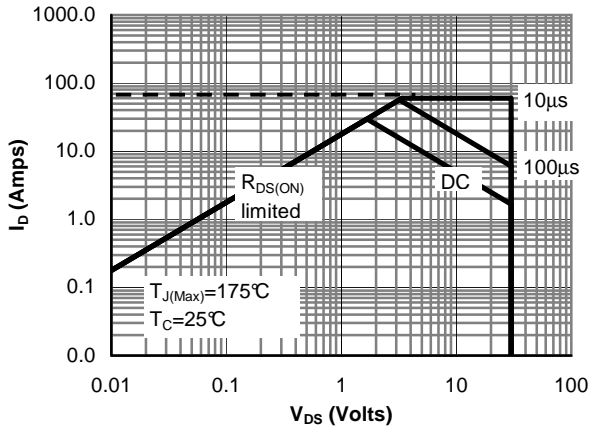


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

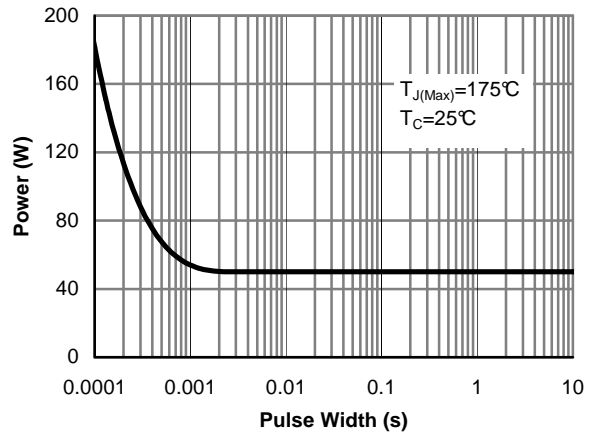


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

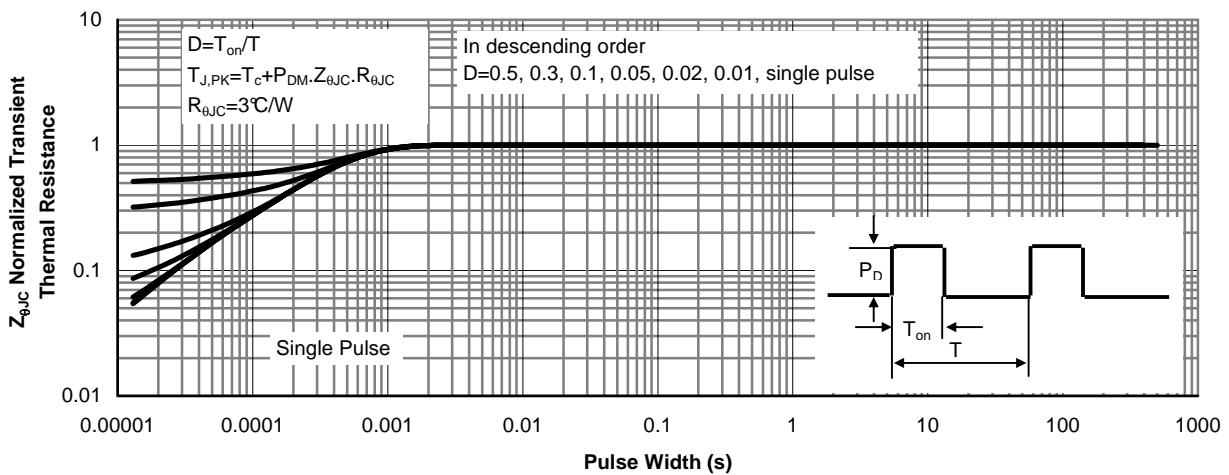


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

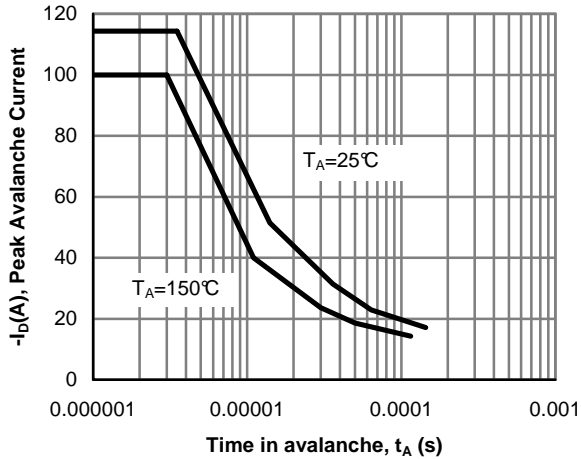


Figure 12: Single Pulse Avalanche capability

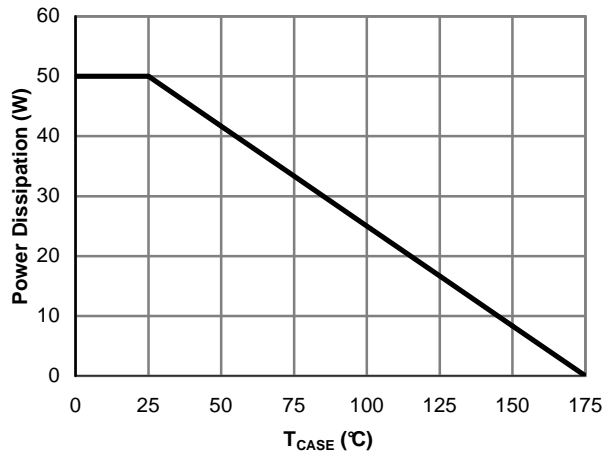


Figure 13: Power De-rating (Note B)

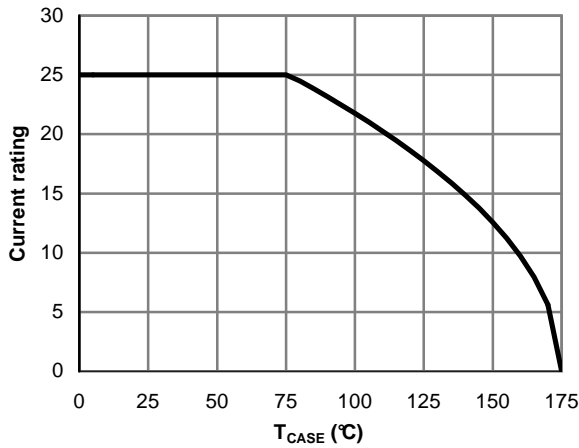


Figure 14: Current De-rating (Note B)

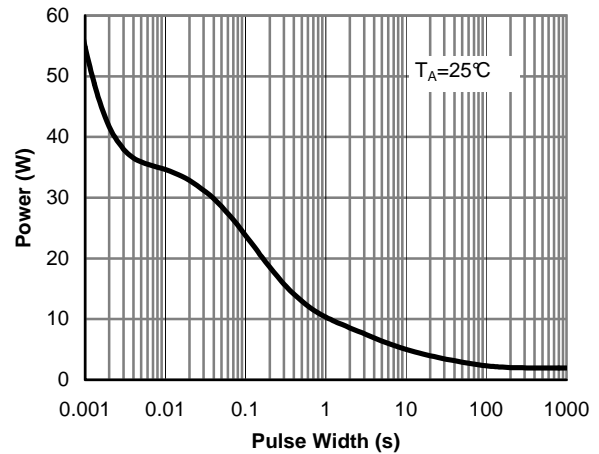


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

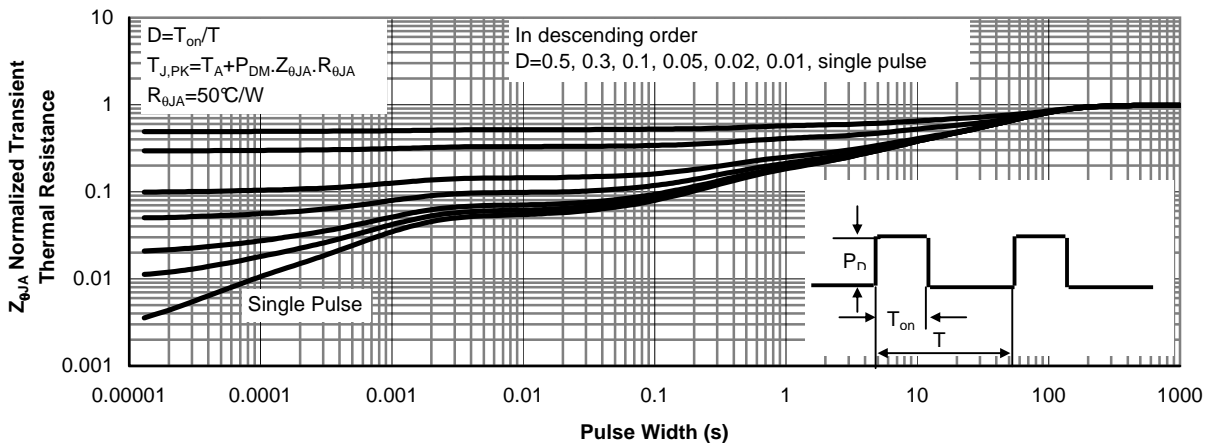
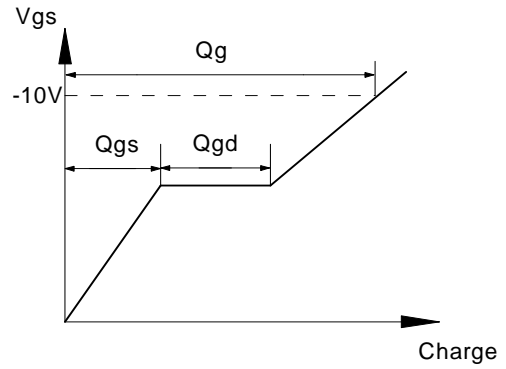
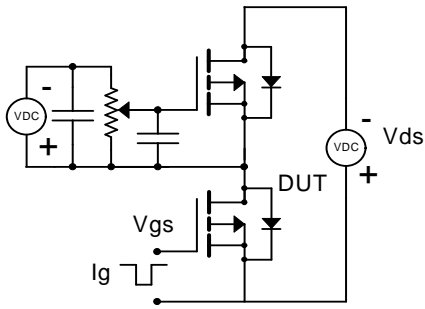
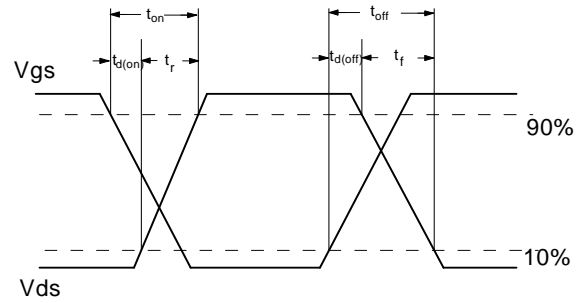
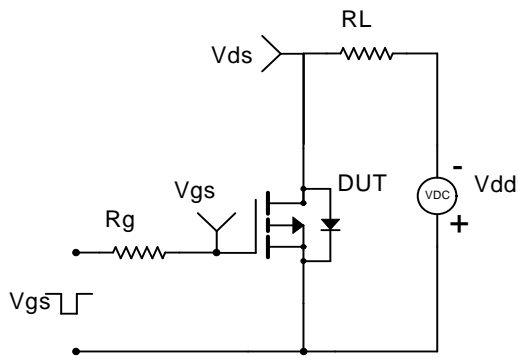


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

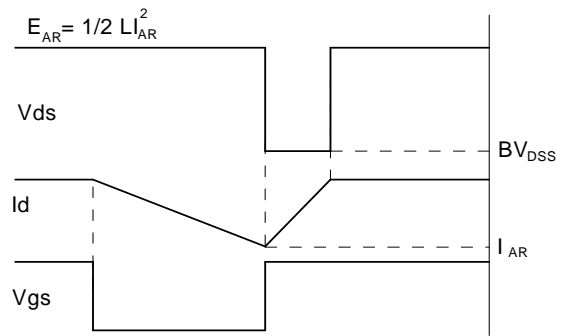
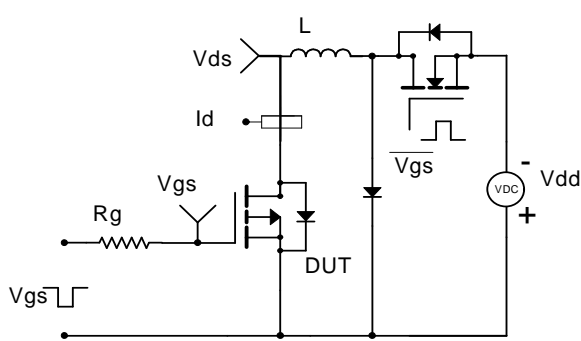
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

