

## AON4805L

### Dual P-Channel Enhancement Mode Field Effect Transistor

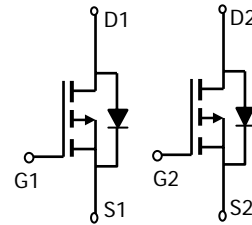
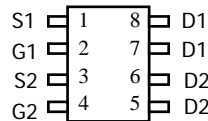
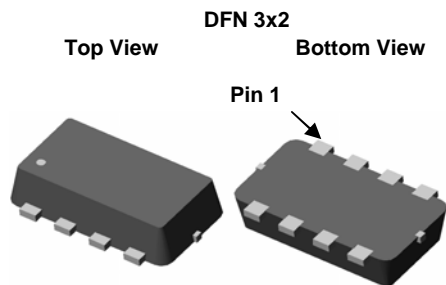
#### General Description

The AON4805L uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltage as low as 1.8V. This device is suitable for use as a load switch or in PWM applications.

-RoHS Compliant  
 -Halogen Free

#### Features

$V_{DS}$  (V) = -20V  
 $I_D$  = -4.5A ( $V_{GS}$  = -4.5V)  
 $R_{DS(ON)} < 65m\Omega$  ( $V_{GS}$  = -4.5V)  
 $R_{DS(ON)} < 85m\Omega$  ( $V_{GS}$  = -2.5V)  
 $R_{DS(ON)} < 115m\Omega$  ( $V_{GS}$  = -1.8V)



#### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	MOSFET	Units
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Continuous Drain Current	$T_A=25^\circ\text{C}$	-4.5	A
	$T_A=70^\circ\text{C}$	-3.5	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-25	
Power Dissipation <sup>B</sup>	$T_A=25^\circ\text{C}$	2	W
	$T_A=70^\circ\text{C}$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

#### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	50	60	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>AD</sup>		84	100	$^\circ\text{C/W}$
Maximum Junction-to-Lead	$R_{\theta JL}$	28	34	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±8V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.5	-0.67	-1	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-5V	-25			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4.5A T <sub>J</sub> =125°C		53 72	65 90	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-3A		66	85	mΩ
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-2A		88	115	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-4.5A		15		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.7	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-1.7	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-10V, f=1MHz		560	670	pF
C <sub>OSS</sub>	Output Capacitance		80		pF	
C <sub>ISS</sub>	Reverse Transfer Capacitance		70		pF	
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		15	23	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-4.5A		8.5	10	nC
Q <sub>gs</sub>	Gate Source Charge		1.2		nC	
Q <sub>gd</sub>	Gate Drain Charge		2.1		nC	
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, R <sub>L</sub> =2.2Ω, R <sub>GEN</sub> =6Ω		7.2		ns
t <sub>r</sub>	Turn-On Rise Time		36		ns	
t <sub>D(off)</sub>	Turn-Off DelayTime		53		ns	
t <sub>f</sub>	Turn-Off Fall Time		56		ns	
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-4.5A, dI/dt=100A/μs		37	45	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-4.5A, dI/dt=100A/μs		27		nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The value in any given application depends on the user's specific board design.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C: Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

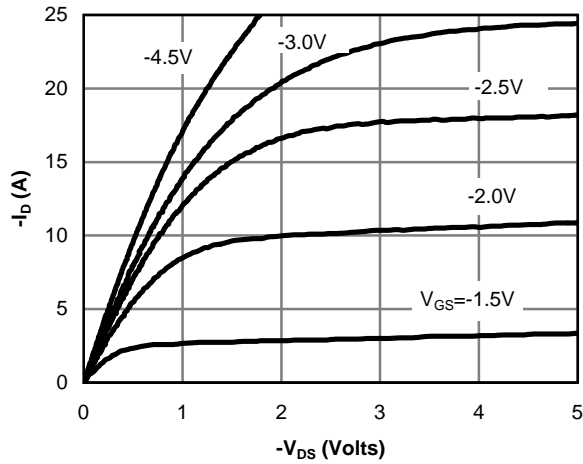
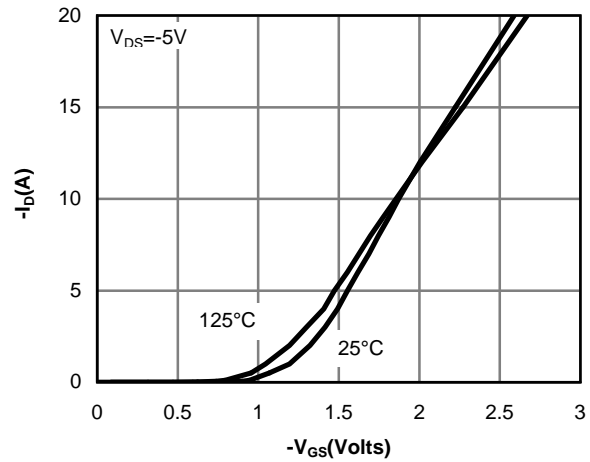
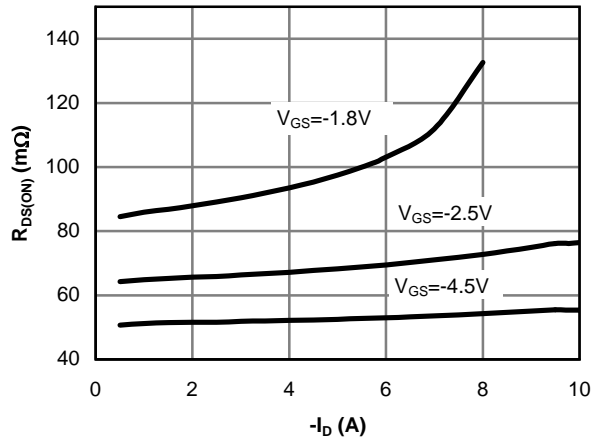
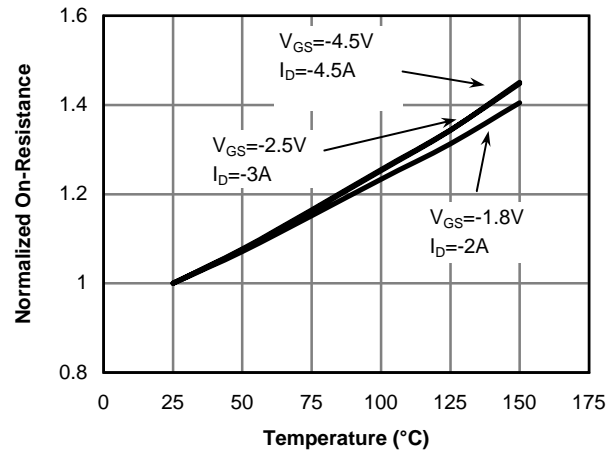
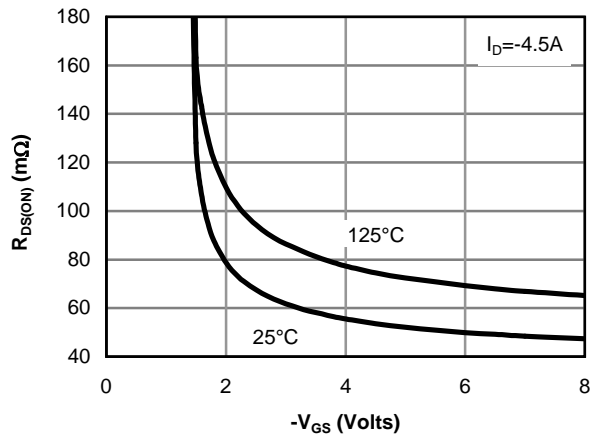
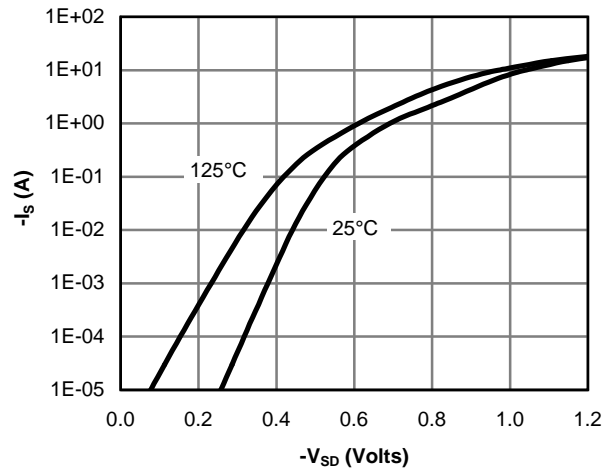
D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to lead R<sub>θJL</sub> and lead to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 1: On-Region Characteristics(Note E)**

**Figure 2: Transfer Characteristics(Note E)**

**Figure 3: On-Resistance vs. Drain Current and Gate Voltage(Note E)**

**Figure 4: On-Resistance vs. Junction Temperature(Note E)**

**Figure 5: On-Resistance vs. Gate-Source Voltage(Note E)**

**Figure 6: Body-Diode Characteristics(Note E)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

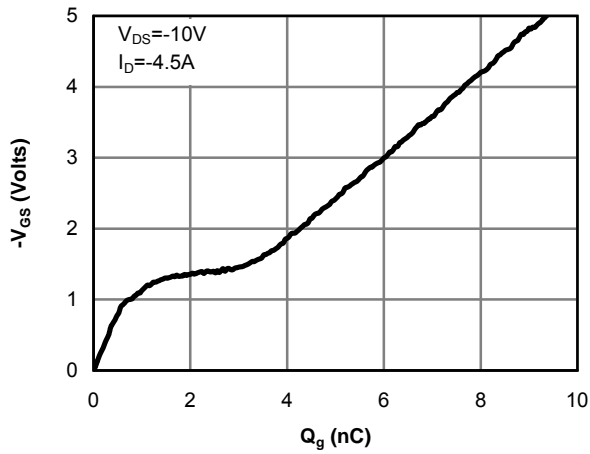


Figure 7: Gate-Charge Characteristics

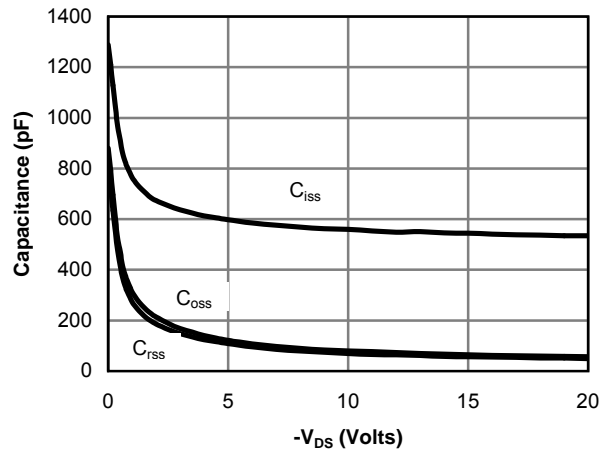


Figure 8: Capacitance Characteristics

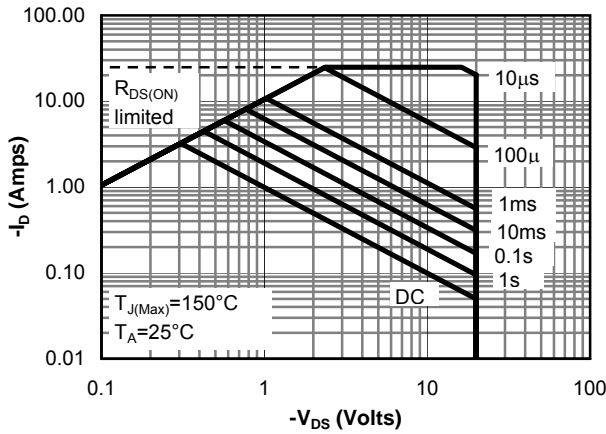


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

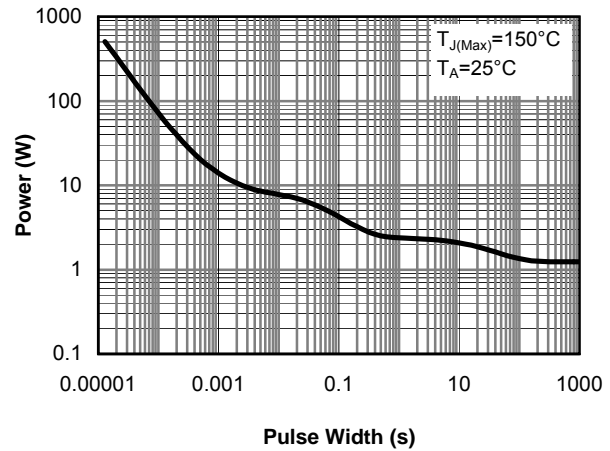


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

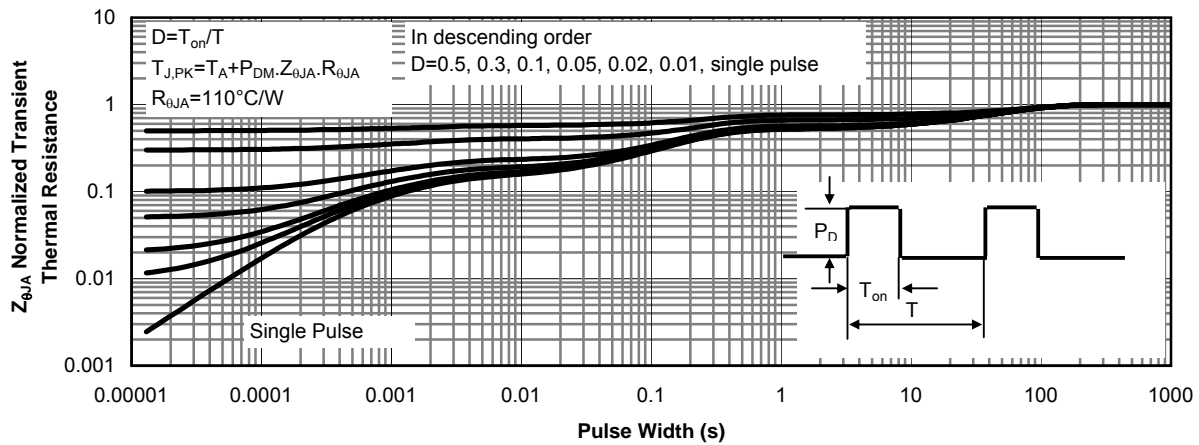
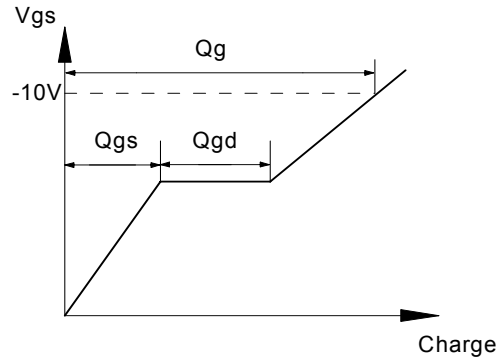
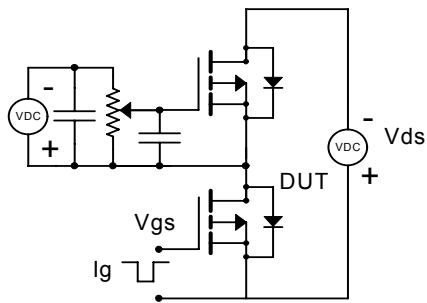
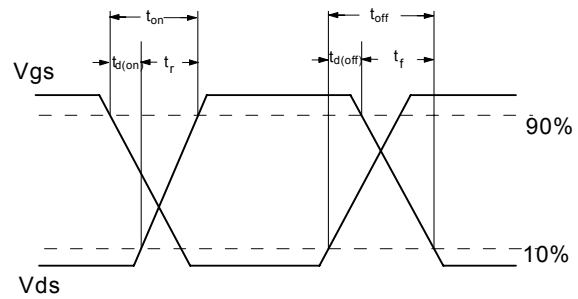
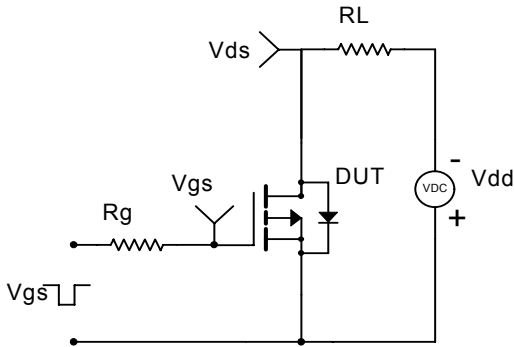


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

