

General Description

- Trench Power MOSFET - AlphaSGT2™ technology 80V
- Low $R_{DS(ON)}$
- Excellent $Q_g \times R_{DS(ON)}$ Product (FOM)
- Pb-Free lead Plating, RoHS 2.0 and Halogen-Free Compliant
- Spike Optimized Process

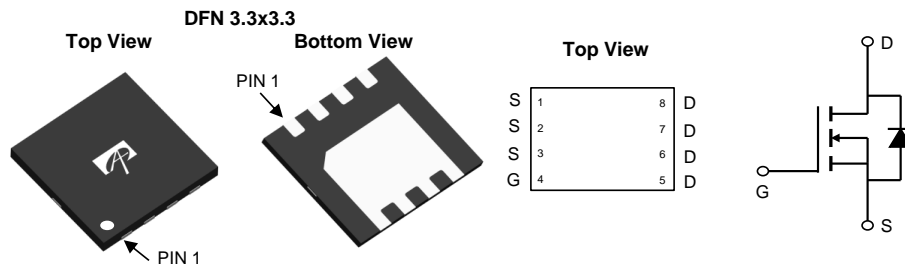
Applications

- Full Bridge MOSFET for isolated DC/DC converter
- DC/DC converters

Product Summary

V_{DS}	80V
I_D (at $V_{GS}=10V$)	50A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 7.2mΩ
$R_{DS(ON)}$ (at $V_{GS}=8V$)	< 8.8mΩ

100% UIS Tested
 100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONR66820	DFN 3.3x3.3	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	150	
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	A
		$T_A=70^\circ\text{C}$	
Avalanche Current ^C	I_{AS}	35	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}	61	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	W
		$T_A=70^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	25	30	°C/W
Maximum Junction-to-Ambient ^{A,D}				
Maximum Junction-to-Case	$R_{\theta JC}$	1.0	1.2	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	80			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2.9	3.5	4.1	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =17A T _J =125°C		6 10.2	7.2 12.2	mΩ
		V _{GS} =8V, I _D =17A		7	8.8	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =17A		47		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.72	1	V
I _S	Maximum Body-Diode Continuous Current ^G				50	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =40V, f=1MHz		1950		pF
C _{oss}	Output Capacitance			470		pF
C _{riss}	Reverse Transfer Capacitance			11		pF
R _g	Gate resistance	f=1MHz	0.3	0.6	0.9	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =40V, I _D =17A		25	50	nC
Q _{gs}	Gate Source Charge			9		nC
Q _{gd}	Gate Drain Charge			4.2		nC
Q _{oss}	Output Charge	V _{GS} =0V, V _{DS} =40V		36		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =50V, R _L =2.78Ω, R _{GEN} =3Ω		10		ns
t _r	Turn-On Rise Time			4		ns
t _{D(off)}	Turn-Off DelayTime			21		ns
t _f	Turn-Off Fall Time			4		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =17A, di/dt=500A/μs		28		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =17A, di/dt=500A/μs		140		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

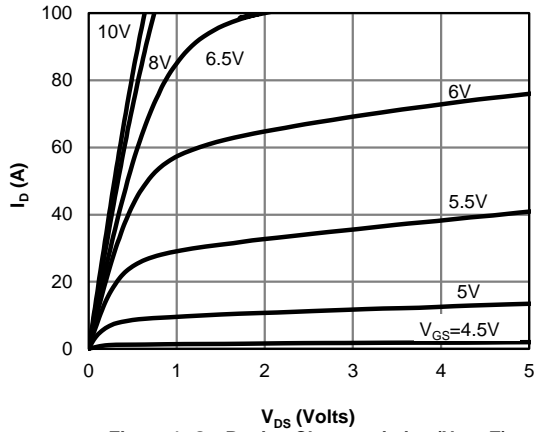


Figure 1: On-Region Characteristics (Note E)

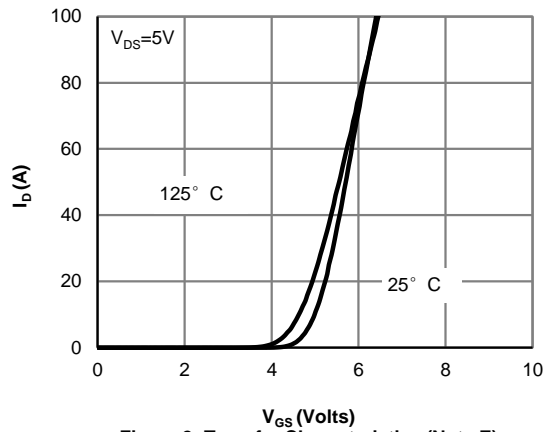


Figure 2: Transfer Characteristics (Note E)

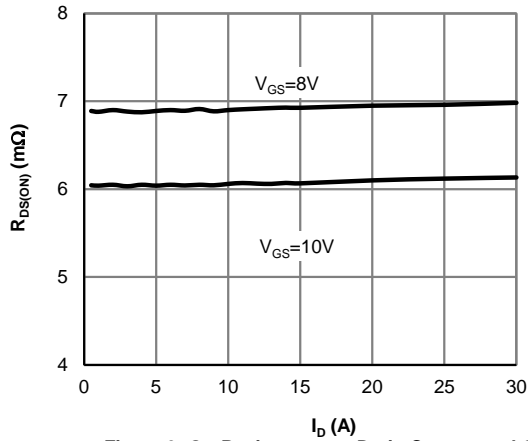


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

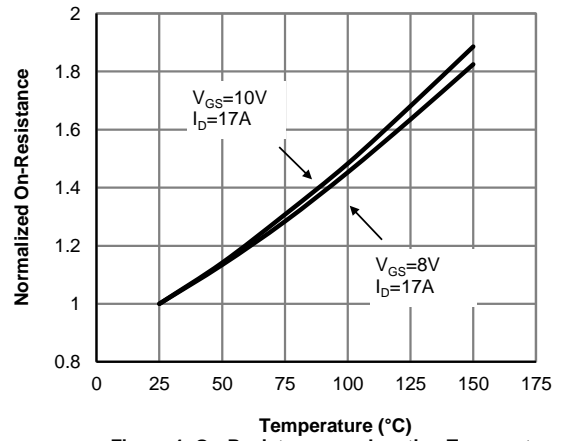


Figure 4: On-Resistance vs. Junction Temperature (Note E)

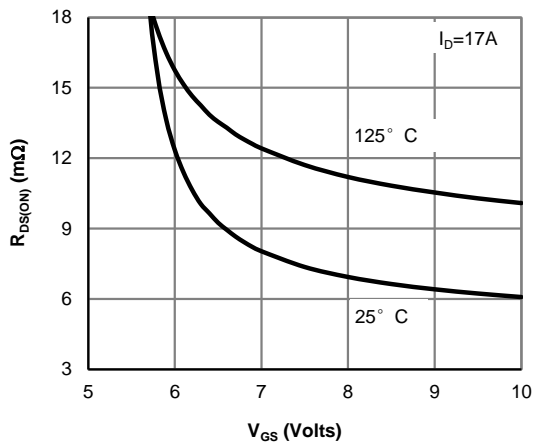


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

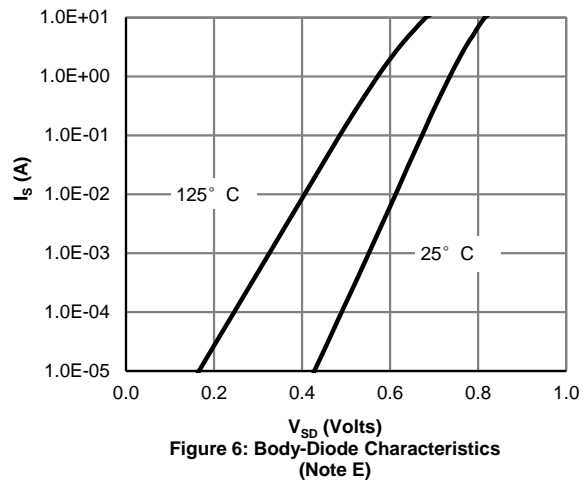


Figure 6: Body-Diode Characteristics (Note E)

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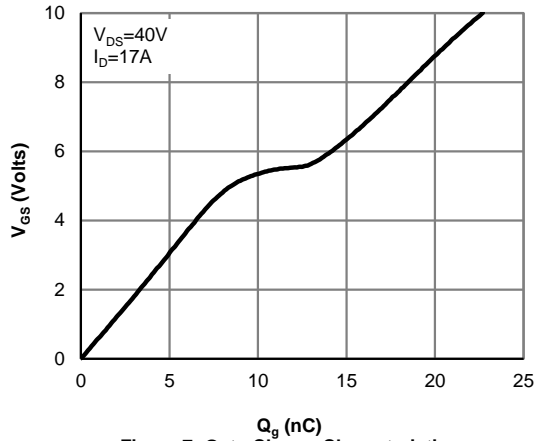


Figure 7: Gate-Charge Characteristics

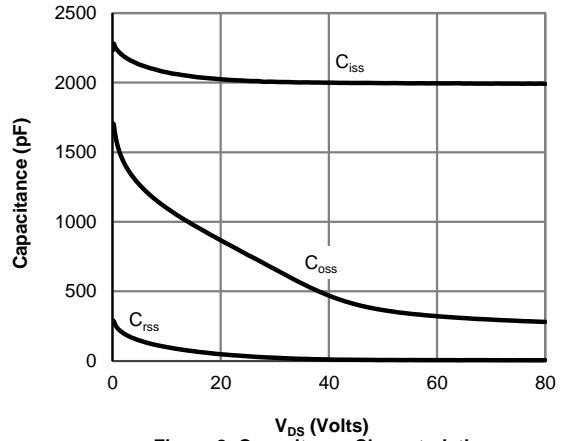


Figure 8: Capacitance Characteristics

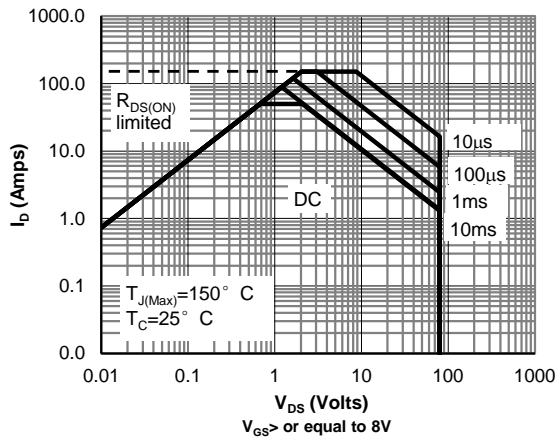


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

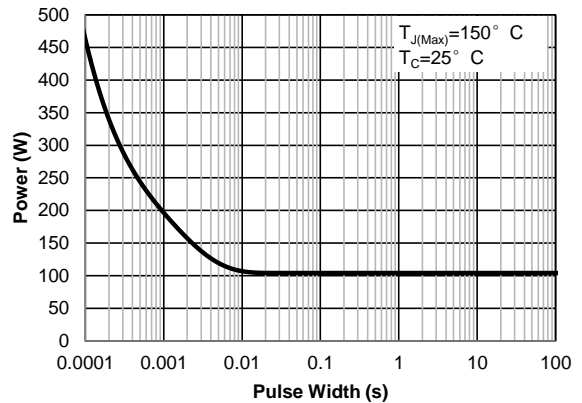


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

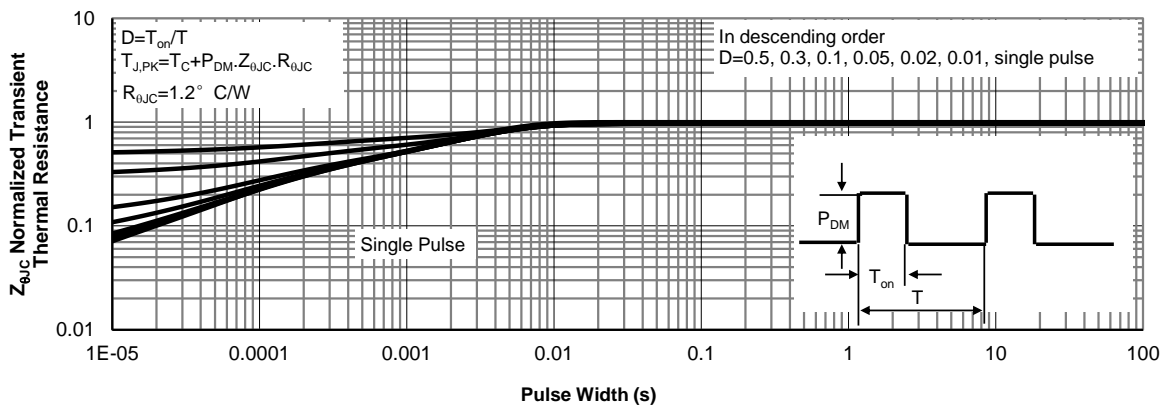


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

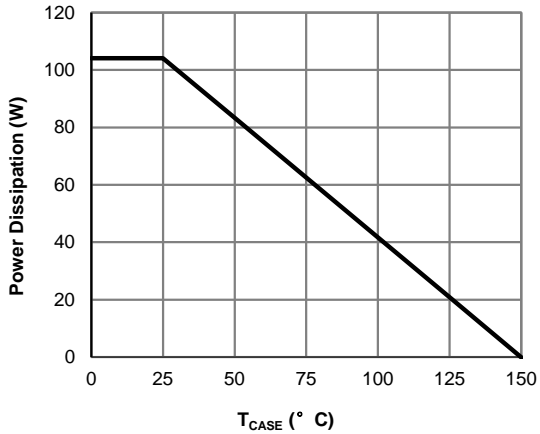


Figure 12: Power De-rating (Note F)

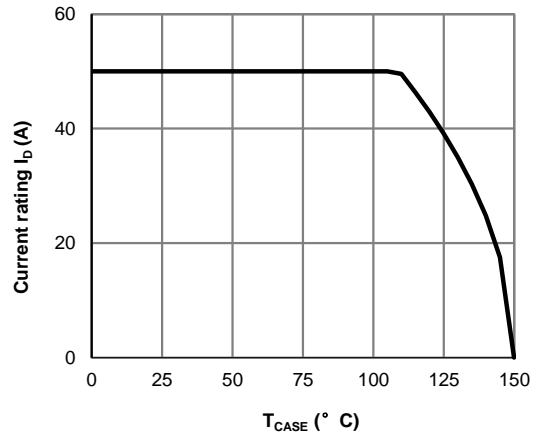


Figure 13: Current De-rating (Note F)

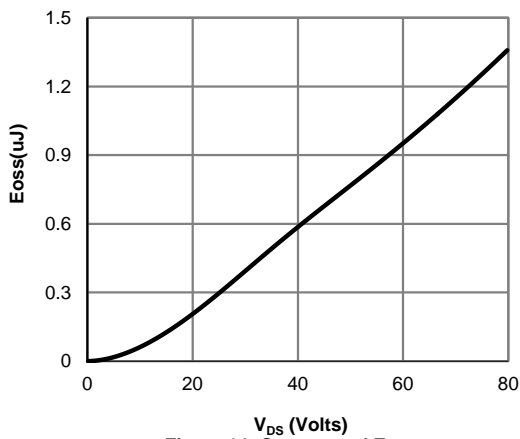


Figure 14: Coss stored Energy

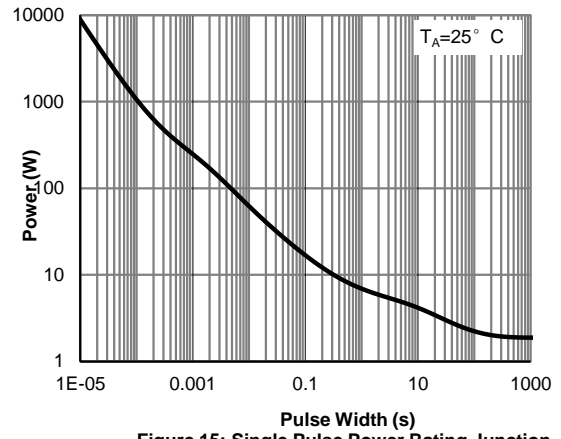


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

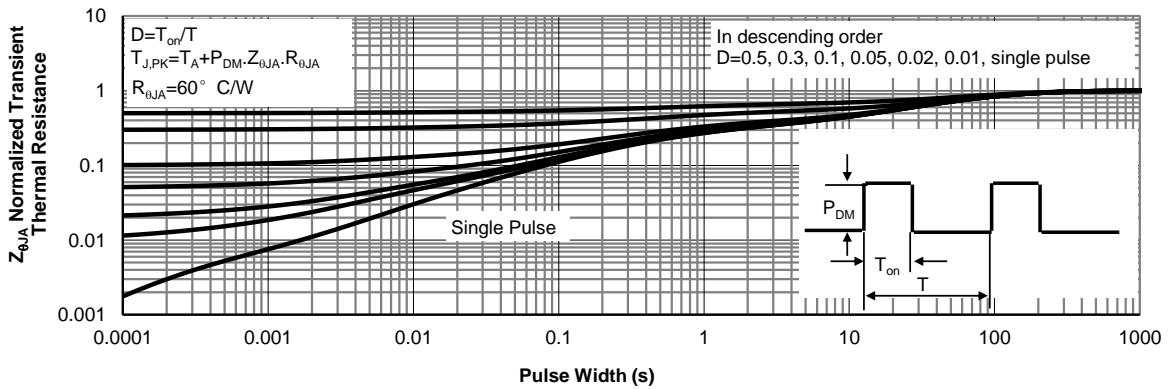


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

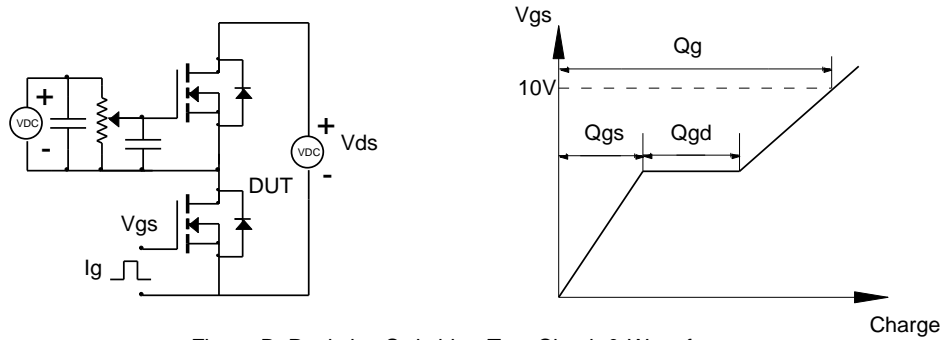


Figure B: Resistive Switching Test Circuit & Waveforms

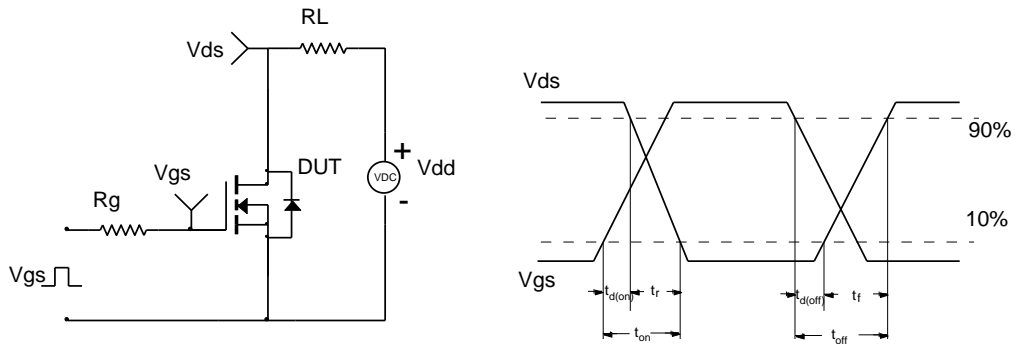


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

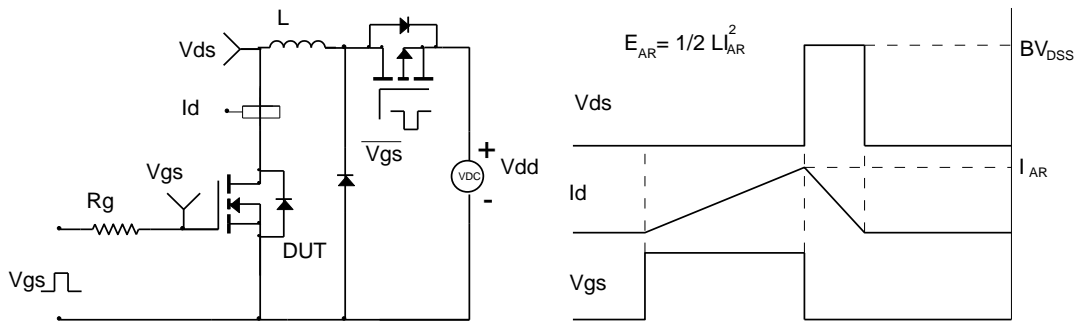


Figure D: Diode Recovery Test Circuit & Waveforms

