ALPHA & OMEGA SEMICONDUCTOR

AONV125A60
600V, α MOS5 ^{TM} N-Channel Power Transistor

General Description

- Proprietary αMOS5^{TM} technology
- Low $R_{DS(ON)}$
- Optimized switching parameters for better EMI performance
- Enhanced body diode for robustness and fast reverse recovery

Product Summary

V_{DS} @ $T_{j,max}$	700V
I_{DM}	100A
$R_{DS(ON),max}$	< 0.125Ω
$Q_{g,typ}$	44nC
E_{oss} @ 400V	6.3μJ

100% UIS Tested
100% R_g Tested

Applications

- PFC and PWM stages (LLC, FSFB,TTF) of Server, Telecom, Industrial, UPS, and Solar Inverters

Green Product

DFN8X8
Top View — Pin1:G
Bottom View — Pin2: Driver Source
AONV125A60
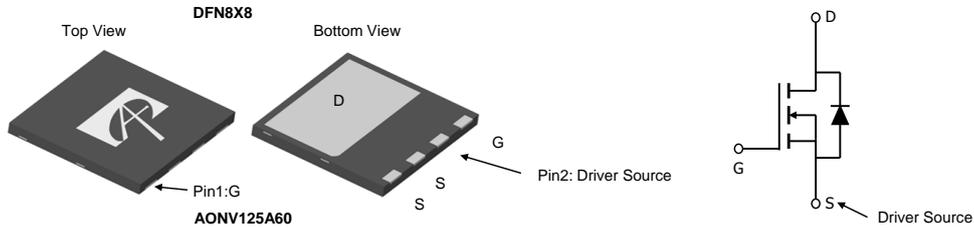
Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONV125A60	DFN8x8_4L_EP1_S	Tape & Reel	3500

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±20	V
Gate-Source Voltage (dynamic) AC(f>1Hz)		V_{GS}	±30	V
Continuous Drain Current	T_C=25°C	I_D	28	A
	T_C=100°C		18	
Pulsed Drain Current [C]		I_{DM}	100	
Continuous Drain Current	T_A=25°C	I_{DSM}	4.9	A
	T_A=70°C		3.9	
Avalanche Current [C] L=1mH		I_{AR}	14	A
Repetitive avalanche energy [C]		E_{AR}	98	mJ
Single pulsed avalanche energy [G]		E_{AS}	555	mJ
MOSFET dv/dt ruggedness		dv/dt	100	V/ns
Diode reverse recovery V_{DS}=0 to 400V,I_F<=14A,Tj=25°C		dv/dt	20	V/ns
		di/dt	300	A/us
Power Dissipation [B]	T_C=25°C	P_D	312	W
	Derate above 25°C		2.5	W/°C
Power Dissipation [A]	T_A=25°C	P_{DSM}	8.3	W
	T_A=70°C		5.3	W/°C
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds		T_L	300	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	12	15	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	50	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	0.24	0.4	°C/W

Electrical Characteristics (T$_J$=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV$_{DSS}$	Drain-Source Breakdown Voltage	I$_D$=250µA, V$_{GS}$=0V, T$_J$=25°C	600			V
		I$_D$=250uA, V$_{GS}$=0V, T$_J$=150°C		700		
BV$_{DSS}$/ΔTJ	Breakdown Voltage Temperature Coefficient	I$_D$=250µA, V$_{GS}$=0V		0.51		V/°C
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$=600V, V$_{GS}$=0V			1	µA
		V$_{DS}$=480V, T$_J$=125°C			10	
I$_{GSS}$	Gate-Body leakage current	V$_{DS}$=0V, V$_{GS}$=±20V			±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$=5V, I$_D$=250µA	3.3	3.9	4.5	V
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$=10V, I$_D$=14A		0.111	0.125	Ω
g$_{FS}$	Forward Transconductance	V$_{DS}$=10V, I$_D$=14A		22		S
V$_{SD}$	Diode Forward Voltage	I$_S$=14A, V$_{GS}$=0V		0.86	1.2	V
I$_S$	Maximum Body-Diode Continuous Current				28	A
I$_{SM}$	Maximum Body-Diode Pulsed Current [C]				100	A
DYNAMIC PARAMETERS						
C$_{iss}$	Input Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz		2995		pF
C$_{oss}$	Output Capacitance			85		pF
C$_{o(er)}$	Effective output capacitance, energy related [H]	V$_{GS}$=0V, V$_{DS}$=0 to 480V, f=1MHz		73		pF
C$_{o(tr)}$	Effective output capacitance, time related [I]			305		pF
C$_{rss}$	Reverse Transfer Capacitance	V$_{GS}$=0V, V$_{DS}$=100V, f=1MHz		0.8		pF
R$_g$	Gate resistance	f=1MHz		2.3		Ω
SWITCHING PARAMETERS						
Q$_g$	Total Gate Charge	V$_{GS}$=10V, V$_{DS}$=480V, I$_D$=14A		44		nC
Q$_{gs}$	Gate Source Charge			21		nC
Q$_{gd}$	Gate Drain Charge			9		nC
t$_{D(on)}$	Turn-On DelayTime	V$_{GS}$=10V, V$_{DS}$=400V, I$_D$=14A, R$_G$=5Ω		39		ns
t$_r$	Turn-On Rise Time			34		ns
t$_{D(off)}$	Turn-Off DelayTime			56		ns
t$_f$	Turn-Off Fall Time			19		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I$_F$=14A, dI/dt=100A/µs, V$_{DS}$=400V		375		ns
I$_{rm}$	Peak Reverse Recovery Current			34		A
Q$_{rr}$	Body Diode Reverse Recovery Charge			8		µC

A. The value of R$_{θJA}$ is measured with the device in a still air environment with T$_A$=25°C.

B. The power dissipation P$_D$ is based on T$_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T$_{J(MAX)}$=150°C, Ratings are based on low frequency and duty cycles to keep initial T$_J$ =25°C.

D. The R$_{θJA}$ is the sum of the thermal impedance from junction to case R$_{θJC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsin k, assuming a maximum junction temperature of T$_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I$_{AS}$=4.3A, R$_G$=25Ω, Starting T$_J$=25°C.

H. C$_{o(er)}$ is a fixed capacitance that gives the same stored energy as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.

I. C$_{o(tr)}$ is a fixed capacitance that gives the same charging time as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{(BR)DSS}$.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics
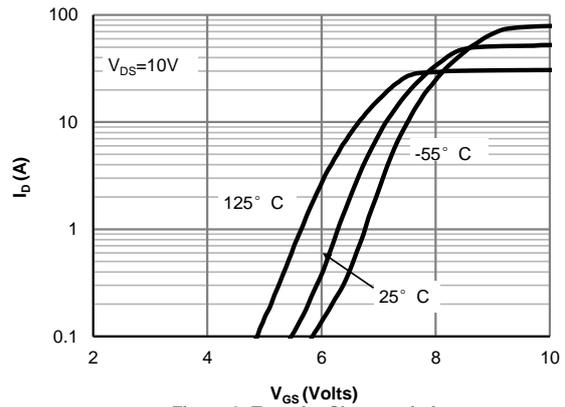
Figure 2: Transfer Characteristics
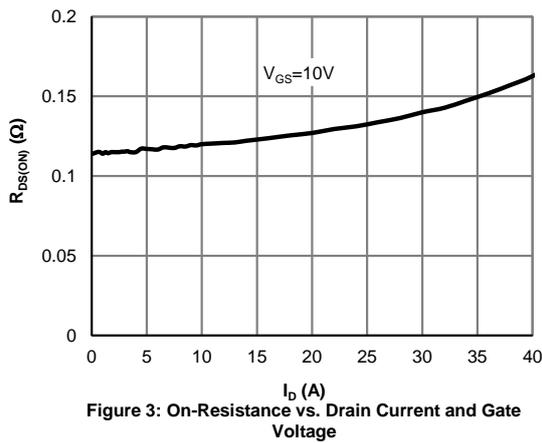
Figure 3: On-Resistance vs. Drain Current and Gate Voltage
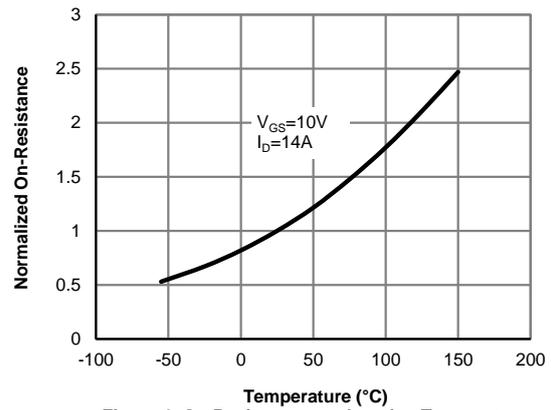

Figure 4: On-Resistance vs. Junction Temperature
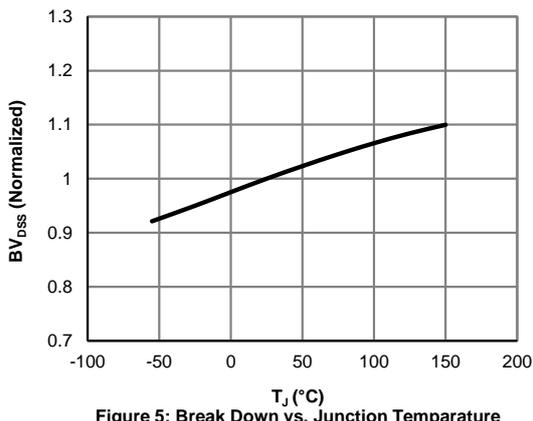

Figure 5: Break Down vs. Junction Temparature
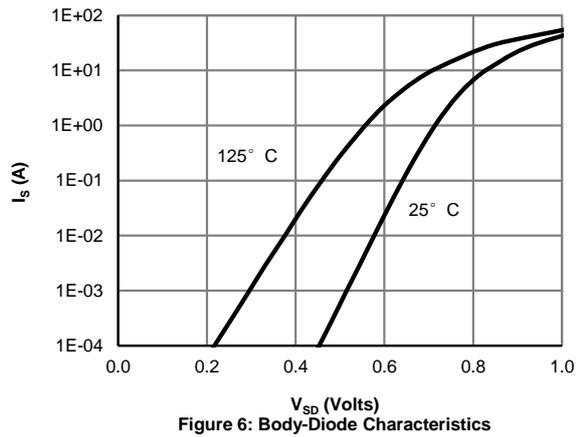
Figure 6: Body-Diode Characteristics

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
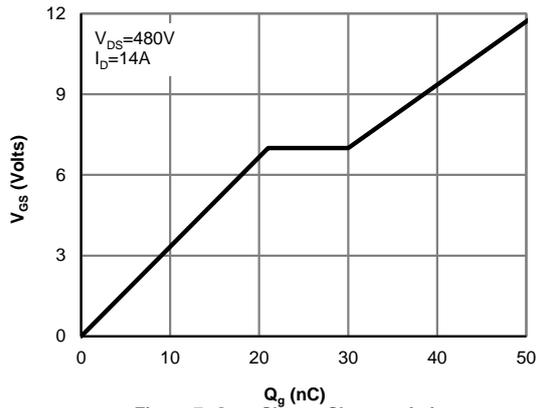
V_{DS}=480V
I_D=14A
V_{GS} (Volts)
Q_g (nC)
Figure 7: Gate-Charge Characteristics
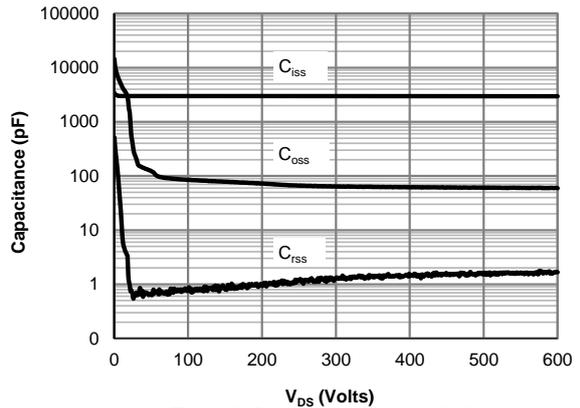
Capacitance (pF)
C_{iss}
C_{oss}
C_{rss}
V_{DS} (Volts)
Figure 8: Capacitance Characteristics
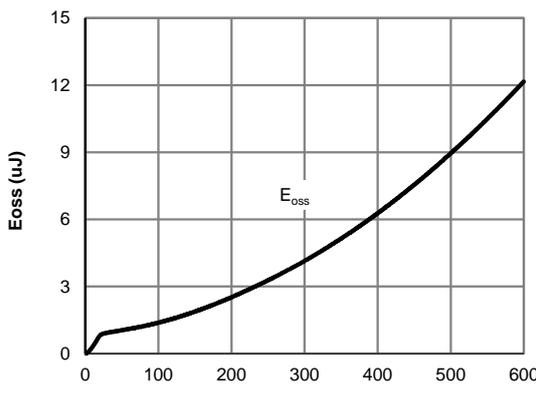
Eoss (uJ)
E_{oss}
V_{DS} (Volts)
Figure 9: Coss stored Energy
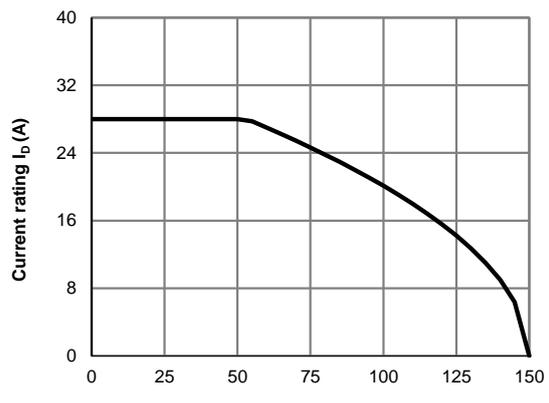
Current rating I_D (A)
T_{CASE} (°C)
Figure 10: Current De-rating (Note F)
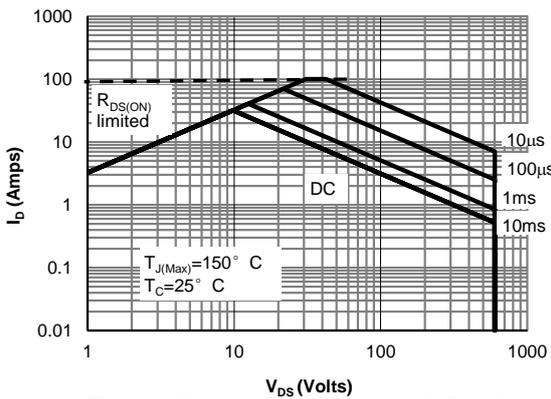
I_D (Amps)
$R_{DS(ON)}$ limited
DC
10µs
100µs
1ms
10ms
$T_{J(Max)}$=150°C
T_C=25°C
V_{DS} (Volts)
Figure 11: Maximum Forward Biased Safe Operating Area (Note F)
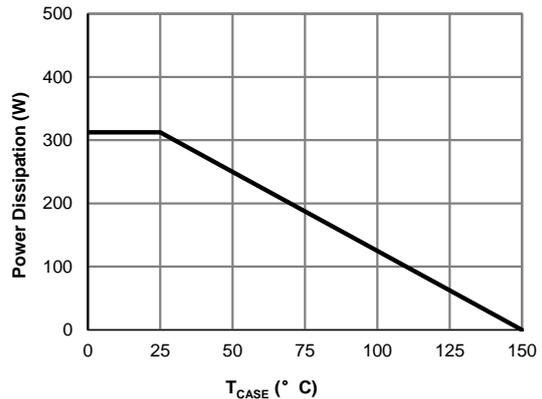
Power Dissipation (W)
T_{CASE} (°C)
Figure 12: Power De-rating (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

$D = T_{on}/T$
$T_{J,PK} = T_C + P_{DM} \cdot Z_{\theta JC} \cdot R_{\theta JC}$
$R_{\theta JC} = 0.4^\circ$ C/W

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse

P_{DM}

T_{on}

T
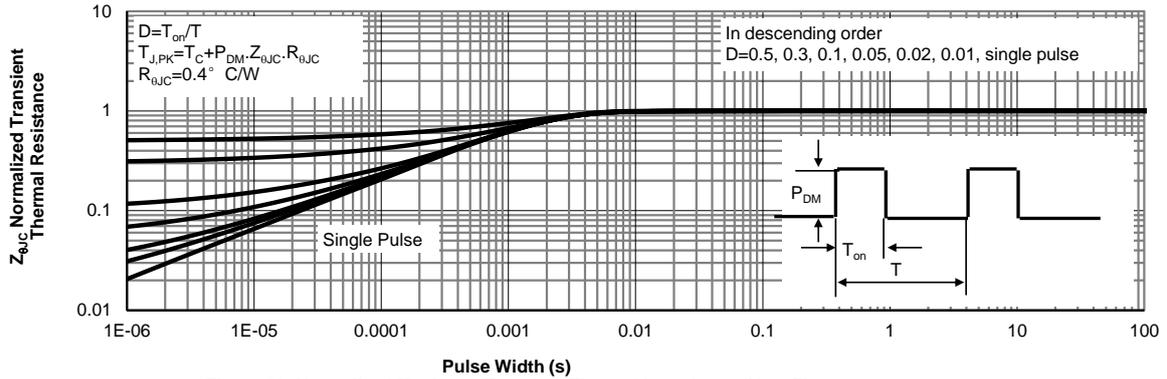
Figure 13: Normalized Maximum Transient Thermal Impedance (Note F)

$T_{J(Max)} = 150^\circ$ C
$T_C = 25^\circ$ C
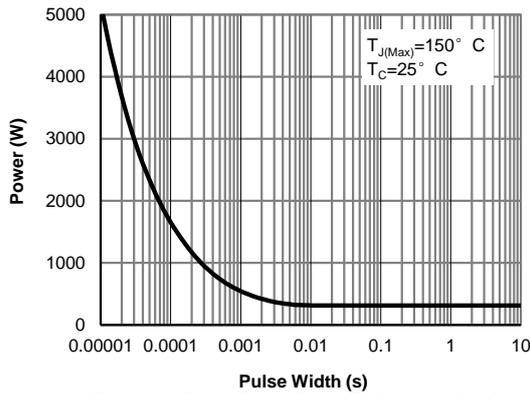
Figure 14: Single Pulse Power Rating Junction-to-Case (Note F)

$T_{J(Max)} = 150^\circ$ C
$T_A = 25^\circ$ C
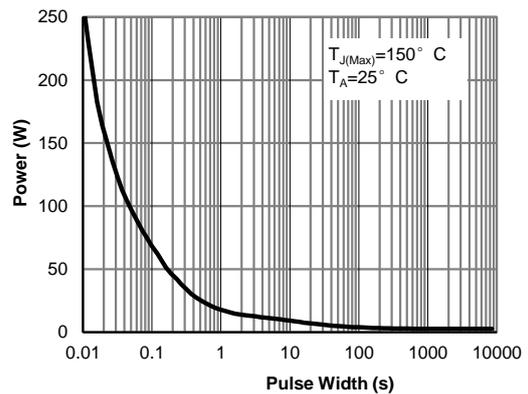
Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

$D = T_{on}/T$
$T_{J,PK} = T_A + P_{DM} \cdot Z_{\theta JA} \cdot R_{\theta JA}$
$R_{\theta JA} = 50^\circ$ C/W

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

P_{DM}

T_{on}

T

Single Pulse
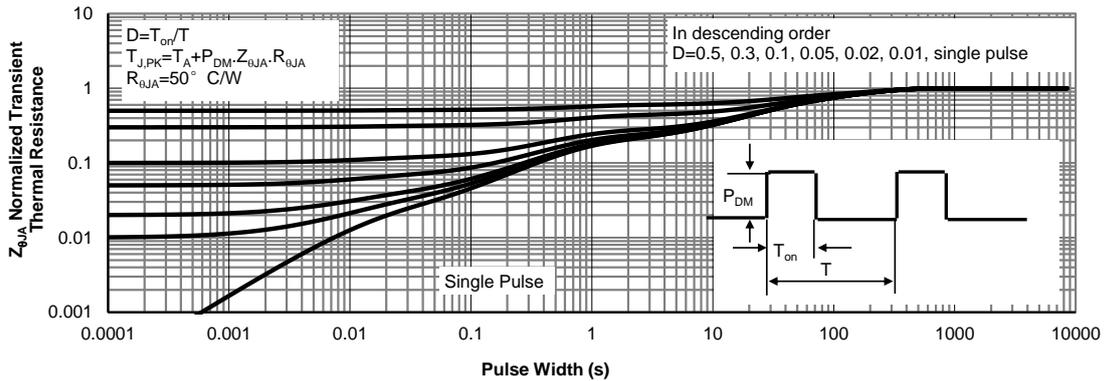
**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

Gate Charge Test Circuit & Waveform
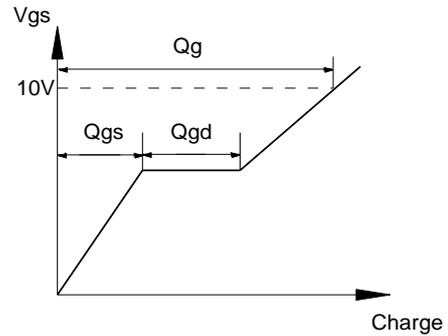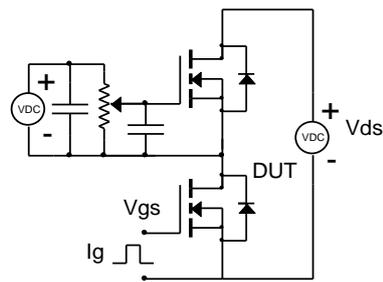
Resistive Switching Test Circuit & Waveforms
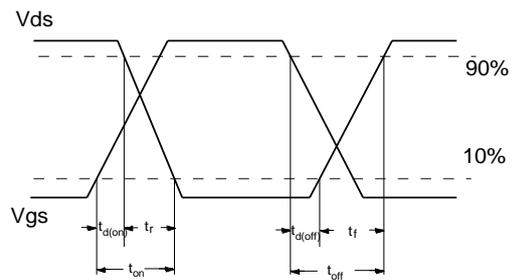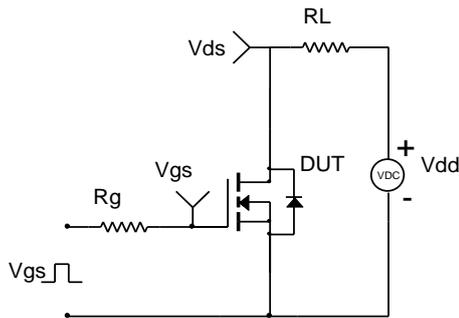
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2 \, L I_{AR}^2$$
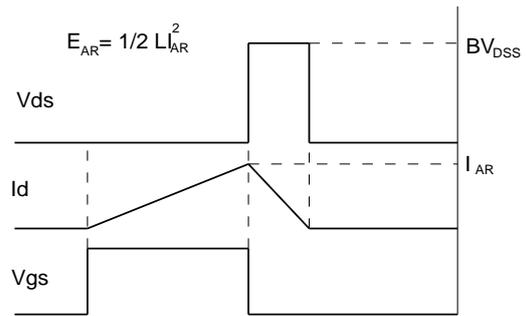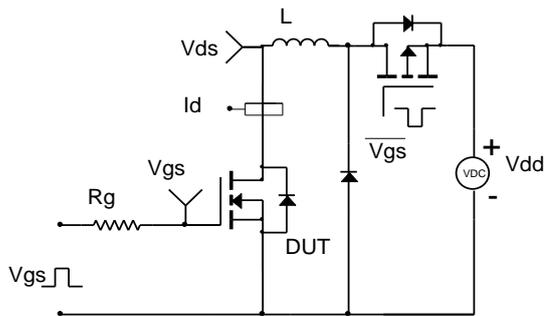
Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = -\int I \, dt$$