

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
STATIC PARAMETERS							
BV _{DSS}	Drain-Source Breakdown Voltage	I _D $\$$ V _{GS} =0V, T _J =25°C	600			V	
		I _D $\$$ V _{GS} =0V, T _J =150°C		700			
BV _{DSS}	Breakdown Voltage Temperature Coefficient	I _D $\$$ V _{GS} =0V		0.49		V/°C	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V			1	μA	
		V _{DS} =480V, T _J =125°C			10		
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	3.4	4	4.6	V	
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =7.6A		0.19	0.21		
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =10A		16		S	
V _{SD}	Diode Forward Voltage	I _S =7.6A, V _{GS} =0V		0.88	1.2	V	
I _S	Maximum Body-Diode Continuous Current				20	A	
I _{SM}	Maximum Body-Diode Pulsed Current ^C				80	A	
DYNAMIC PARAMETERS							
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		1935		pF	
C _{oss}	Output Capacitance				55		pF
C _{o(er)}	Effective output capacitance, energy related ^I	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz		49		pF	
C _{o(tr)}	Effective output capacitance, time related ^J				213		pF
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz		1.25		pF	
R _g	Gate resistance	f=1MHz		5			
SWITCHING PARAMETERS							
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =10A		34		nC	
Q _{gs}	Gate Source Charge				15		nC
Q _{gd}	Gate Drain Charge				8.5		nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =400V, I _D =10A, R _G =25Ω		80		ns	
t _r	Turn-On Rise Time				70		ns
t _{D(off)}	Turn-Off Delay Time				80		ns
t _f	Turn-Off Fall Time				20		ns
t _{rr}	Body Diode Reverse Recovery Time				341		ns
I _{rm}	Peak Reverse Recovery Current	I _F =10A, di/dt=100A/μs, V _{DS} =400V		28		A	
Q _{rr}	Body Diode Reverse Recovery Charge			6.8		μC	

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25° C.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. This is the absolute maximum rating. Parts are 100% tested at T_J=25° C, L=60mH, I_{AS}=2.7A, V_{DD}=150V, R_G=25 .

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C

I. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

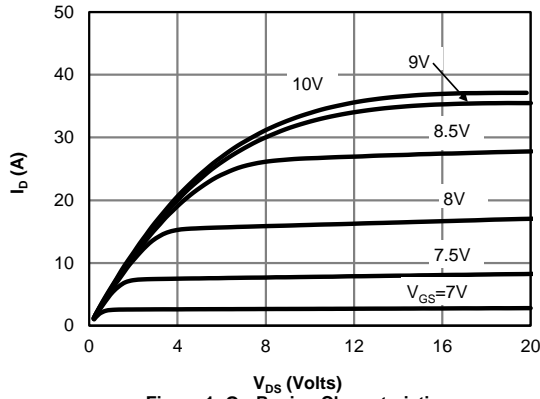


Figure 1: On-Region Characteristics

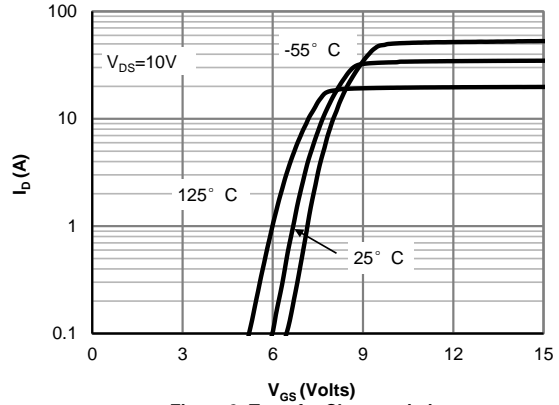


Figure 2: Transfer Characteristics

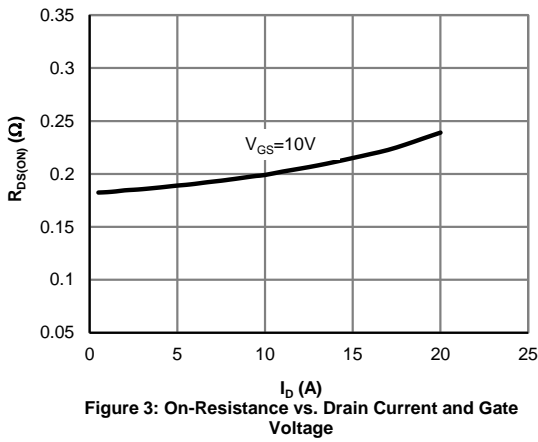


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

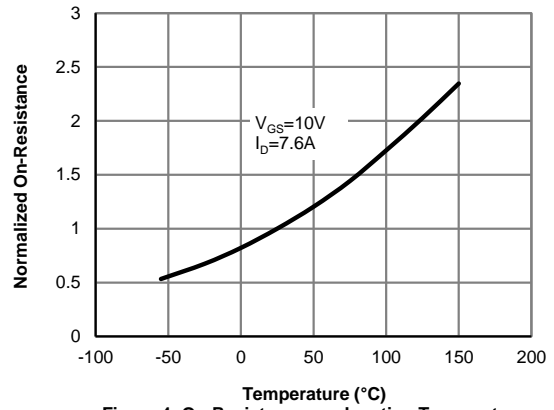


Figure 4: On-Resistance vs. Junction Temperature

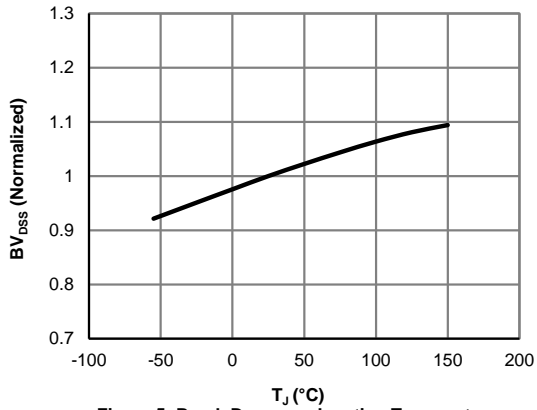


Figure 5: Break Down vs. Junction Temperature

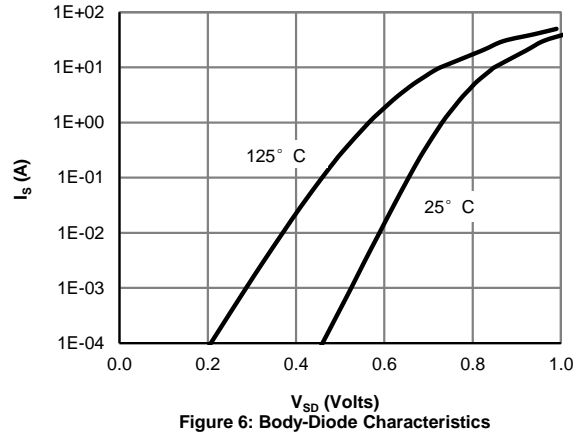


Figure 6: Body-Diode Characteristics

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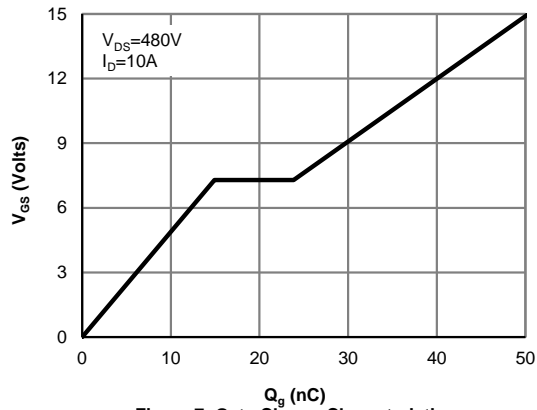


Figure 7: Gate-Charge Characteristics

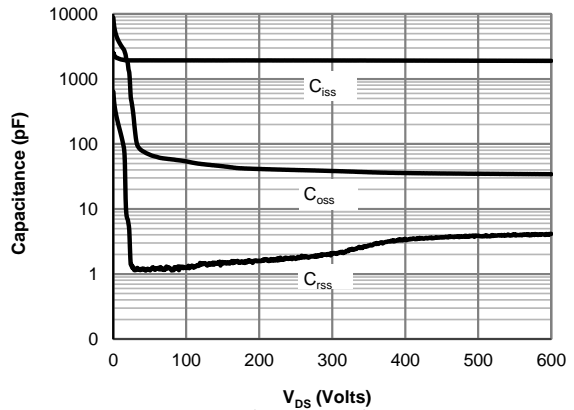


Figure 8: Capacitance Characteristics

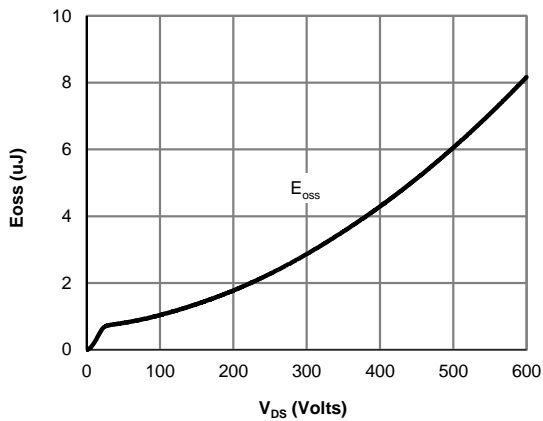


Figure 9: Coss stored Energy

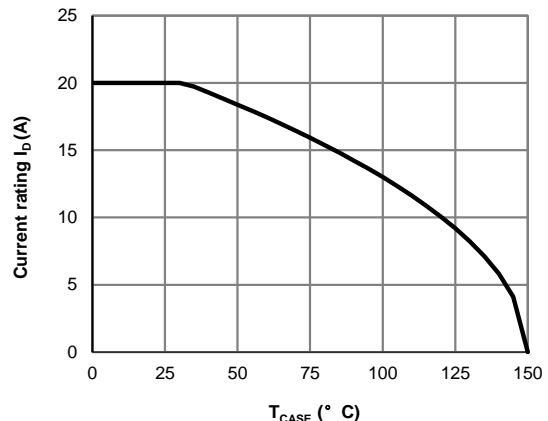


Figure 10: Current De-rating (Note F)

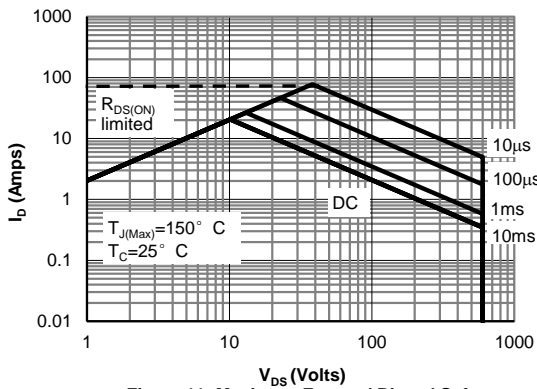


Figure 11: Maximum Forward Biased Safe Operating Area (Note F)

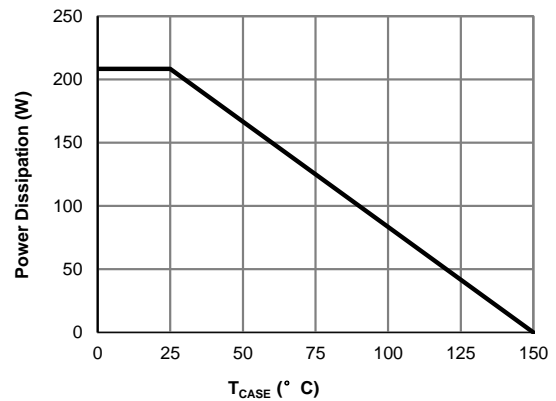
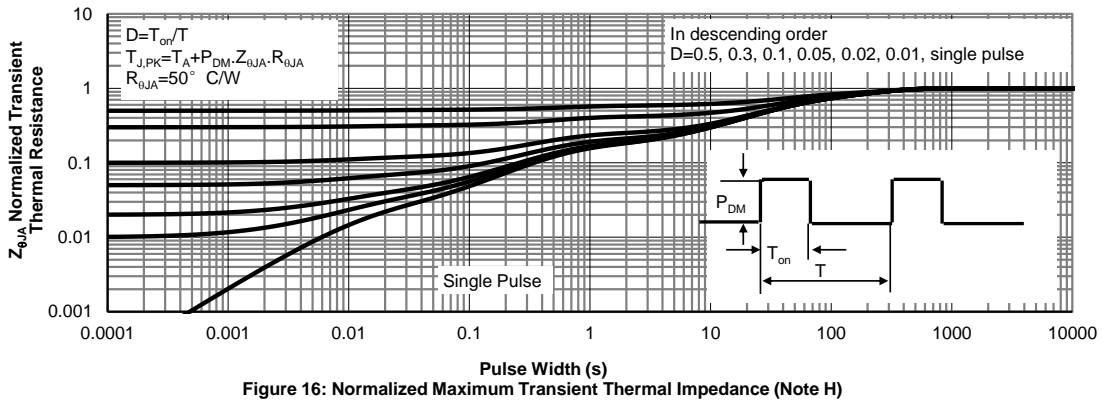
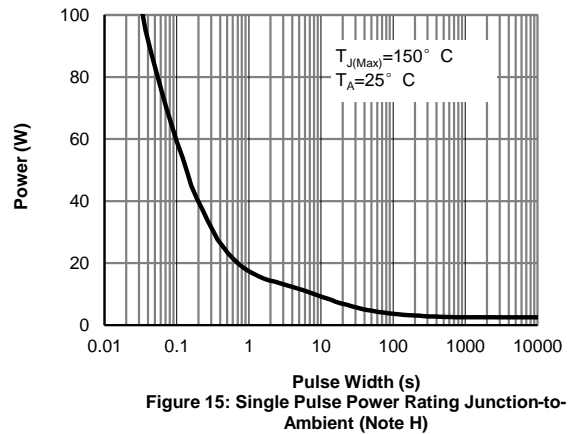
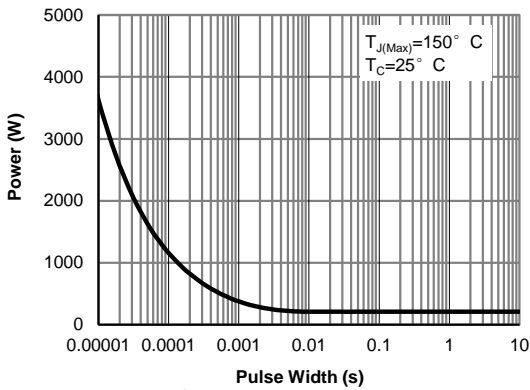
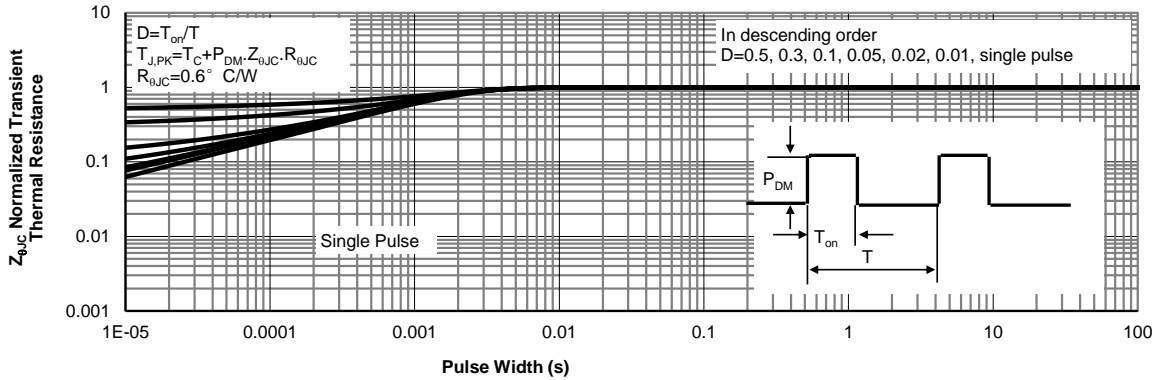
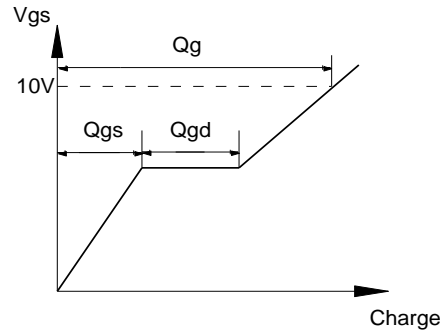
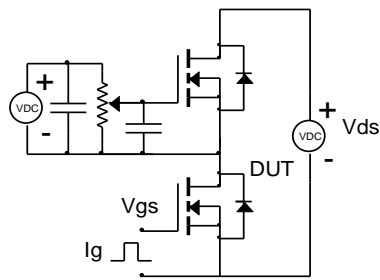


Figure 12: Power De-rating (Note F)

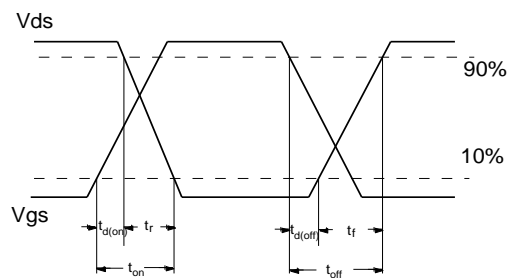
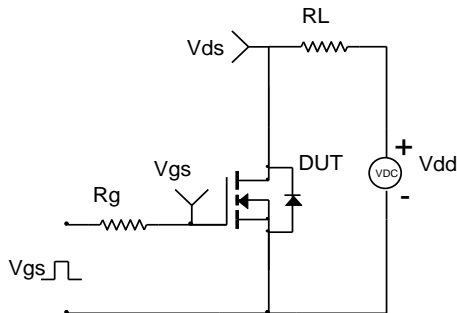
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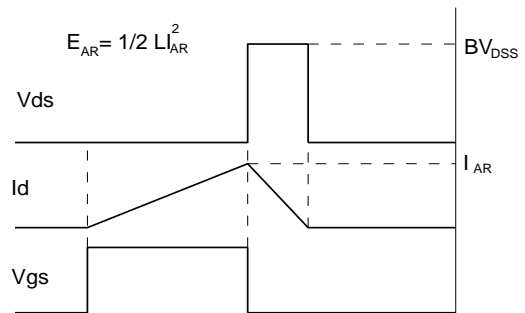
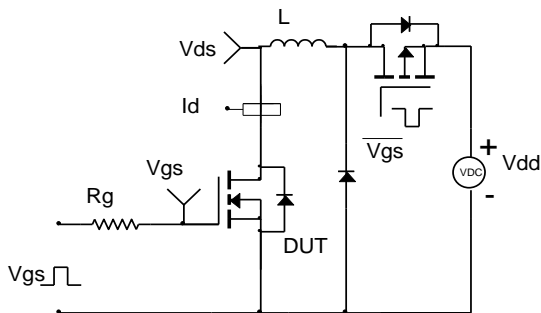
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

