

AOZ13287DI-01

wer™ 20V, 9mΩ Ideal Diode Smart Protection ith Integrated TVS Diode for Surge Protection

General Description

The AOZ13287DI-01 is a protection switch intended for applications that require reverse current protection. The input operating voltage range is between 3.4V and 22V, and both VIN and VOUT terminals are rated at 28V Absolute Maximum. The power switch is capable of 13A continuous current and 22.5A surge current for 10ms. AOZ13287DI-01 provides under-voltage lockout, over-voltage, and over-temperature protection. The FLTB pin flags thermal shutdown, over-voltage, and soft-start short circuit faults. AOZ13287DI-01 also integrated TVS diode for surge protection.

AOZ13287DI-01 is the ideal solution for multi-port Type-C PD current sinking application. The Ideal Diode True Reverse Current Blocking (IDTRCB) feature prevents VIN to rise due to reverse current flow from VOUT under all conditions.

An internal soft-start circuit controls inrush current due to highly capacitive loads and the slew rate can be adjusted using an external capacitor. The integrated back-to-back MOSFET offer industry's lowest ON resistance and highest SOA to safely handle high current and a wide range of output capacitances on VOUT.

The AOZ13287DI-01 is available in a thermally enhanced DFN 3.2mm x 5.5mm 17L package which can operate over -40°C to +125°C junction temperature range.

Features

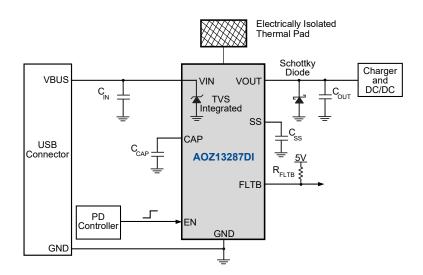
- 13A continuous sink current
- 22.5A peak current for 10ms @ 2% duty cycle
- 9mΩ typical ON resistance
- 3.4V to 22V operating input voltage
- VIN and VOUT are rated 28V Abs max
- Ideal Diode True Reverse Current Blocking (IDTRCB)
- Programmable Soft-Start
- VIN Under-Voltage Lockout (UVLO)
- VIN Over-Voltage Lockout (OVLO)
- Thermal Shutdown Protection
- Short Circuit Protection
- Integrated TVS diode for surge protection
- IEC61000-4-2: ±30kV contact discharge, ±30kV air discharge on VIN
- IEC61000-4-5: 30 A (8/20 μs), 33.5V Clamp Voltage, no cap
- Thermally Enhanced DFN3.2x5.5-17L package

Applications

- Thunderbolt/USB Type-C PD power switch
- Notebooks computer barrel jack
- Docking Stations / Dongles
- Power ORing applications



Typical Application





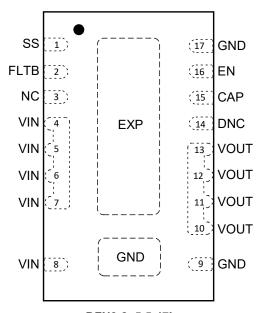
Ordering Information

Part Number	Start-up SCP Recovery	Junction Temperature Range	Package	Environmental
AOZ13287DI-01	Auto-Restart	-40°C to +125°C	DFN3.2x5.5-17L	RoHS



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



DFN3.2x5.5-17L (Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	SS	Soft-start pin. Connect a capacitor CSS from SS to GND to set the soft-start time.
2 FLTB Fault Indicator, Open-drain output. Pulls Low after a fault condition is detected.		Fault Indicator, Open-drain output. Pulls Low after a fault condition is detected.
3	NC	No Connect.
4, 5, 6, 7	VIN	Connect to adapter or power input. Place a 10 µF capacitor from VIN to GND.
8	Vin	Vin for TVS. Connect to the other VIN pins on PCB.
9 GND Ground for TVS. Connect to the Pin 17 on PCB.		Ground for TVS. Connect to the Pin 17 on PCB.
17 GND Ground. Connect to Pin 9 on PCB.		Ground. Connect to Pin 9 on PCB.
10, 11, 12, 13 VOUT Output pins. Connect to internal load.		Output pins. Connect to internal load.
14 DNC		Do Not Connect. Internally connected to Exposed Pad (EXP).
15 CAP		Connect a 1nF Capacitor to GND.
16 EN		Enable Active High.
GND GND C		Ground for TVS. Internally connected to Pin 9.
EXP EXP directly underneath the EXP and connect to		Common drain exposed thermal pad. For best thermal performance solder to a metal surface directly underneath the EXP and connect to other PCB layers through multiple VIAs. Exposed pad shall not be connected to any other signal or power and ground.

Rev. 1.0 January 2023 **www.aosmd.com** Page 2 of 17



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating		
VIN, VOUT to GND	-0.3V to +28V		
EN, SS, FLTB to GND	-0.3V to +6V		
CAP to VIN	-0.3V to +6V		
Junction Temperature (T _J)	+150°C		
Storage Temperature (T _S)	-65°C to +150°C		
ESD Rating HBM All Pins	±4kV		
IEC 61000-4-2 (Air and Contact) (1)	±30kV for Air ±30kV for Contact		
IEC 61000-4-5 (t _P = 8/20 µs)	30A		

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating		
Supply Voltage (VIN)	3.4V to 22V		
EN, FLTB	0V to 5.5V		
SS	0V to 3V		
DC Fully On Switch Current (I _{SW})	13A		
Peak Switch Current (I _{SW}) for 10 ms @ 2% Duty Cycle	22.5A		
Junction Temperature (T _J)	-40°C to +125°C		
Package Thermal Resistance DFN3.5x5.5-12L ($\Theta_{\rm JC}$) DFN3.5x5.5-12L ($\Theta_{\rm JA}$)	1.4°C/W 36°C/W		

Note:

Electrical Characteristics

 T_A = 25°C, VIN = 20V, EN = 5V, C_{IN} = 10 μ F, C_{OUT} = 10 μ F, C_{SS} = 5.6 nF, C_{CAP} = 1 nF, unless otherwise specified.

Symbol Parameter		Conditions	Min	Тур	Max	Units
General						
V_{VIN}	Input Supply Voltage		3.4		22	V
V _{UVLO}	Under-voltage Lockout Threshold	VIN rising	3.0		3.35	V
V _{UVLO_HYS}	Under-voltage Lockout Hysteresis			250		mV
I _{VIN_ON}	Input Quiescent Current	I _{VOUT} = 0A		500	750	μA
I _{VIN_OFF}	Input Shutdown Current	I _{VOUT} = 0A, EN = 0V		25	48	μA
I _{VOUT_OFF}	Output Leakage Current	VOUT = 20 V, VIN = 0 V, EN = 0 V		24	48	μA
R _{ON_20V}	Switch ON-Resistance ⁽²⁾	I _{VOUT} > 4.5A		9		mΩ
R _{ON_5V}	Switch ON-Resistance	VIN = 5V, I _{VOUT} > 4.5A		9.5		mΩ
V _{EN_H}	EN Input High Threshold	EN rising			1.4	V
V _{EN_L}	EN Input Low Threshold	EN falling	0.6			V
R _{EN_LO}	EN Input Pull-down Resistance		475	730	985	kΩ
V _{FLTB_LO}	FLTB Pin Pull-down Voltage	FLTB sinking 3mA			0.3	V
Input Over-	Voltage Protection					
V _{OVP}	Over-Voltage Protection Threshold	VIN rising	23	24	25	V
t _{OVP_DEB}	Over-Voltage Protection Debounce Time	Latch off. No restart.		512		μs

Rev. 1.0 January 2023 **www.aosmd.com** Page 3 of 17

^{1.} IEC 61000-4-2 discharge with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω



Electrical Characteristics (Continued)

 T_A = 25°C, VIN = 20V, EN = 5V, C_{IN} = 10 μ F, C_{OUT} = 10 μ F, C_{SS} = 5.6 nF, C_{CAP} = 1 nF, unless otherwise specified.

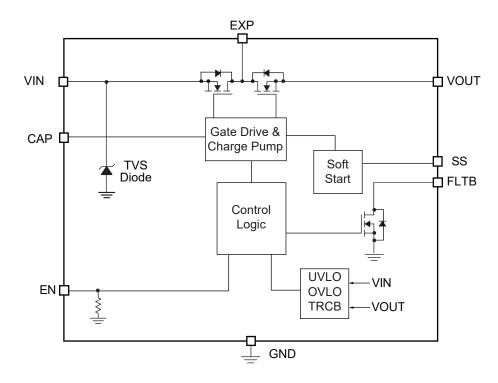
Symbol Parameter		Conditions	Min	Тур	Max	Units
Ideal Diode Tr	ue Reverse Current Blocking (ID	TRCB)	<u>'</u>			
V _{IDTRCB}	Ideal Diode TRCB Regulation Voltage	VIN – VOUT		35		mV
V _{FRCB}	Fast TRCB Threshold	VOUT - VIN		50		mV
t _{TRCB_DEL}	TRCB Delay Time			0.5		μs
	ng Characteristics					
t _{D_ON}	Turn-On Delay Time	From EN rising edge to VOUT reaching 10% of VIN		8		ms
t _{ON}	Turn-On Rise Time	VOUT from 10% to 90%		1.9		ms
t _{SCP_RST}	SCP Restart Time			64		ms
Thermal Shute	down Protection					
T _{SD}	Thermal Shutdown Threshold	Temperature rising. Latch off. No restart.		140		°C
Startup Short	Circuit Protection					
I _{SCP}	Current Limit Threshold for Short Circuit Protection	During Startup	13			А
TVS						
V_{RWM}	Reverse Working Voltage	Vin = Pin 8 , GND = Pin9			20	V
V_{BR}	Reverse Breakdown Voltage	I _T = 1mA at Vin at Vin = Pin 8 , GND=Pin9	22.1	24	26	V
V	Clamping Voltage ⁽³⁾⁽⁴⁾ (100ns Transmission Line Pulse,	I _{TLP} = 1A I _{TLP} = -1A At Vin=Pin 8 , GND=Pin9		25 -1		V
V _{CL}	Î/O Pin to GND(Pin9))	I _{TLP} = 30A I _{TLP} = -30A At Vin = Pin 8 , GND = Pin9		29 -3.5		V
R _{DYN}	Dynamic Resistance ⁽³⁾⁽⁴⁾	I _{TLP} = 1 to 30A I _{TLP} = -1 to -30A At Vin = Pin 8 , GND=Pin9		0.1 0.1		Ω
		I _{PP} = 10A I _{PP} = -10A At Vin=Pin 8 , GND=Pin9		26 -2	28 -3	V
V _{CL}	Clamping Voltage ⁽³⁾ (IEC61000-4-5 Surge 8/20μs)	I _{TLP} = 17A I _{TLP} = -17A At Vin = Pin 8 , GND = Pin9		28.5 -6	30 -9	V
		I _{TLP} = 30 A I _{TLP} = -30 A At Vin = Pin 8 , GND = Pin9		33.5 -6	35 -9	V
C _J	Junction Capacitance ⁽³⁾	V _{TLP} = 0V, f = 1Mhz, At Vin = Pin 8, GND = Pin9		200		pF

Note:

- 2. R_{ON} is tested at 1A in test mode to bypass ideal diode regulation.
- 3. These specifications are guaranteed by design and characterization.
- 4. Measurements performed using a 100ns Transmission Line Pulse (TLP) system.



Functional Block Diagram





Timing Diagrams

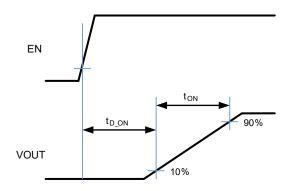


Figure 1. Turn-on Delay and Turn-on Time

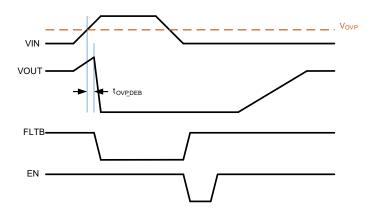


Figure 2. Over-voltage Protection

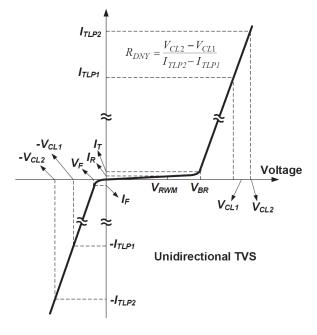


Figure 3. TVS Voltage vs. Current

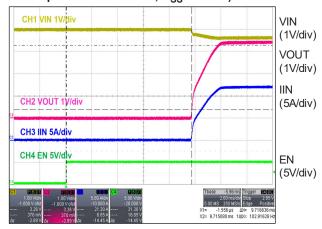
Rev. 1.0 January 2023 **www.aosmd.com** Page 6 of 17



Typical Characteristics

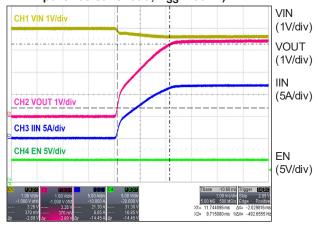
 $VIN = 20 \text{ V, EN} = 5 \text{ V, C}_{IN} = 10 \,\mu\text{F, C}_{OUT} = 10 \,\mu\text{F, C}_{SS} = 5.6 \,\text{nF, C}_{CAP} = 1 \,\text{nF, T}_{A} = 25 \,^{\circ}\text{C} \text{ , unless otherwise specified.}$

Soft Start Delay Time (VIN = 4V, Load = 12A pure resistive load, C_{SS} = 33nF)



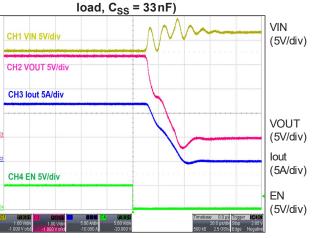
2.00ms/div

Soft Start Ramp (VIN = 4V, Load = 12A pure resistive load, C_{SS} = 33nF)



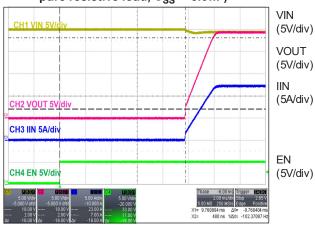
1.00ms/div

Shut Down (VIN = 4V, Load = 12A pure resistive



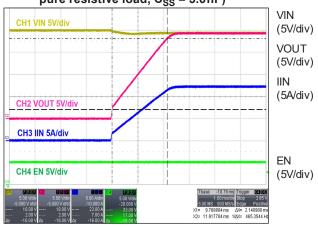
20µs/div

Soft Start Delay Time (VIN = 20 V, Load = 12 A pure resistive load, C_{SS} = 5.6 nF)



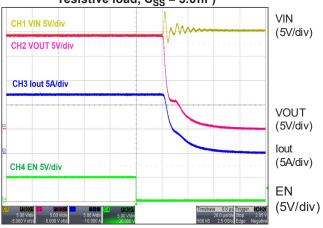
2.00ms/div

Soft Start Ramp (VIN = 20V, Load = 12A pure resistive load, C_{SS} = 5.6nF)



1.00ms/div

Shut Down (VIN = 20V, Load = 12A pure resistive load, C_{SS} = 5.6nF)



20µs/div

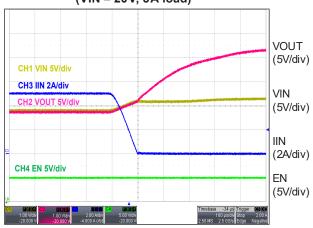
Rev. 1.0 January 2023 www.aosmd.com Page 7 of 17



Typical Characteristics (Continued)

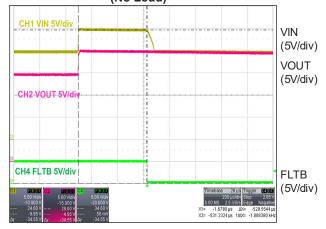
 $VIN = 20\,V,\,EN = 5\,V,\,C_{IN} = 10\,\mu\text{F},\,C_{OUT} = 10\,\mu\text{F},\,C_{SS} = 5.6\,\text{nF},\,C_{CAP} = 1\,\text{nF},\,T_A = 25^\circ\text{C}\,\,,\,\text{unless otherwise specified}.$

Ideal Diode True Reverse Current Blocking (VIN = 20V, 5A load)



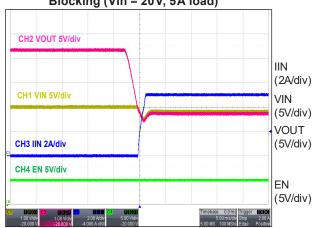
100µs/div

Over Voltage Protection Debounce Time (No Load)



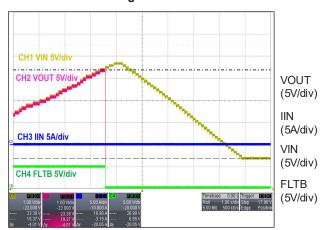
200µs/div

Recovery of Ideal Diode True Reverse Current Blocking (Vin = 20V, 5A load)



5.00ms/div

Over Voltage Protection



1.00s/div



Typical Characteristics

 $T_A = 25$ °C, unless otherwise specified.

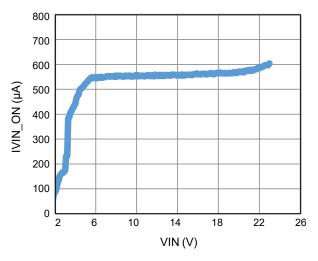


Figure 4. Quiescent Current vs. VIN

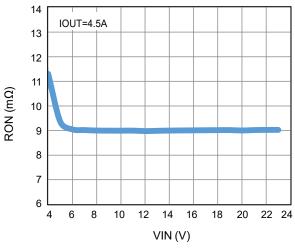


Figure 6. On Resistance (Rss) vs. VIN

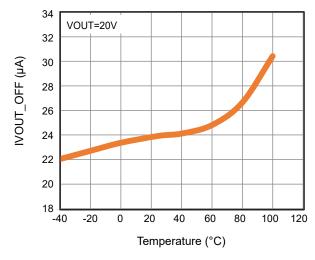


Figure 8. VOUT Reverse Current Leakage vs. Temperature

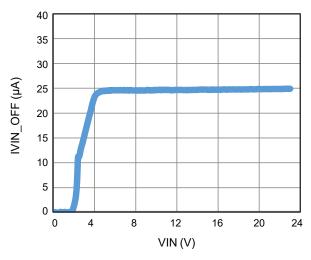


Figure 5. Shutdown Current vs. VIN

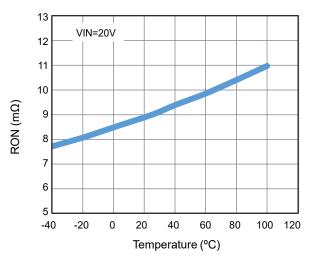


Figure 7. On Resistance (Rss) vs. Temperature

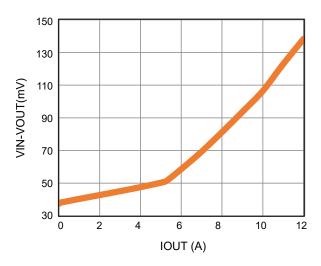


Figure 9. Ideal Diode Regulation Voltage vs. lout

Rev. 1.0 January 2023 **www.aosmd.com** Page 9 of 17



Typical Characteristics (Continued)

 $T_A = 25$ °C, unless otherwise specified.

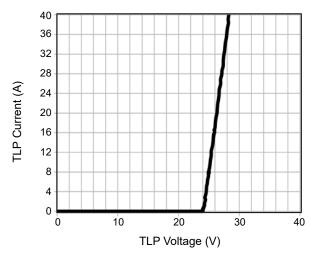


Figure 10. Positive Curve IEC61000-4-5 Surge $8/20\,\mu s$

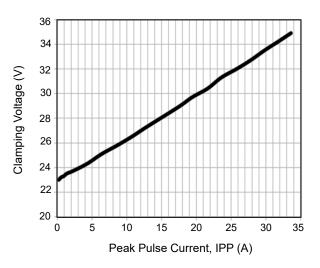


Figure 12. Typical Variations of C_J vs. Input Voltage

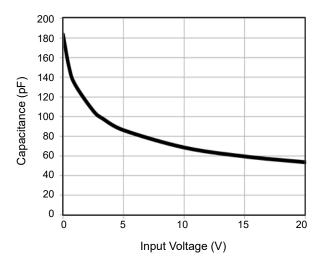


Figure 14. Input Voltage (V)

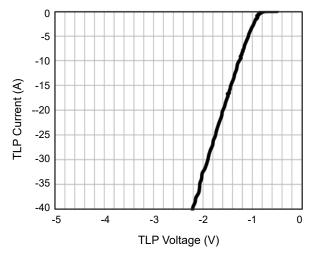


Figure 11. Negative Curve IEC610000-4-5 Surge 8/20µs

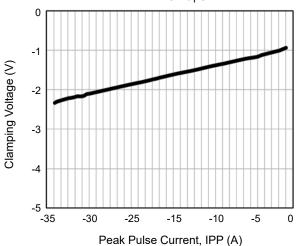


Figure 13. EPeak Pulse Current, IPP (A)



Detailed Description

The AOZ13287DI-01 is a high-side protection switch with programmable soft-start, over-voltage, and over-temperature protections. It is capable of operating from 3.4V to 22V. A TVS diode is integrated into the package for surge protection.

The internal power switch consists of back-to-back connected MOSFET. When the switch is enabled, the overall resistance between VIN and VOUT is only $9m\Omega$, minimizing power loss and heat generation. The back-to-back configuration of MOSFET completely isolates VIN and VOUT when the switch is turned off, preventing leakage between the two pins.

Power Delivery Capability

During start-up, the voltage at VOUT linearly ramps up to the VIN voltage over a period of time set by the soft-start time. This ramp time is referred to as the soft-start time and is typically in milliseconds. Figure 15 illustrates the soft-start condition and power dissipation.

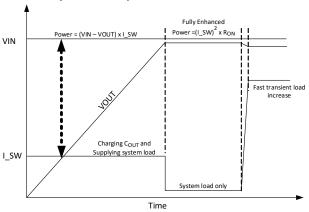


Figure 15. Soft-Start Power Dissipation

During this soft-start time, there will be a large voltage across the power switch. Also, there will be current I_SW through the switch to charge the output capacitance. In addition, there may be load current to the downstream system as well. This total current is calculated as:

$$I_{SW} = C_{OUT} \left(\frac{dVOUT}{dt} \right) + I_{SYS}$$

In the soft-start condition, the switch is operating in the linear mode, and power dissipation is high. The ability to handle this power is largely a function of the power MOSFET linear mode SOA and good package thermal performance $R\Theta_{JC}$ (Junction-to-Case) as the soft-start ramp time is in milliseconds. $R\Theta_{JA}$ (Junction-to-Ambient), which is more a function of PCB thermal performance, doesn't play a role.

With a high-reliability MOSFET as the power switch and superior packaging technology, the AOZ13287DI-01 is

capable of dissipating this power. The power dissipated is:

Power Dissipation =
$$I SW \times (VIN - VOUT)$$

To calculate the average power dissipation during the softstart period: $\frac{1}{2}$ of the input voltage should be used as the output voltage will ramp towards the input voltage, as shown in Figure 15.

For example, if the output capacitance C_{VOUT} is $10\,\mu\text{F}$, the input voltage VIN is 20V, the soft-start time is 2ms, and there is an additional 1A of system current (I_SYS), then the average power being dissipated by the part is:

$$I_{SW} = 10 \mu F \left(\frac{20 V}{2 m s}\right) + 1A = 1.1A$$

Average Power Dissipation =
$$1.1A \times \frac{20V}{2} = 11W$$

Referring to the SOA curve in Figure 16, the maximum power allowed for 2ms is 140W. The AOZ13287DI-01 power switch is robust enough to drive a large output capacitance with load in reasonable soft-start time.

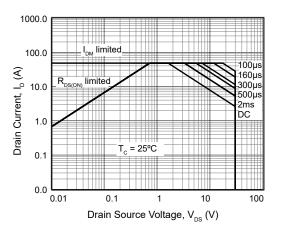


Figure 16. Safe Operating Area (SOA) Curves for Power Switch

After soft-start is completed, the power switch is fully on, and it is at its lowest resistance under heavy load condition. The power switch acts as a resistor. Under this condition, the power dissipation is much lower than the soft-start period. However, as this is a continuous current, a low on-resistance is required to minimize power dissipation. Attention must be paid to board layout so that losses dissipated in the sinking switch are dissipated to the PCB and hence the ambient.

Rev. 1.0 January 2023 www.aosmd.com Page 11 of 17



With a low on-resistance of $9m\Omega$, the AOZ13287DI-01 provides the most efficient power delivery without much resistive power dissipation.

While Type C power delivery is limited to 20V @ 5A or a 100W, many high-end laptops require peak currents far in excess of the 5A. While the thermal design current (TDC) for a CPU may be low, peak current (ICCmax in the case of Intel and EDP in the case of AMD) of many systems is often 2 x thermal design current. These events are typical of short duration (<2ms) and low duty cycle, but they are important for system performance as a CPU/GPU capable of operating at several GHz can boost its compute power in those 2ms peak current events. The AOZ13287DI-01 can handle such short, high current, transient pulses without any reliability degradation, thus enhancing the performance of high-end systems when plugged into the Type C adapter. The shorter the pulse and the lower the duty cycle, the higher the pulse current that the part can sustain. The part has enough time to dissipate the heat generated from the pulse current with longer off-time, as shown in Figure 17. For example, AOZ13287DI-01 can maintain 22.5A for 10 ms with a duty cycle of 2%.

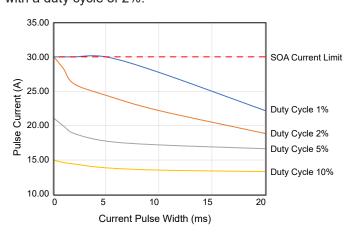


Figure 17. AOZ13287DI-01 Sinking Switch Pulsed Current vs. Duration for a Given Duty Cycle

Enable

The active high EN pin is the ON/OFF control for the power switch. The device is enabled when the EN pin is high and not in UVLO state. The EN pin must be driven to a logic high (V_{EN_H}) or logic low (V_{EN_L}) state to guarantee operation. AOZ13287DI-01 draws about 25µA supply current when it is disabled.

Input Under-Voltage Lockout (UVLO)

The internal control circuit is powered from VIN. The under-voltage lockout (UVLO) circuit monitors the voltage at the input pin (VIN) and only allows the power switches to turn on when it is higher than V_{UVLO} . If VIN is below V_{UVLO} , the device is in under-voltage lockout state.

Over-Voltage Protection (OVP)

The voltages at VIN pin are constantly monitored once the device is enabled. In case the voltage exceeds the OVP threshold, over-voltage protection is activated:

- If the power switch is on, it will be turned off after OVP debounce time (t_{OVP DEB}) to isolate VOUT from VIN;
- 2. OVP will prevent power switch to be turned on if it is in off state:

In either case FLTB pin is pulled low to report the fault condition. The device can only be re-enabled by either toggling EN pin or cycling the input power supply.

Ideal Diode True Reverse Current Blocking

When the device is ON with no load or under light load conditions, it regulates VOUT to be 35mV below VIN. As the load current is increasing or decreasing, the device adjusts the gate drive to maintain the 35mV drop from VIN to VOUT. As the load current continues to increase the device increases the gate drive until the gate is fully turned on and VIN to VOUT drop is determined by IR drop through the MOSFET. If for any reason VOUT increases such that VIN to VOUT drop to less than 35mV, the gate driver forces the switch to turn off.

The AOZ13287DI-01 also features a fast comparator that turns off the power switch upon detection of VOUT – VIN is higher than V_{FRCB} after TRCB delay time (t_{TRCB_DEL}) . When the AOZ13287DI-01 is first enabled or during each autorestart, power switch will be kept off if VOUT is V_{FRCB} higher than VIN.

Thermal Shutdown Protection

When the die temperature reaches 140°C, the power switch is turned off. The device can only be re-enabled by either toggling EN pin or cycling the input power supply.

Soft-Start Slew-Rate Control

When EN pin is asserted high, the slew rate control applies voltage on the gate of the power switch in a manner such that the output voltage is ramped up linearly until VOUT reaches VIN voltage level. The output ramps up time (t_{ON}) is programmable by an external soft-start capacitor (C_{SS}) . The following formula provides the estimated 10% to 90% ramp up time.

$$t_{ON} = \left(\frac{VIN}{24}\right) \times \left(\left(\frac{C_{SS}}{0.0023}\right) - 100\right)$$

where C_{SS} is in nF and t_{ON} is in μ s.



System Startup

The device is enabled when EN \geq 1.4V and VIN is higher than UVLO threshold (V_{UVLO}). The device will check if any fault condition exists. If no fault exists, the power switch is turned on and VOUT is then ramped up after enable delay (t_{D_ON}), controlled by the soft-start time (t_{ON}) until VOUT reaches VIN voltage level. Soft-start time can be programmed externally through SS input with a capacitor CSS to control in-rush current.

In-rush Current Limit and SCP at Start-up

AOZ13287DI-01 has the current limit and short circuit protection functions at start-up. The current limit ramp increases linearly and reaches to a fixed current within 1.25 ms. With this fixed current limit ramp, the inrush current can be effectively clamped to reduce the initial current spikes. At initial startup, the internal power switch carries large voltage close to Vin and has large power loss. To ensure the internal FET working in Safe Operation Area (SOA), a fixed timer is set to shut down the power switch if the inrush current is clamped by current limit ramp for about 380 µs continuously. This timer will be reset once the inrush current drops below the current limit ramp. For short circuit event, the part will shut down after this 380 µs timer is finished. In case of large output capacitors, the soft-start time needs to increase to avoid the large inrush current hit the current limit ramp for 380 µs. The AOZ13287DI-01 will auto-retry soft start after 64ms (t_{SCP RST}) blanking time. This auto-restart feature enables the device to be used in systems with a large output capacitance on the Vout node. Both current limit and SCP shutdown functions are disabled after the switch is fully turned on.

Fault Protection

The AOZ13287DI-01 offers multiple protection against the following fault conditions: VIN Over Voltage Protection (OVP), True Reverse Current Blocking when VOUT > VIN, and over temperature.

When the device is first enabled, the power switch is off and fault conditions are checked. If any of these conditions exist:

- 1. VIN is higher than the OVP threshold (V_{OVI O});
- Die temperature is higher than thermal shutdown threshold (T_{SD});
- 3. VOUT is V_{FRCB} higher than VIN

The power switch will not be turned on and FLTB pin will be pulled low for OVP and TSD conditions but not IDTRCB condition to indicate fault status of the device.

The power switch will be turned on once IDTRCB condition

no longer exists. The device will continuously monitor these fault conditions. In addition, the short circuit condition is being monitored during the soft start. See previous section on SCP at start up for more details.

Table 1. Fault Flag Response to All Protection Functions

Protection	Fault Response	FLTB Status		
IDTRCB	Auto-restart without soft start at fault removal	High Impedance		
Startup SCP	Auto-restart after 64ms	Low		
TSD	Latch-off	Low		
OVP	Latch-off	Low		

Input Capacitor Selection

The input capacitor prevents large voltage transient from appearing at the input. It also provides the instantaneous current needed when the power switch turns on to charge output capacitors while limiting the input voltage drop. It is also to prevent high-frequency noise on the power line from passing through to the output. The input capacitor should be located as close to the VIN pin as possible. A 10 µF ceramic capacitor is recommended.

Output Capacitor Selection

The output capacitor has to supply enough current for a large peak current load that it may encounter during system transient. This bulk capacitance must be large enough to supply fast transient load in order to prevent the output from dropping.

Power Dissipation Calculation

The following equation can be used to estimate the power dissipation for normal load condition:

Power Dissipated =
$$R_{ON} \times (I_{OUT})^2$$



Layout Guidelines

AOZ13287DI-01 is a protection switch designed deliver high current. Layout is critical to remove the heat generated by this current. For the most efficient heat sinking, connect as much copper as possible to the exposed pad. The exposed pad is the common drain of the power switch which must be electrically isolated.

On the top layer expand the exposed pad island as much as possible for optimal thermal performance. The exposed pad copper plane must be electrically isolated. See example in Figure 18.

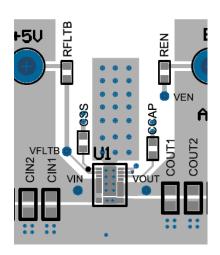


Figure 18. Top layer layout. Maximum number of VIAs from top layer exposed pad to inner layer.

The more layers that have these electrically isolated thermal heat sink islands the better the thermal performance will be. Connect all isolated thermal island (top, inner layers and bottom) together with as many VIAs as possible. On the bottom layer, similar to the inner layers, create an isolated thermal island. Typically, there is more area available on the bottom area for a larger thermal pad. The top and bottom layers have better thermal performance than the inner layers because they are exposed to the atmosphere. See example in Figure 19.

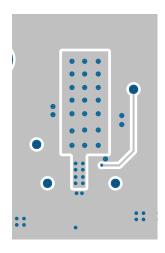
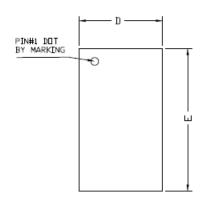
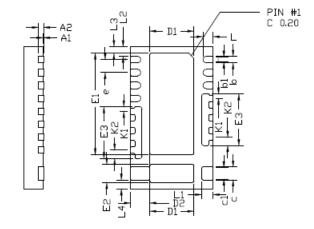


Figure 19. Bottom layer layout. Create a large electrically isolated thermal pad.



Package Dimensions, DFN3.2x5.5B-17L





TOP VIEW

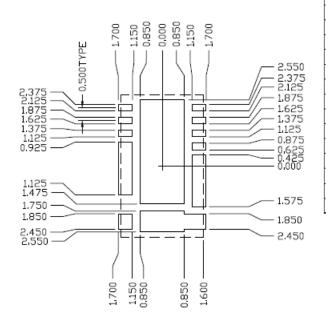
SIDE VIEW

BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
STWIBULS	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.650	0.750	0.850	0.026	26 0.030 0.	
A1	0.000	-	0.050	0.000	-	0.002
A2	0.2REF		0.008REF			
D	3.100	3.200	3.300	0.122	0.126	0.130
E	5.400	5.500	5.600	0.213	0.217	0.220
D1	1.650	1.700	1.750	0.065	0.067	0.069
D2	0.700	0.750	0.800	0.028	0.030	0.031
E1	3.875	3.925	3.975	0.153	0.155	0.156
E2	0.650	0.700	0.750	0.026 0.028		0.030
E3	E3 1.950 2.000 2.050		0.077	0.079	0.081	
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.400	0.450	0.500	.500 0.016 0.01		0.020
L2	0.325	0.375	0.425	0.013 0.015		0.017
L3	0.200	0.250	0.300	0.008 0.010 0		0.012
L4	0.300	0.350	0.400	0.012	0.014	0.016
K1	0.125	0.175	0.225	0.005 0.007 0		0.009
K2	0.275	0.325	0.375	0.011 0.013		0.015
b	0.200	0.250	0.300	0.008 0.010		0.012
b1	0.140	0.190	0.240	0.006	0.007	0.009
С	0.450	0.500	0.550	0.018	0.020	0.022
c1	0.390	0.440	0.490	0.015	0.017	0.019
е	0.50BSC			0.02BSC		

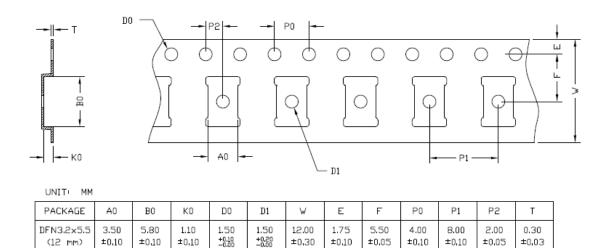
NOTE CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

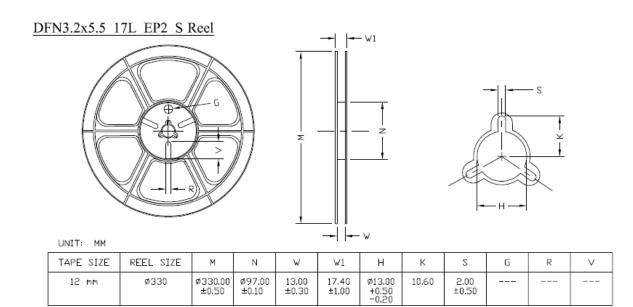
Rev. 1.0 January 2023 **www.aosmd.com** Page 15 of 17



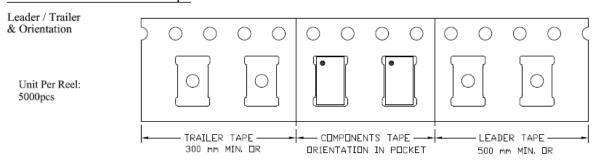
Tape and Reel Dimensions, DFN3.2x5.5B-17L

DFN3.2x5.5_17L_EP2_S Carrier Tape





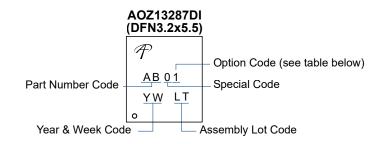
DFN3.2x5.5 17L EP2 S Tape



Rev. 1.0 January 2023 **www.aosmd.com** Page 16 of 17



Part Marking



Part Number	Description	Code	
AOZ13287DI-01	Green Product	AB01	

LEGAL DISCLAIMER

Applications or uses as critical components in life support devices or systems are not authorized. Alpha and Omega Semiconductor does not assume any liability arising out of such applications or uses of its products. AOS reserves the right to make changes to product specifications without notice. It is the responsibility of the customer to evaluate suitability of the product for their intended application. Customer shall comply with applicable legal requirements, including all applicable export control rules, regulations and limitations.

AOS's products are provided subject to AOS's terms and conditions of sale which are set forth at: http://www.aosmd.com/terms_and_conditions_of_sale

LIFE SUPPORT POLICY

ALPHA AND OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Rev. 1.0 January 2023 www.aosmd.com Page 17 of 17