ALPHA & OMEGA SEMICONDUCTOR

AOZ21502QI-10

28V Input, 10V/4A Output Synchronous EZBuck™ Regulator

General Description

The AOZ21502QI-10 is a high-efficiency, easy-to-use DC/DC buck regulator that is targeted for system-power supply solution. It provides 5V LDO. The devices are capable of supplying 4A of continuous output current with 10V output voltage.

A proprietary constant on-time control with input feed-forward results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range.

The device features multiple protection functions such as LDO under-voltage lockout, cycle-by-cycle current limit, output over-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ21502QI-10 is available in a 3mm×3mm QFN-21L package and is rated over a -40°C to +85°C ambient temperature range.

Features

- Wide input voltage range
  - 12V to 28V
- 4A continuous output current
- Output voltage: 10V
- Low $R_{DS(ON)}$ internal NFETs
  - 28mΩ high-side
  - 28mΩ low-side
- Constant On-time with input feed-forward
- Output voltage ripple reduction at light load
- Light-load mode selectable from ultrasonic mode (USM), PFM mode and forced PWM mode
- Ceramic capacitor stable
- Adjustable soft-start
- Power Good output
- Integrated bootstrap diode
- Cycle-by-cycle current limit
- Short-circuit protection
- Hiccup mode after triggering protections
- Thermal shutdown
- Thermally enhanced 21-pin 3mm× 3mm QFN

Applications

- Notebook fan power
- DC fan
- 10V Point of load DC/DC converter

GREEN Product

Typical Application

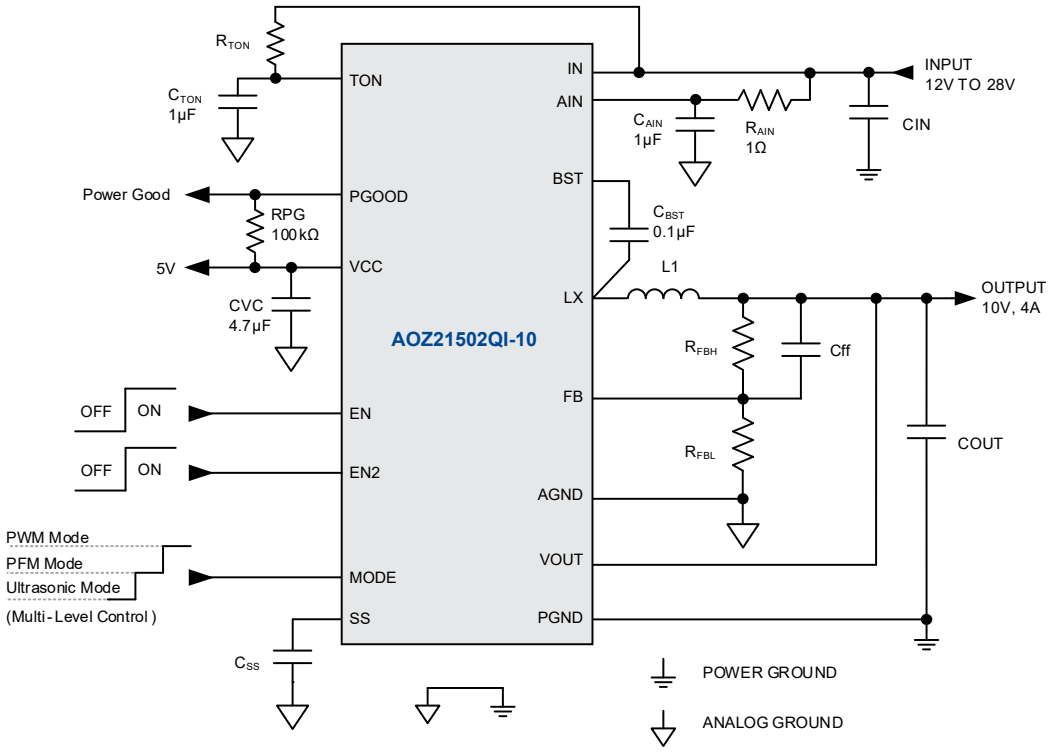


Table 1. Recommended BOM List

Part	Value
CIN	40µF
COUT	80µF
R_{AIN}	1Ω
C_{AIN}	1µF
R_{TON}	1MΩ
C_{TON}	1µF
RPG	100kΩ
CVC	4.7µF
C_{SS}	22nF
C_{BST}	100nF
L1	4.7µH
R_{FBH}	30kΩ
R_{FBL}	7.5kΩ
Cff	33pF

Ordering Information

Part Number	Temperature Range	Package	Environmental
AOZ21502QI-10	-40°C to +85°C	21-Pin 3mm × 3mm QFN	Green

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

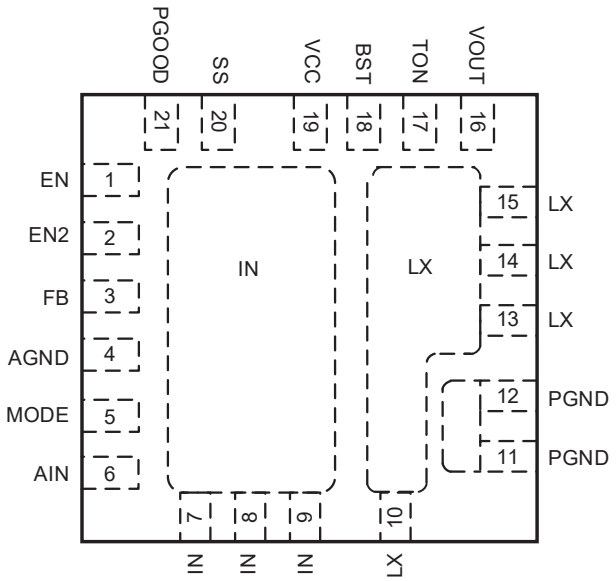


Figure 1. AOZ21502QI-10
21-Pin 3mm x 3mm QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	EN	Enable Input. The device is enabled when EN is pulled high. The device shuts down when EN is pulled low. Assert EN to high for power-up after IN is supplied.
2	EN2	Internal 5V LDO Enable Input. The 5V LDO is enabled when EN2 is pulled high. The 5V LDO shuts down when EN2 is pulled low. Connect this pin with EN signal if individually LDO control is not needed.
3	FB	Feedback Input. Adjust the output voltage with a resistive voltage-divider between the regulator's output and AGND.
4	AGND	Analog Ground.
5	MODE	MODE Selection. Connect this pin to a DC bias to set the operation mode to ultrasonic mode (USM), pulse-frequency modulation (PFM) mode or pulse-width modulation (PWM) mode. Refer to electronic table for mode setting information.
6	AIN	LDO Input. Connect this pin to input power directly.
7, 8, 9	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
10, 13, 14, 15	LX	Switching Node.
11, 12	PGND	Power Ground.
16	VOUT	Output voltage sense. This pin is used in ultrasonic mode compensation. Connect this pin to output node directly.
17	TON	On-Time Setting Input. Connect a resistor between VIN and TON to set the on-time, and shunt a 1µF bypass capacitor to ground.
18	BST	Bootstrap Capacitor Connection. The device includes an internal bootstrap diode. Connect an external capacitor between BST and LX.
19	VCC	LDO Output.
20	SS	Soft-Start Time Setting Pin. Connect a capacitor between SS and AGND to set the soft-start time.
21	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 10% lower than the nominal regulation voltage or 20% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
IN, AIN to AGND	-0.3V to 30V
LX, TON, VOUT to AGND(1)	-0.3V to 30V
BST to AGND	-0.3V to 36V
PGND to AGND	-0.3V to +0.3V
Other Pins to AGND	-0.3V to 6V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating-HBM(2)	2kV
ESD Rating-CDM	1kV

Notes:

1. LX to PGND Transient (t<20ns) ------- -7V to Vin+7V.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5KΩ in series with 100pF

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
Supply Voltage (V_{IN})	12V to 28V
Output Voltage (V_{OUT})	10V
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance (θ_{JA}) (θ_{JC})	 40°C/W 6°C/W

Electrical Characteristics

T_A = 25°C, V_{IN}=20V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

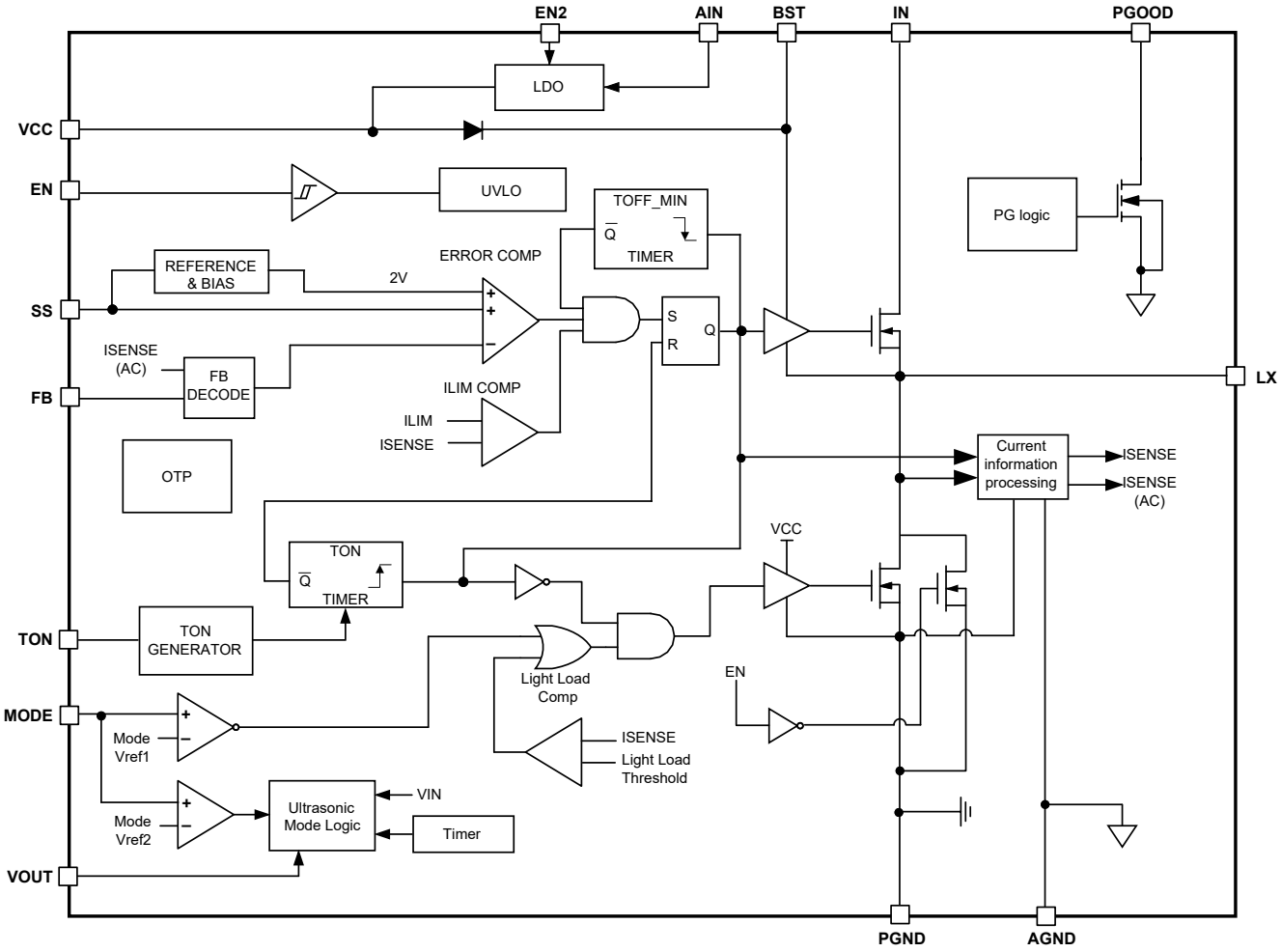
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	IN Supply Voltage		**12**		**28**	V
V_{UVLO}	Under-Voltage Lockout Threshold of V_{IN}	V_{IN} rising V_{IN} falling		**4.2** **3.9**		V
I_q	Quiescent Supply Current of V_{IN}	I_{OUT} = 0A, V_{EN}> 2V, PFM mode		**650**		µA
I_{OFF}	Shutdown Supply Current of V_{IN}	V_{IN} = 20V, V_{EN} = 0V		**10**		µA
V_{REF}	Reference Voltage	T_A = 25°C T_A = 0°C to 85°C	1.980 1.970	2.000 2.000	2.020 2.030	V
I_{FB}	FB Input Bias Current				200	nA
Enable						
V_{EN}	EN Input Threshold	Off threshold On threshold	 1.6		0.5	V
V_{EN_HYS}	EN Input Hysteresis			300		mV
Mode Selection						
V_{MODE}	Mode Voltage	Ultrasonic Mode PFM Mode FPWM Mode	 1.6 2.6		1.4 2.4	V
T_{USM}	Switching Period at Ultrasonic Mode	V_{MODE} = 1.5V, Ultrasonic Mode		20		µs
Overshoot Improvement (OHI)						
ΔV_{OHI}	The spacing between OHI threshold and V_{REF}		40	50	60	mV

Electrical Characteristics

T_A = 25°C, V_{IN}=20V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Modulator						
T_{ON_MIN}	Minimum On-time			130		ns
T_{ON_MAX}	Maximum On-time	Ultrasonic Mode		10000		ns
T_{ON_MAX2}	Maximum On-time 2	PFM or FPWM Mode		6000		ns
T_{OFF_MIN}	Minimum Off-time			300		ns
Soft-start						
I_{SS_OUT}	SS Source Current	V_{SS} = 0V C_{SS} = 0.001µF to 0.1µF	8	11	13	µA
Power Good Signal						
V_{PG_LOW}	PGOOD Low Voltage	I_{OL} = 500µA			0.5	V
	PGOOD Leakage Current				±1	µs
V_{PGH}	PGOOD Threshold (Low level to High level)	FB rising		95		%
V_{PGL}	PGOOD Threshold (High level to Low level)	FB rising FB falling		120 80		%
Under Voltage and Over Voltage Protection						
V_{PL}	Under Voltage Threshold	FB falling		50		%
V_{PH}	Over Voltage Threshold	FB rising		120		%
Power Stage Output						
$R_{DS(ON)}$	High-Side NFET On-Resistance	V_{IN} = 20V, V_{CC} = 5V		28		mΩ
	High-Side NFET Leakage	V_{EN} = 0V, V_{LX} = 0			10	µA
$R_{DS(ON)}$	Low-Side NFET On-Resistance	V_{LX} = 20V, V_{CC} = 5V		28		mΩ
	Low-Side NFET Leakage	V_{EN} = 0V			10	µA
Over-current and Thermal Protection						
I_{LIM}	Current Limit	V_{OUT} = 5V	10			A
	Thermal Shutdown Threshold	T_J rising T_J falling		150 100		°C
LDO Output						
V_{CC}	LDO Output Voltage	V_{IN} > 5.5V, V_{OUT} = 0V, I_{CC} < 35mA	4.85	5.0	5.10	V
I_{CC}	LDO Current Limit	V_{OUT} = 0V, V_{CC} = 4.5V, V_{IN} = 20V	50	100		mA
Output Discharge						
R_{DIS}	Discharge Resistance	V_{EN} = 0V, V_{LX} = 0.1V,		100		Ω

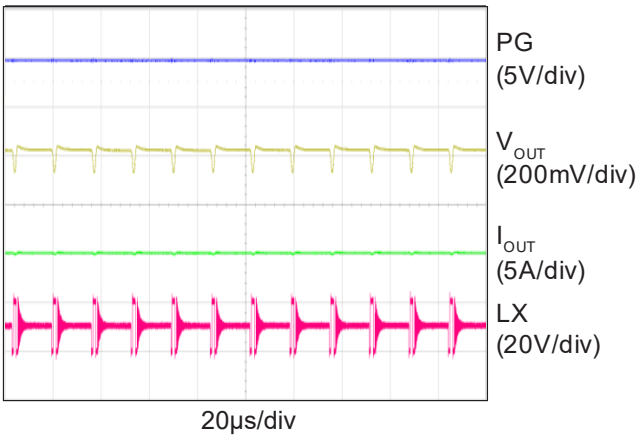
Functional Block Diagram



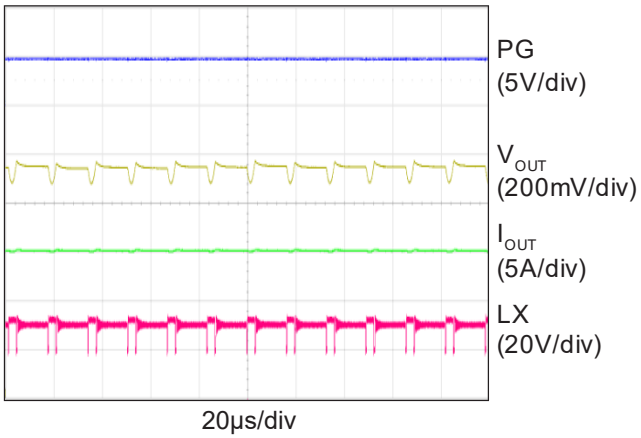
Typical Characteristics

T_A = 25°C, V_{IN} = 12V/20V, V_{OUT} = 10V, fs = 400kHz, L = 4.7µH, C_{OUT} = 10µF*8, unless otherwise specified.

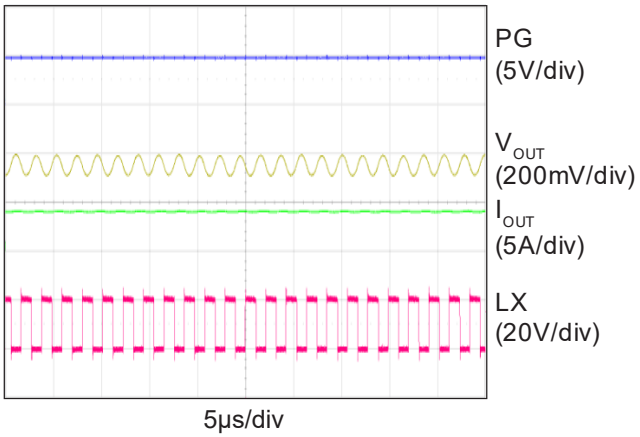
Normal Operation (USM)
(V_{IN} = 20V, I_{OUT} = 0A)



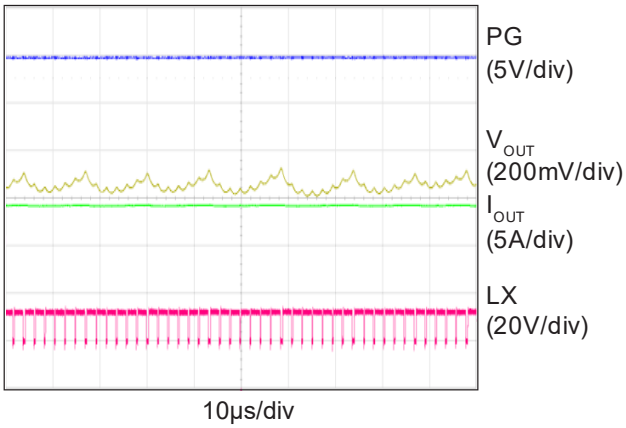
Normal Operation (USM)
(V_{IN} = 12V, I_{OUT} = 0A)



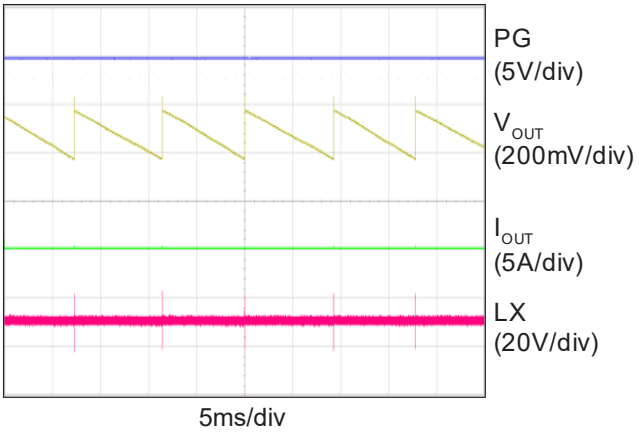
Normal Operation (USM)
(V_{IN} = 20V, I_{OUT} = 4A)



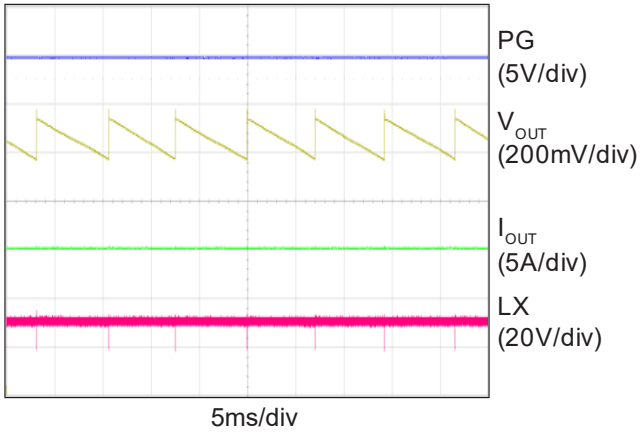
Normal Operation (USM)
(V_{IN} = 12V, I_{OUT} = 4A)



Normal Operation (PFM)
(V_{IN} = 20V, I_{OUT} = 0A)



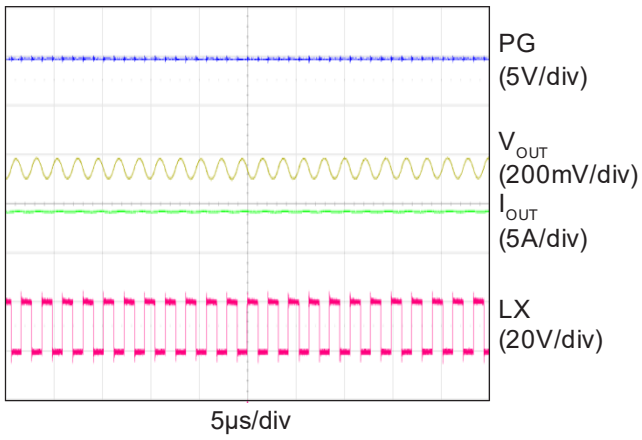
Normal Operation (PFM)
(V_{IN} = 12V, I_{OUT} = 0A)



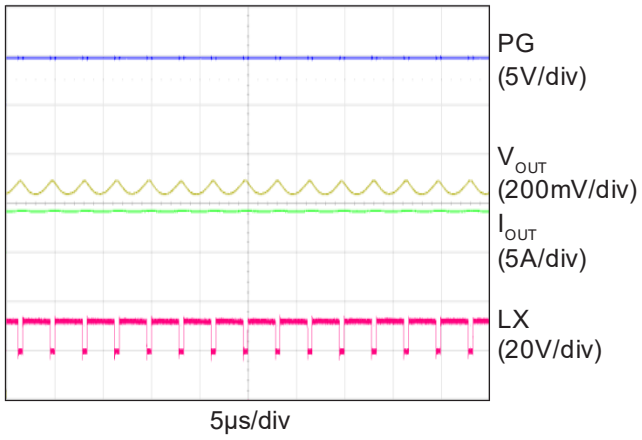
Typical Characteristics

T_A = 25°C, V_{IN} = 12V/20V, V_{OUT} = 10V, fs = 400kHz, L = 4.7µH, C_{OUT} = 10µF*8, unless otherwise specified.

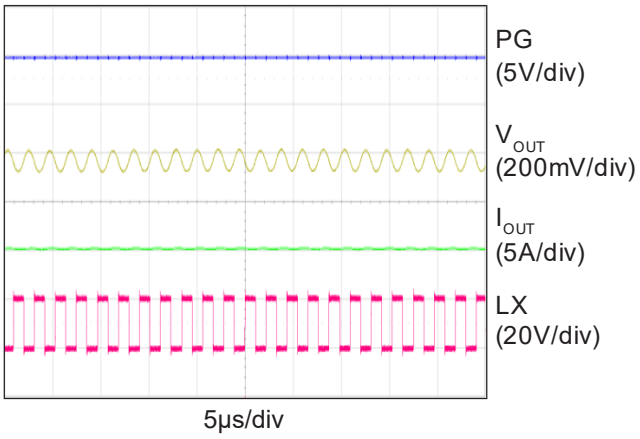
Normal Operation (PFM)
(V_{IN} = 20V, I_{OUT} = 4A)



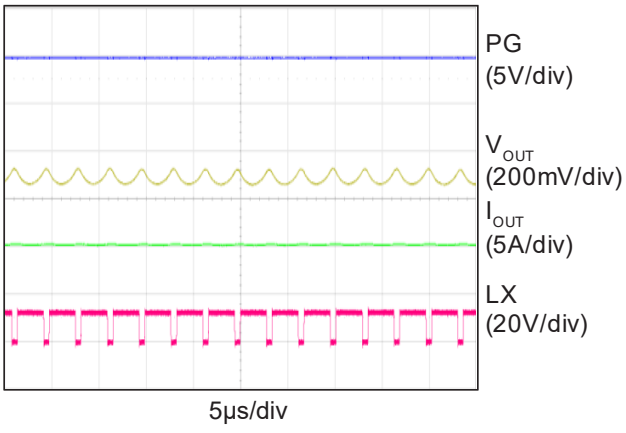
Normal Operation (PFM)
(V_{IN} = 12V, I_{OUT} = 4A)



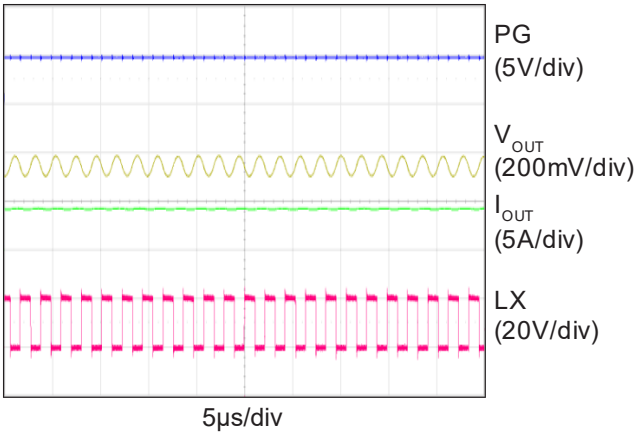
Normal Operation (PWM)
(V_{IN} = 20V, I_{OUT} = 0A)



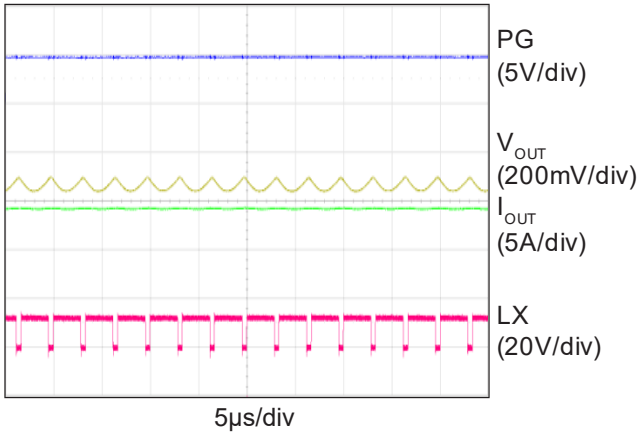
Normal Operation (PWM)
(V_{IN} = 12V, I_{OUT} = 0A)



Normal Operation (PWM)
(V_{IN} = 20V, I_{OUT} = 4A)



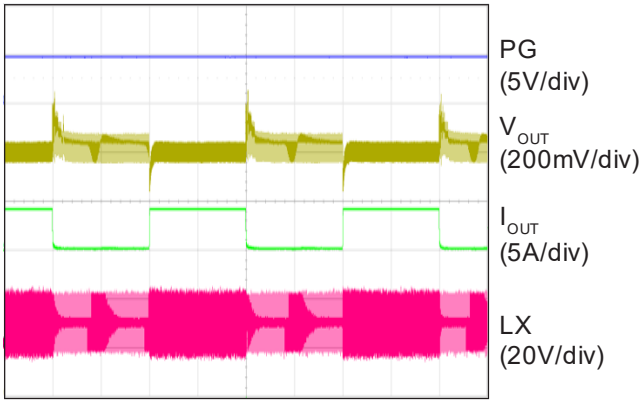
Normal Operation (PWM)
(V_{IN} = 12V, I_{OUT} = 4A)



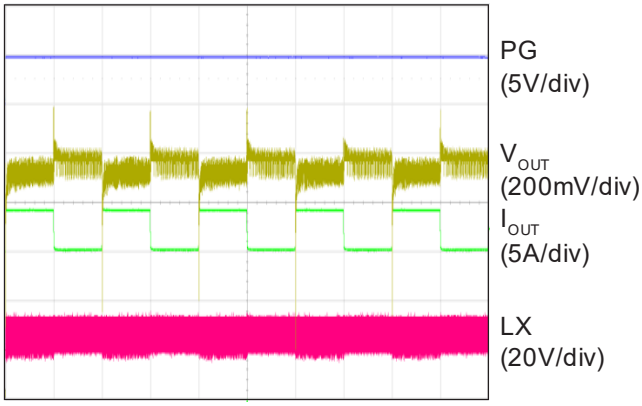
Typical Characteristics

T_A = 25°C, V_{IN} = 12V/20V, V_{OUT} = 10V, fs = 400kHz, L = 4.7µH, C_{OUT} = 10µF*8, unless otherwise specified.

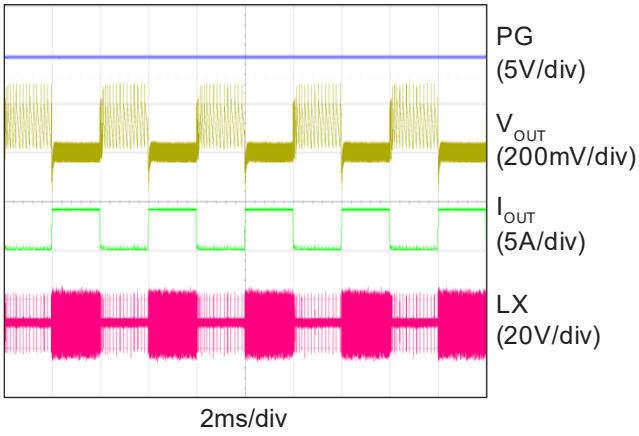
Load Transient (USM)
(V_{IN} = 20V, I_{OUT} = 0A~4A)



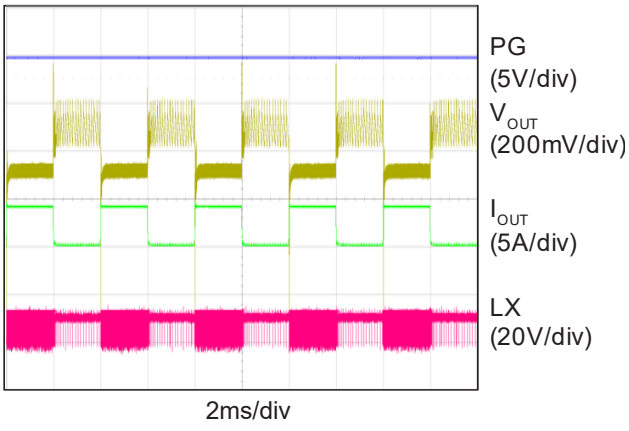
Load Transient (USM)
(V_{IN} = 12V, I_{OUT} = 0A~4A)



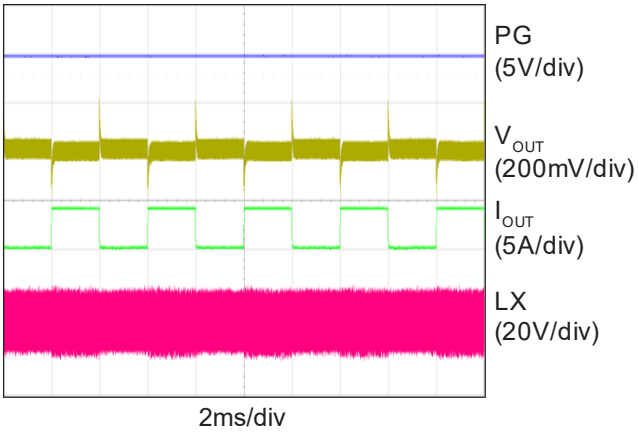
Load Transient (PFM)
(V_{IN} = 20V, I_{OUT} = 0A~4A)



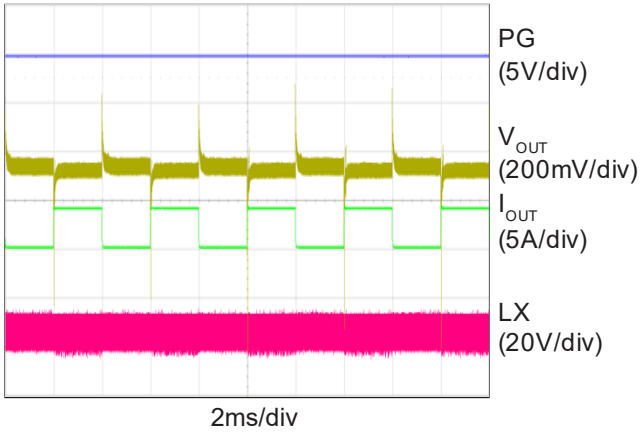
Load Transient (PFM)
(V_{IN} = 12V, I_{OUT} = 0A~4A)



Load Transient (PWM)
(V_{IN} = 20V, I_{OUT} = 0A~4A)



Load Transient (PWM)
(V_{IN} = 12V, I_{OUT} = 0A~4A)



Typical Characteristics

T_A = 25°C, V_{IN} = 12V/20V, V_{OUT} = 10V, fs = 400kHz, L = 4.7µH, C_{OUT} = 10µF*8, unless otherwise specified.

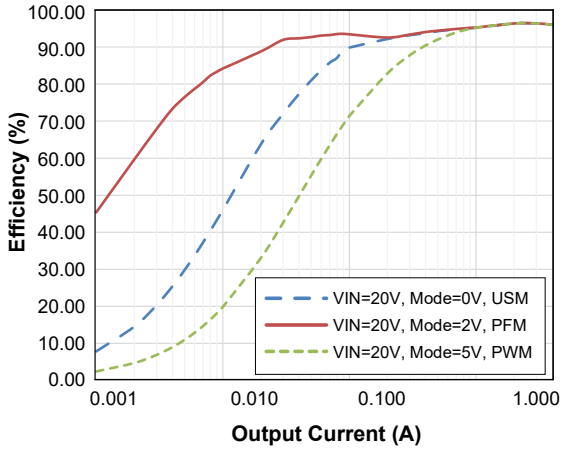


Figure 2. Efficiency, V_{IN} = 20V, I_{OUT} = 1mA~4A

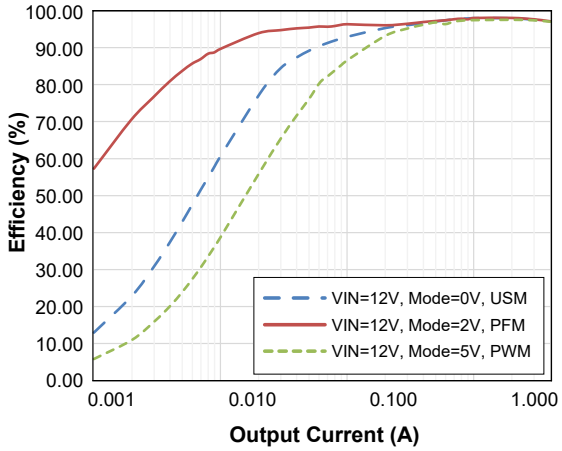


Figure 3. Efficiency, V_{IN} = 12V, I_{OUT} = 1mA~4A

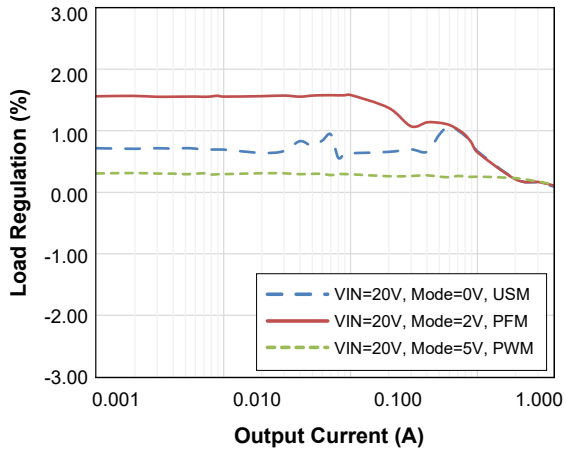


Figure 4. Load Regulation, V_{IN} = 20V, I_{OUT} = 1mA~4A

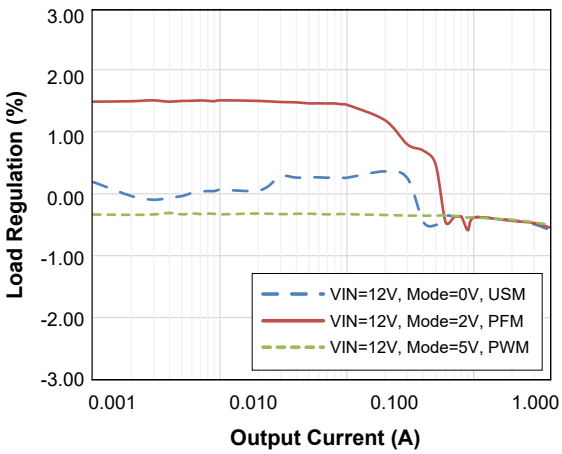


Figure 5. Load Regulation, V_{IN} = 12V, I_{OUT} = 1mA~4A

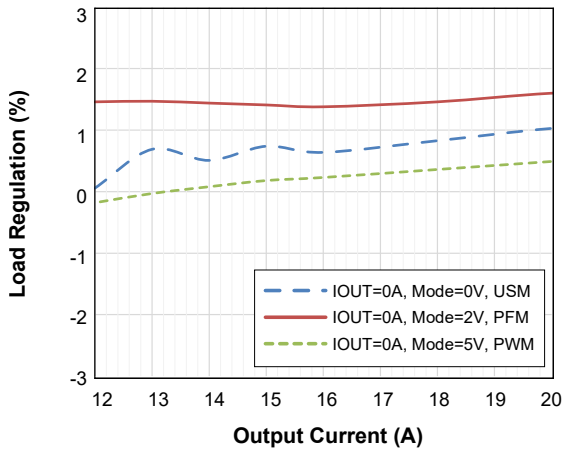


Figure 6. Line Regulation, V_{IN} = 12V ~20V, I_{OUT} = 0A

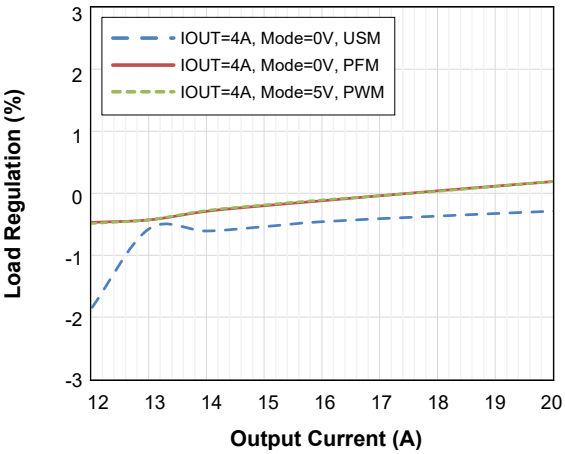


Figure 7. Line Regulation, V_{IN} = 12V ~20V, I_{OUT} = 4A

Detailed Description

The AOZ21502QI-10 is a high-efficiency, easy-to-use DC/DC buck regulator that is targeted for system-power supply solution. It provides 5V LDO. The devices are capable of supplying 4A of continuous output current with 10V output voltage.

The input voltage of AOZ21502QI-10 can be as low as 12V. The highest input voltage of AOZ21502QI-10 can be 28V. Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulators can be stable with ceramics output capacitor. The AOZ21502QI-10 also has switch over function. When the output voltage ready and PGOOD signal is pulled high, the internal LDO is turned off, and then the power of AOZ21502QI-10 internal control circuit is supplied by output terminal to reduce the LDO power loss. Protection features include LDO under-voltage lockout, cycle-by-cycle current limit, output over voltage and under-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ21502QI-10 is available in 21-pin 3mm×3mm QFN package

Enable and Soft-start

The AOZ21502QI-10 has external soft-start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulate voltage. A soft-start process begins when V_{CC} rises to over than UVLO threshold and the EN pin voltage is HIGH. An internal current source charges the external soft-start capacitor; the FB voltage follows the voltage of soft-start pin (V_{SS}) when it is lower than 2V. When V_{SS} is higher than 2V, the FB voltage is regulated by internal precise band-gap voltage (2V). When V_{SS} is higher than 3.8V, the PGOOD signal is pulled high. The soft-start time for PGOOD can be calculated by the following formula:

$$T_{SS\_PG}(\mu s)=380*C_{SS}(nF)$$

If C_{SS} is 1nF, the PGOOD high time will be 380μ seconds; if C_{SS} is 10nF, the PGOOD high time will be 3.8m seconds.

The soft-start time for V_{OUT} ready can be calculated by the following formula:

$$T_{SS\_VOUT}(\mu s)=200*C_{SS}(nF)$$

If C_{SS} is 1nF, the V_{OUT} ready time will be 200μ second; if C_{SS} is 10nF, the V_{OUT} ready time will be 2m second.

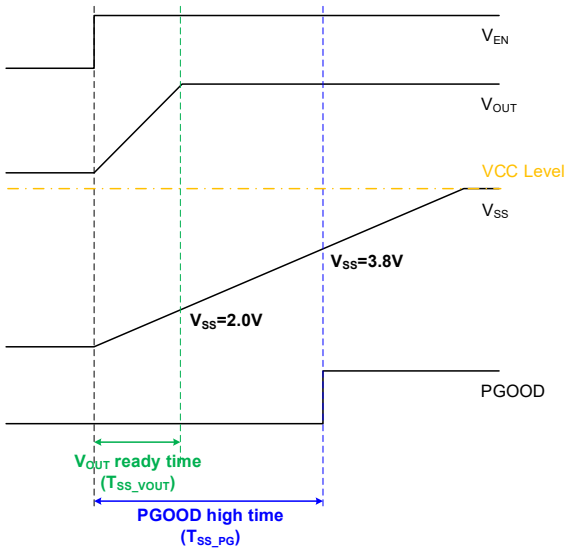


Figure 8. Soft-start Sequence of AOZ21502QI-10

Constant-on-time PWM Control with Input Feed-forward

The control algorithm of AOZ21502QI-10 is constant-on-time control with input feed-forward. The simplified control schematic is shown in Figure 9. The high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage (IN). The one-shot is triggered when the internal 2V is higher than the combined information of FB voltage and the AC current information of inductor, which is processed and obtained through the sensed low-side MOSFET current once it turns on. The added AC current information can help the stability of constant-on time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other V^2 constant-on time control schemes.

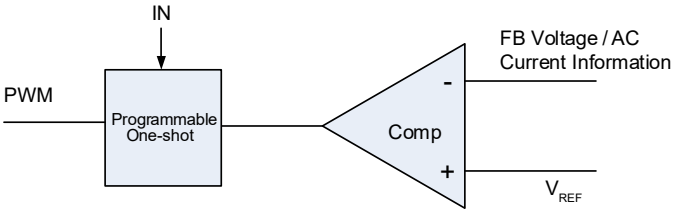


Figure 9. Simplified Control Schematic of AOZ21502QI-10

True Current Mode Control

The constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually cannot be used as output capacitor. The AOZ21502QI-10 senses the low-side MOSFET current and processes it into DC current and AC current information using AOS proprietary technique. The AC current information is decoded and added on the FB pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's ESR; and thus the pure ceramic capacitor solution can be applicant. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

Pulse-frequency Modulation Mode (PFM Mode)

If the MODE is set to PFM mode, the low-side MOSFET turns-off while inductor current valley reaches zero current. Without low-side MOSFET discharging path, the output voltage is naturally discharged by loading current. Until VFB drops to lower than VREF, the controller initiates next cycle again. As a result, the switching frequency is decreased along with loading current decreased. This brings a benefit of higher efficiency but also causes a higher output ripple. Figure 10 shows the inductor current waveform of PFM mode.

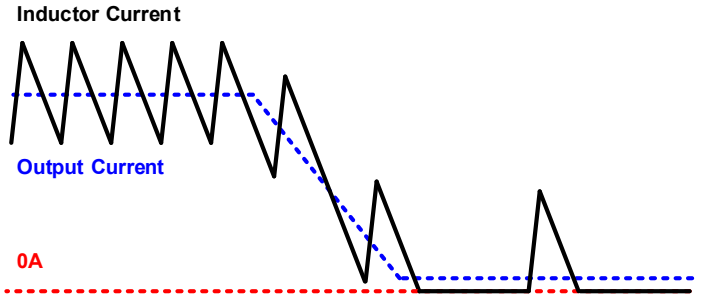


Figure 10. Inductor Current of PFM Mode

Ultrasonic Mode (USM)

If the MODE is set to ultrasonic mode, the light-load behavior is same with PFM mode but an internal clock is added into control loop to limit the minimum switching frequency of AOZ21502QI-10. Once the switching period is detected over than 20µs, the low-side MOSFET is turned-on until feedback voltage drops to reference. With the mechanism, the switching frequency can be well remained above human audible range (20Hz~20kHz) even loading current drops to zero. Figure 11 shows the inductor current waveform of ultrasonic mode.

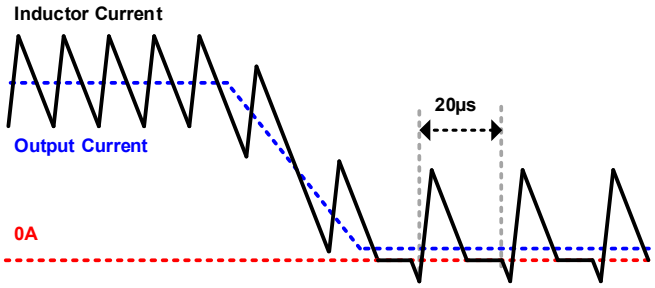


Figure 11. Inductor Current of Ultrasonic Mode

Forced Pulse-width Modulation Mode (FPWM Mode)

If the MODE is set to forced PWM mode, the switching frequency will be approximately a constant. In this mode, the switching loss is obvious but the output ripple can be very small in light-load. Figure 12 shows the inductor current waveform of FPWM mode.

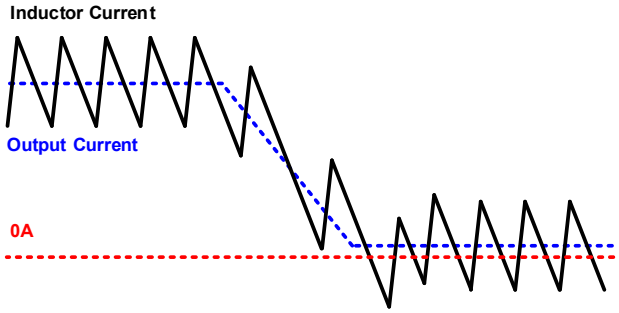


Figure 12. Inductor Current of FPWM Mode

Constant On-time Modulations

In order to adaptively work with a wide operating range, various on-time modulations are adopted to perform a suitable on-time for different input voltage, output current conditions, and operating modes.

Table 2 shows the on-time modulations corresponding to different operating mode for AOZ21502QI-10.

Table 2. On-time Modulations

Modulation	USM	PFM	FPWM
Normal TON	✓	✓	✓
Output Voltage Ripple Reduction	✓		
Ultrasonic Mode On-time Extension	✓		
Low VIN On-time Modulation	✓		
Constant Inductor Current Ripple On-time Modulation		✓	✓

The behaviors of each on-time modulation are described in following:

Normal TON

The constant-on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. The internal circuit of AOZ21502QI-10 sets the on-time of high-side switch inversely proportional to the IN. An external resistor between the IN and TON pin sets the normal on-time according to the following equation:

$$T_{ON\_NOR}(ns) = \frac{R_{TON}(k\Omega)}{V_{IN} - 0.5} \times 21.5$$

The normal TON is active for all operating modes.

Output Voltage Ripple Reduction

When operating in ultrasonic mode or PFM mode, the switching frequency will go down along with output current decreases. If the switching frequency is down to 50% of the original setting, AOZ21502QI-10 actively decreases on-time pulse width to reduce inductor current ripple and output voltage ripple. On-time pulse width can shrink to 70% of original after this mechanism executes 3 times at most.

Ultrasonic Mode On-time Extension

In ultrasonic mode, an on-time extension is added to the normal T_{ON} for stability consideration. The summation of the on-time in ultrasonic mode can be calculated by below equation:

$$T_{ON\_USM}(ns) = 1.33 \times \left(\frac{V_{OUT}}{V_{IN} - V_{OUT}}\right) \times T_{OFF\_MIN}(ns) + T_{ON\_NOR}(ns)$$

Figure 13 illustrates the waveform of one ultrasonic mode switching cycle:

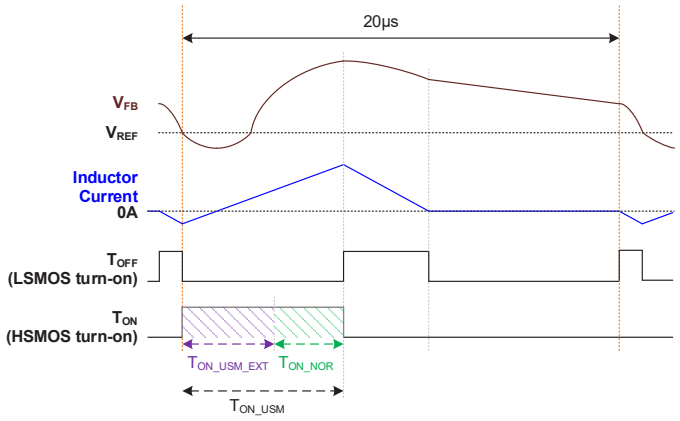


Figure 13. Ultrasonic Mode Switching Cycle

The ultrasonic mode on-time extension is only active when MODE is set to ultrasonic mode and operating in light-load.

Low VIN On-time Modulation

When input voltage goes low to be very closed to target output voltage, the on-time have to be extended because T_{OFF_MIN} limitation will make output voltage drop. The low VIN on-time modulation is used to solve this problem. It is independent from other on-time modulations, and can be estimated by following equation:

$$T_{ON\_LVIN}(ns) = \left(\frac{V_{OUT}}{V_{IN} - V_{OUT}}\right) \times T_{OFF\_MIN}(ns)$$

The T_{ON_LVIN} becomes longer when (V_{IN}-V_{OUT}) goes low. If T_{ON_LVIN} is longer than other on-time modulations, the final on-time will be dominated by T_{ON_LVIN}, the on-time will be further extended. It can effectively prevent the output voltage drop and won't influence the original on-time of high VIN conditions. The low VIN on-time modulation is only active when MODE is set to ultrasonic mode.

The major difference between low VIN on-time extension and ultrasonic mode extension is the former is active even operating in heavy-load.

Constant Inductor Current Ripple On-time Modulation

When MODE is set to PFM or FPWM mode, the constant inductor current ripple on-time modulation is active. This function is used to extend on-time for improving stability and load regulation. The concept of this modulation is illustrated as below:

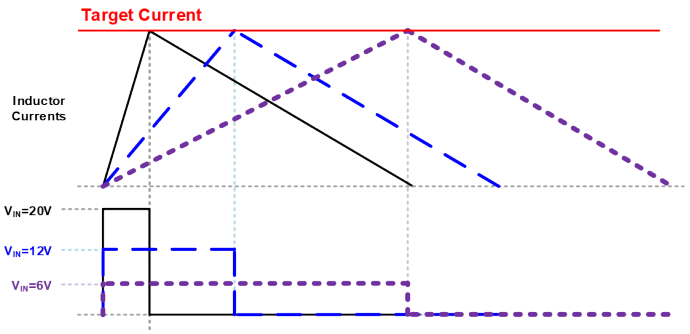


Figure 14. Constant Inductor Current Ripple On-time Modulation

The extended on-time of this function can be calculated by following equation:

$$T_{ON\_ILR}(ns) = \frac{7000}{(V_{IN} - 10)}$$

The target inductor current will be:

$$I_{L\_const}(A) = \frac{(V_{IN} - V_{OUT})}{L} \times T_{ON\_ILR}$$

For V_{OUT}=10V, the inductor current is constant. Only if T_{ON_ILR} is longer than other on-time modulations, the final on-time will be dominated by T_{ON_ILR}. A second maximum on-time limit ($T_{ON\_MAX\_2}$) is used to limit the on-time at extreme low input voltage to prevent output ripple becomes too big when VIN is closed to VOUT.

Switching Frequency

To achieve the flux balance of inductor, the buck converter has the equation:

$$F_{SW} = \frac{V_{OUT}}{V_{IN} \times T_{ON}}$$

It is important to note that the TON would be adjusted by various modulation mechanisms mentioned in previous section. Once the TON is gotten by previous equations, the switching frequency can be estimated by:

$$F_{SW}(kHz) = \frac{V_{OUT}}{V_{IN} * T_{ON}(ns)} \times 10^6$$

Overshoot Improvement (OHI)

The OHI function is used to reduce the overshoot voltage caused by loading current release. When output voltage rises to over OHI threshold because of a sudden loading current decreasing, it immediately turn-off low-side MOSFET. Moreover, both high-side and low-side MOSFETs are not allowed to be turned-on until V_{FB} drops to V_{REF}. In this period, the inductor current flows through low-side MOSFET's body diode, the voltage across inductor is added with a body-diode's forward voltage (0.7V), as illustrated in Figure 15. As a result, the inductor current decreasing speed is increased to suppress output voltage overshoot. Figure 16 shows the behavior of overshoot improvement.

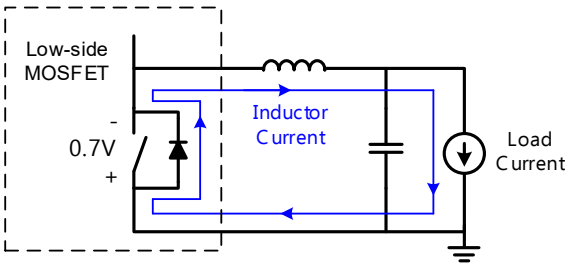


Figure 15. Overshoot Improvement

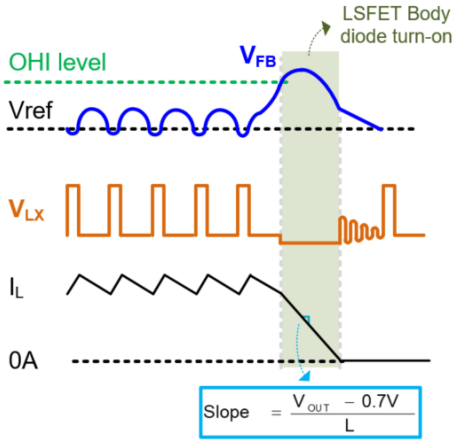


Figure 16. Behavior of Overshoot Improvement

Current-limit Protection

The AOZ21502QI-10 has the current-limit protection by using R_{dson} of the low-side MOSFET to be as current sensing. To detect real current information, a minimum constant off-time (300ns typical) is implemented after a constant on-time. If the current exceeds the current-limit threshold, the controller is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input and output voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit.

After 16 switching cycles, the AOZ21502QI-10 considers this is a true failed condition and thus turns-off both high-side and low-side MOSFET and shuts down. The AOZ21502QI-10 enters hiccup mode to periodically restart the part. When the current limit protection is removed, the AOZ21502QI-10 exits hiccup mode.

Output Voltage Under-voltage Protection

If the output voltage is lower than 50% by over-current or short circuit, AOZ21502QI-10 will turn off both high-side and low-side MOSFET and shut down. When the output voltage under-voltage protection is removed, the AOZ21502QI-10 restarts again.

Output voltage Over-voltage Protection

The threshold of OVP is set 20% higher than 2V. When the VFB voltage exceeds the OVP threshold, high-side MOSFET is turned-off and low-side MOSFETs is turned-on 1µs, then shuts down. When the output voltage over-voltage protection is removed, the AOZ21502QI-10 restarts again.

Power Good Output

The power good (PGOOD) output, which is an open drain output, requires the pull-up resistor. When the output voltage is 10% below than the nominal regulation voltage for, the PGOOD is pulled low. When the output voltage is 20% higher than the nominal regulation voltage, the PGOOD is also pulled low. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance

Application Information

The basic AOZ21502QI-10 application circuit is shown in the Typical Application section. Component selection is explained below.

Input Capacitor

The input capacitor must be connected to the IN pins and PGND pin of the AOZ21502QI-10 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 4.7µF, should be connected to the VCC pin and AGND pin for stable operation of the AOZ21502QI-10. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{V_{OUT}}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

if let *m* equal the conversion ratio:

$$\frac{V_{OUT}}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure. 18. It can be seen that when V_{OUT} is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_{OUT}$.

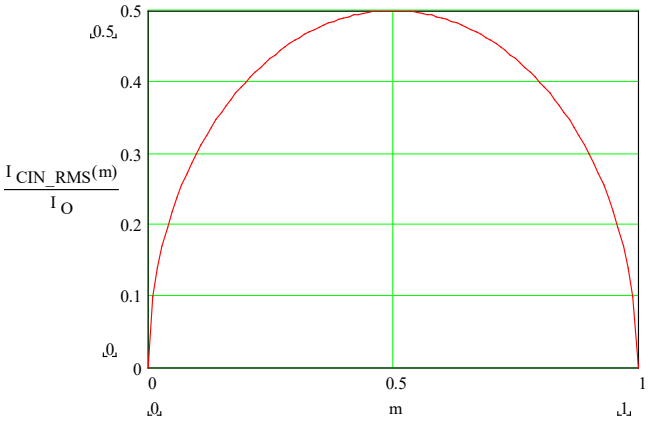


Figure 17. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than $I_{CIN-RMS}$ at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_{OUT} + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR_{C_o} + \frac{1}{8 \times F_{SW} \times C_o} \right)$$

where C_O is output capacitor value and ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_{OUT} = \Delta I_L \times \frac{1}{8 \times F_{SW} \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_{OUT} = \Delta I_L \times ESR_{C_o}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Thermal Management and Layout Consideration

In the AOZ21502QI-10 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the IN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ21502QI-10.

In the AOZ21502QI-10 buck regulator circuit, the major power dissipating components are the AOZ21502QI-10 and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \cdot I_{IN} - V_{OUT} \cdot I_{OUT}$$

The power dissipation of inductor can be approximately calculated by DCR of inductor and output current.

$$P_{inductor\_loss} = I_{OUT}^2 \cdot R_{inductor} \cdot 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ21502QI-10 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \cdot \theta_{JA} + T_A$$

The maximum junction temperature of AOZ21502QI-10 is 150ºC, which limits the maximum load current capability.

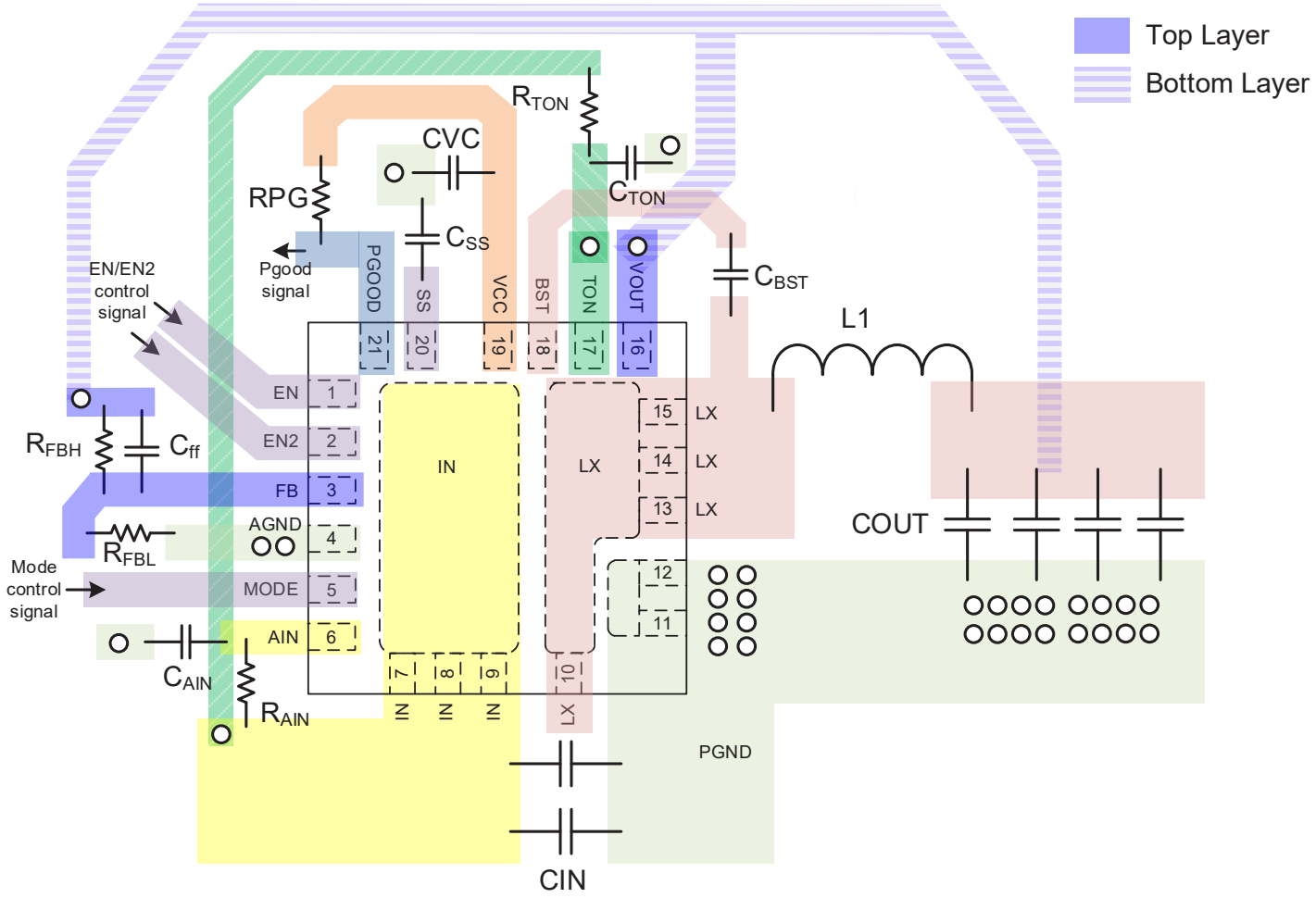
When AOZ21502QI-10 operates at the ambient temperature -40°C condition, the external components must cover the -40°C temperature condition. For example: the capacitor must use X-series type components to cover -40°C temperature condition, which can avoid the system unstable by capacitance reduction.

The thermal performance of the AOZ21502QI-10 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

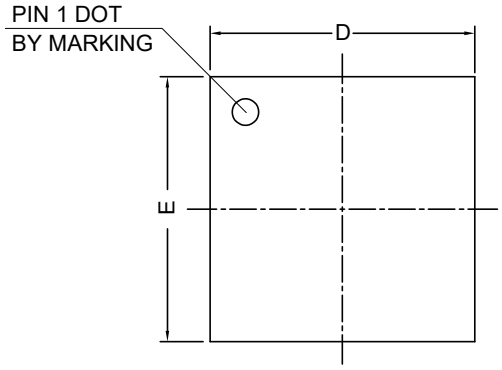
Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

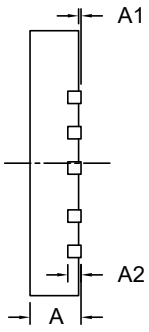
1. Several layout tips are listed below for the best electric and thermal performance.
2. Connected a small copper plane to LX pin to have lower noise interference area.
3. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to IN pins to help thermal dissipation.
4. Input capacitors should be connected to the IN pin and the PGND pin as close as possible to reduce the switching spikes.
5. Decoupling capacitor CVC should be connected to VCC and AGND as close as possible.
6. A large ground plane is preferred.
7. Keep sensitive signal traces such as feedback trace far away from the LX pins. The feedback trace is recommended to be placed at a different layer to LX pad and have a GND layer to separate them.
8. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
9. Place via to connect AGND pin and ground layer, the via must be placed as close as possible to AGND pin. Place via as close as possible to PGND pins and the ground side of output capacitor, too.



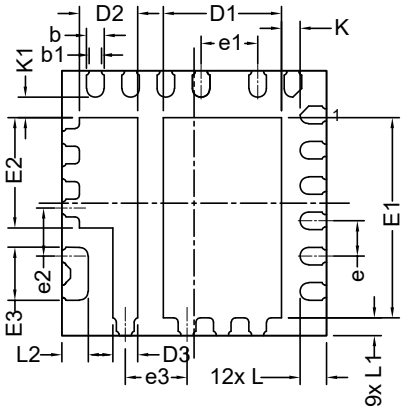
Package Dimensions, QFN3x3-21L



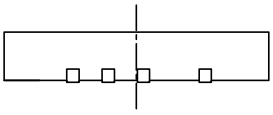
TOP VIEW



SIDE VIEW

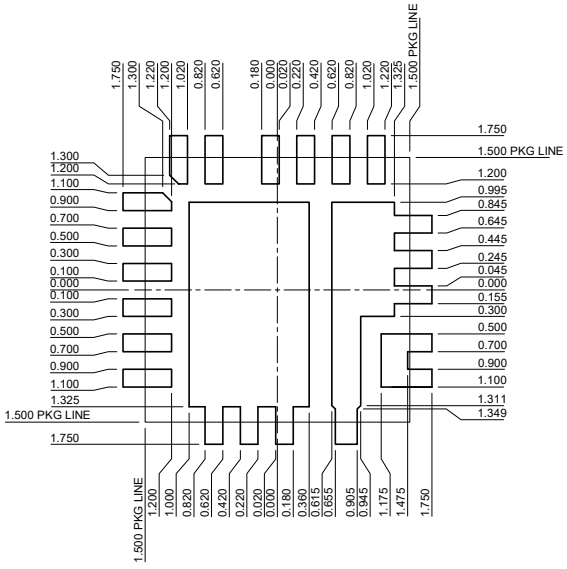


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



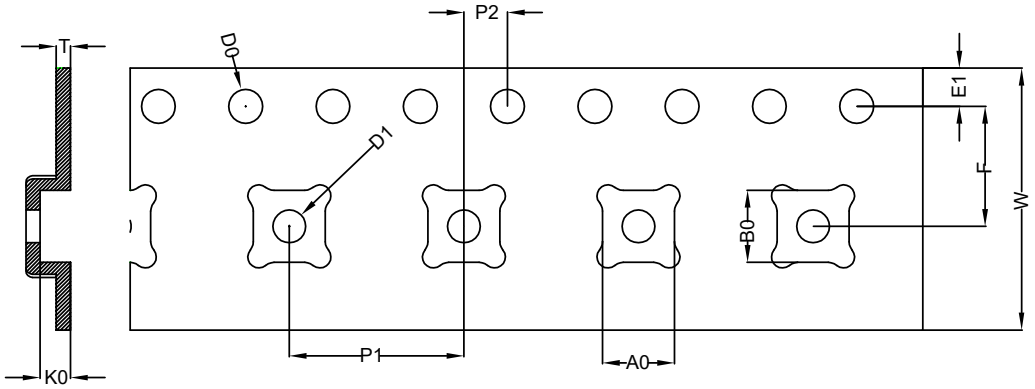
SYMBOLS	DIM. IN MM			DIM. IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	---	0.05	0.000	---	0.002
A2	0.152 REF.			0.006 REF.		
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	1.24	1.34	1.44	0.049	0.053	0.057
D2	0.56	0.66	0.76	0.022	0.026	0.030
D3	0.18	0.28	0.38	0.007	0.011	0.015
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	2.17	2.27	2.37	0.085	0.089	0.093
E2	1.15	1.25	1.35	0.045	0.049	0.053
E3	0.50	0.60	0.70	0.020	0.024	0.028
L	0.25	0.30	0.35	0.010	0.012	0.014
L1	0.15	0.20	0.25	0.006	0.008	0.010
L2	0.25	0.30	0.35	0.010	0.012	0.014
K	0.21 REF.			0.008 REF.		
K1	0.23 REF.			0.009 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
b1	0.09	0.14	0.19	0.004	0.006	0.007
e	0.40 BSC			0.016 BSC		
e1	0.64 BSC			0.025 BSC		
e2	0.545 BSC			0.021 BSC		
e3	0.70 BSC			0.028 BSC		

Note:

1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN3x3-21L

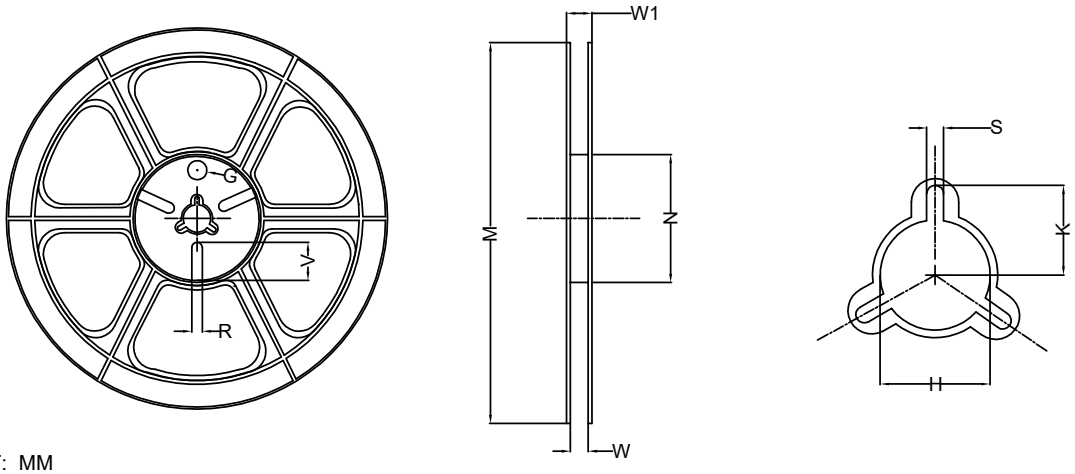
QFN3 x3_18L_EP2_S /QFN3x3_21L_EP2_S Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E1	F	P0	P1	P2	T
QFN3X3_18L_EP2_S QFN3X3_21L_EP2_S	3.30 ±0.10	3.30 ±0.10	0.80 ±0.10	1.55 ±0.05	1.50 Min.	12.00 +0.30 -0.00	1.75 ±0.10	5.50 ±0.10	4.00 ±0.10	8.00 ±0.10	2.00 ±0.10	0.30 ±0.05

QFN3 x3_18L_EP2_S /QFN3x3_21L_EP2_S Reel



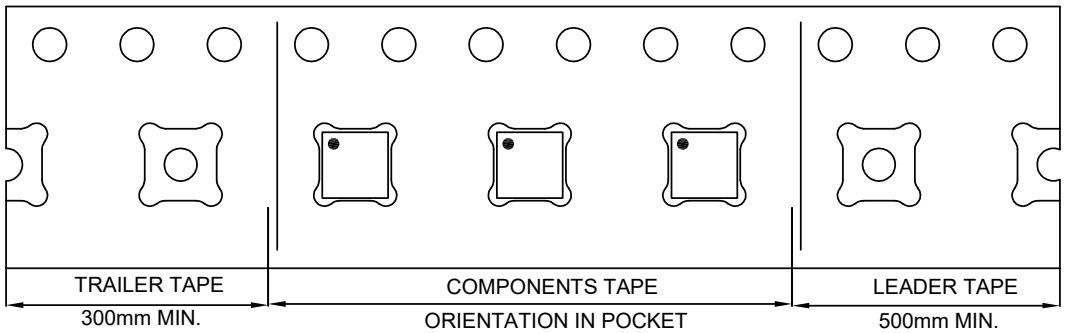
UNIT: MM

TAPESIZE	REEL SIZE	M	N	W	W1	H	S	K	G	R	V
12 mm	Ø330	Ø330.00 ±2.00	Ø101.6 ±2.00	12.40 +2.00 -0.00	12.40 +3.00 -0.20	Ø13.20 ±0.30	1.70-2.60	---	---	---	---

QFN3x3_18L_EP2_S
QFN3x3_21L_EP2_S Tape

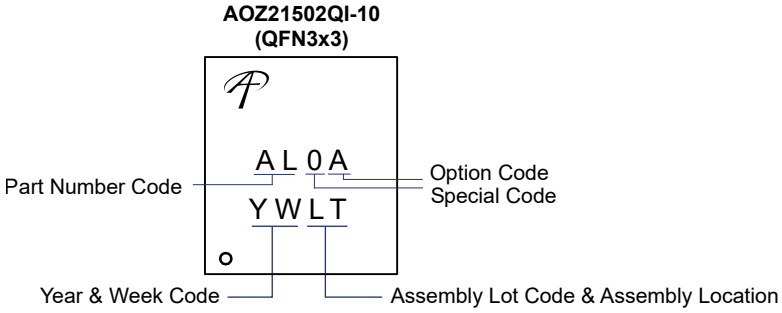
Leader / Trailer
& Orientation

Unit Per Reel:
5000pcs



All Dimensions Comply with EAI-481

Part Marking



LEGAL DISCLAIMER

Applications or uses as critical components in life support devices or systems are not authorized. Alpha and Omega Semiconductor does not assume any liability arising out of such applications or uses of its products. AOS reserves the right to make changes to product specifications without notice. It is the responsibility of the customer to evaluate suitability of the product for their intended application. Customer shall comply with applicable legal requirements, including all applicable export control rules, regulations and limitations.

AOS's products are provided subject to AOS's terms and conditions of sale which are set forth at:
http://www.aosmd.com/terms_and_conditions_of_sale

LIFE SUPPORT POLICY

ALPHA AND OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.