

General Description

The AOZ2232CQI-02 is an I²C controllable, high efficiency, easy-to-use DC-DC synchronous buck regulator capable of operation from a 6.5V to 28V input bus. Ability to control the output voltage using the I²C bus simplifies converter design for microprocessors or SoCs that require dynamic voltage scaling or voltage margining. The device is capable of supplying 6A of continuous output current with an output voltage adjustable from 1.790625V to 0.6V ($\pm 2.0\%$).

The AOZ2232CQI-02 integrates an internal linear regulator to generate 5.3V V_{CC} from input. If input voltage is lower than 5.3V, the linear regulator operates at low drop output mode, which allows the V_{CC} voltage is equal to input voltage minus the drop-output voltage of the internal linear regulator.

A proprietary constant on-time PWM control with input feed-forward results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range.

The devices feature multiple protection functions such as V_{CC} under-voltage lockout, cycle-by-cycle current limit, output over-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ2232CQI-02 is available in a 4mm×4mm QFN-22L package and is rated over a -40°C to +85°C ambient temperature range.

Features

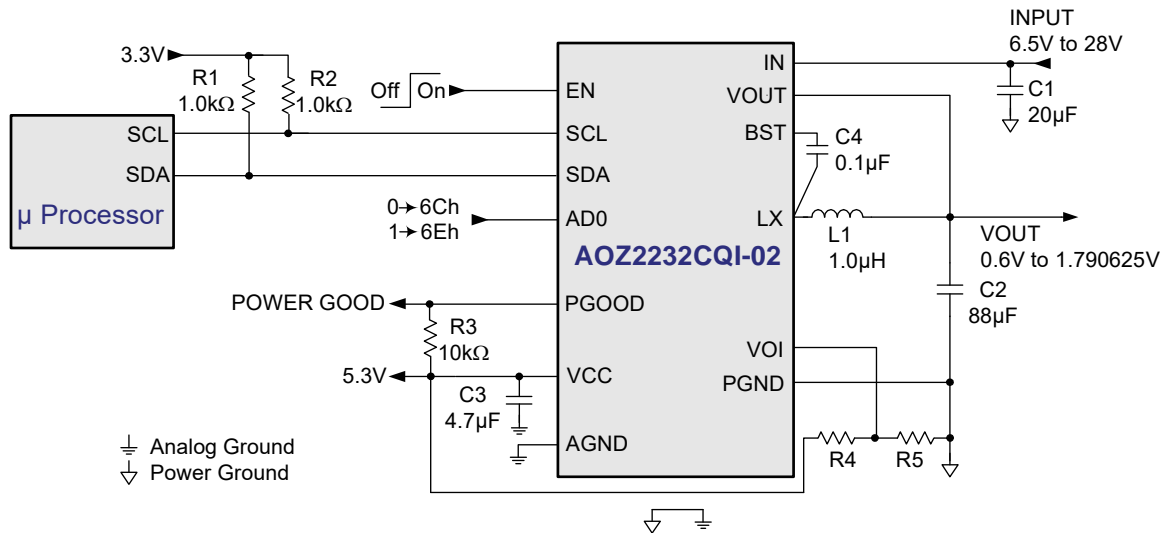
- Wide input voltage range
 - 6.5V to 28V
- 6A continuous output current
- Output voltage adjustable from 0.6V to 1.790625V in 9.375mV
- $\pm 2.0\%$ output voltage accuracy for I²C control
- Low R_{DS(ON)} internal NFETs
 - 28m Ω high-side
 - 11m Ω low-side
- Constant On-Time with input feed-forward
- Selectable PFM Light-Load Operation
- Ceramic capacitor stable
- Power Good output
- I²C address programming
- Integrated bootstrap diode
- Cycle-by-cycle current limit
- Short-circuit protection
- Over voltage protection
- Thermal shutdown
- Thermally enhanced 4mm x 4mm QFN-22L package

Applications

- Portable computers
- Compact desktop PCs
- Servers
- Graphics cards
- Set-top boxes
- LCD TVs
- Cable modems
- Point-of-load DC/DC converters
- Telecom/Networking/Datacom equipment



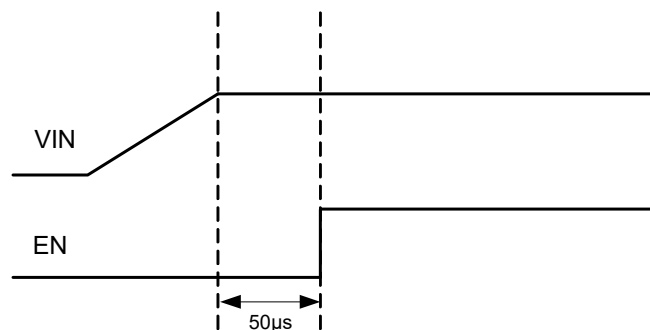
Typical Application



Option Table

| Code \ Item | AD0 | Address (Binary) | Address (Hex) |
|---------------|------------|------------------|---------------|
| AOZ2232CQI-01 | Ground (0) | 01101000 | 68h |
| | Open (1) | 01101010 | 6Ah |
| AOZ2232CQI-02 | Ground (0) | 01101100 | 6Ch |
| | Open (1) | 01101110 | 6Eh |

Recommended Start-up Sequence



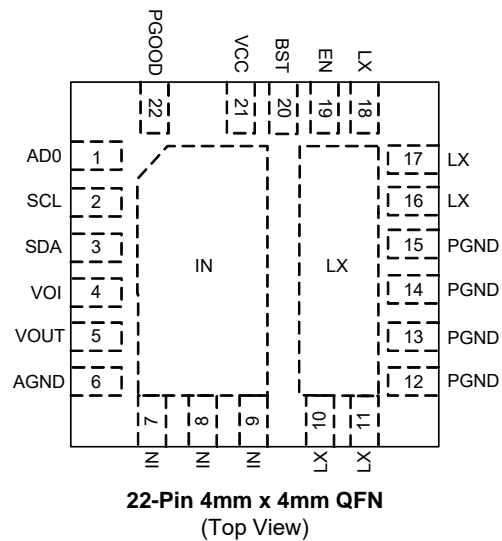
Ordering Information

| Part Number | Ambient Temperature Range | Package | Environmental |
|---------------|---------------------------|----------------------|---------------|
| AOZ2232CQI-02 | -40°C to +85°C | 22-Pin 4mm x 4mm QFN | Green Product |



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant. Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Function |
|--------------------|----------|---|
| 1 | AD0 | Chip Address. The AD0 pin just connects to AOZ2232CQI-02 VCC pin or GND. |
| 2 | SCL | Clock I/O Terminal. |
| 3 | SDA | Data I/O Terminal. |
| 4 | VOI | Initial Output Voltage Feedback Input. Adjust the output voltage with a resistive voltage-divider between VCC and AGND. |
| 5 | VOUT | Output Voltage Feedback Input. Connection to output voltage. |
| 6 | AGND | Analog Ground. |
| 7, 8, 9 | IN | Supply Input. IN is the regulator input. All IN pins must be connected together. |
| 10, 11, 16, 17, 18 | LX | Switching Node. |
| 12, 13, 14, 15 | PGND | Power Ground. |
| 19 | EN | Enable Input. The AOZ2232CQI-02 is enabled when EN is pulled high. The device shuts down when EN is pulled low. |
| 20 | BST | Bootstrap Capacitor Connection. The AOZ2232CQI-02 includes an internal bootstrap diode. Connect an external capacitor between BST and LX as shown in Typical Application diagram. |
| 21 | VCC | Supply Input for Analog Functions. Bypass VCC to AGND with a 1 μ F~4.7 μ F ceramic capacitor. Place the capacitor close to VCC pin. |
| 22 | PGOOD | Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 15% lower than the nominal regulation voltage or 20% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down. |

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

| Parameter | Rating |
|--|-----------------|
| IN to AGND | -0.3V to 30V |
| LX to AGND ⁽¹⁾ | -0.3V to 30V |
| BST to AGND | -0.3V to 36V |
| PGOOD, EN, VCC, SCL, SDA, VOUT, VOI, AD0 to AGND | -0.3V to 6V |
| PGND to AGND | -0.3V to +0.3V |
| Junction Temperature (T _J) | +150°C |
| Storage Temperature (T _S) | -65°C to +150°C |
| ESD Rating ⁽²⁾ | 2kV |

Notes:

1. LX to PGND Transient (t<20ns) ----- -7V to V_{IN}+7V.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating ratings.

| Parameter | Rating |
|--|--------------------|
| Supply Voltage (V _{IN}) | 6.5V to 28V |
| Output Voltage Range | 0.6 V to 1.790625V |
| Ambient Temperature (T _A) | -40°C to +85°C |
| Package Thermal Resistance (θ _{JA}) (θ _{JC}) | 32°C/W 4°C/W |

Electrical Characteristics

T_A = 25°C, V_{IN}=12V, EN = 5V, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

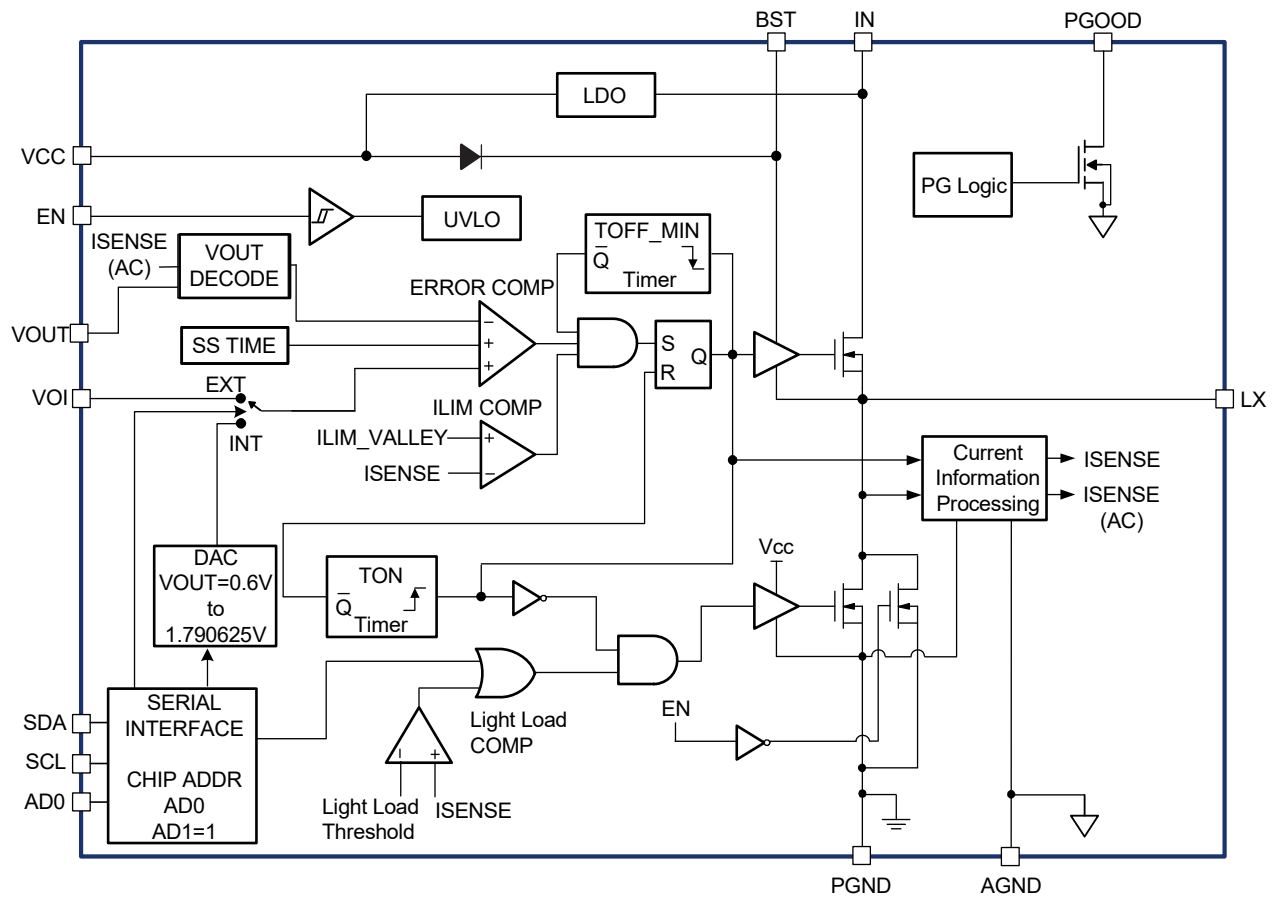
| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|----------------------|--|--|------------|--------------------------|------------|------------------|
| V _{IN} | IN Supply Voltage | | 6.5 | | 28 | V |
| V _{UVLO} | Under-Voltage Lockout Threshold of V _{CC} | V _{CC} rising V _{CC} falling | 3.7 | 4.2 3.9 | 4.4 | V |
| I _q | Quiescent Supply Current of V _{CC} | I _{OUT} = 0, V _{EN} ≥ 2V, PFM mode | | 0.5 | | mA |
| I _{OFF} | Shutdown Supply Current | V _{EN} = 0V | | 1 | 20 | μA |
| V _{OUT} | Output Voltage | T _A = 25°C, V _{IN} =12V V _{OUT} = 0.6 to 1.790625V, L= 1μH | -2% | 0% | 2% | V _{OUT} |
| V _{OUT} | Output Voltage | T _A = 25°C, V _{IN} =12V, V _{OUT} =0.9 to 1.125V, L=1uH | -1.5% | 0% | 1.5% | V _{OUT} |
| T _{r_OUT} | Output Voltage Rising Time | V _{OUT} = 0.9V to 1.3V, C _{OUT} = 88μF, PWM mode | 2.5 | | 15 | μs |
| T _{f_OUT} | Output Voltage Falling Time | V _{OUT} = 1.3V to 0.9V, C _{OUT} = 88μF, PWM mode | 2.5 | | 15 | μs |
| Enable | | | | | | |
| V _{EN} | EN Input Threshold | Off threshold On threshold | 1.4 | | 0.5 | V V |
| V _{EN_HYS} | EN Input Hysteresis | | | 100 | | mV |
| AD0 | | | | | | |
| V _{AD0} | AD0 Input Threshold | Off threshold On threshold | 4.2 | | 0.5 | V V |
| Modulator | | | | | | |
| f _{SW} | Operating Frequency | | | 400 | | kHz |
| T _{ON_MIN} | Minimum On Time | | | 100 | | ns |
| T _{ON_MAX} | Maximum On Time | | | 2.6 | | μs |
| T _{OFF_MIN} | Minimum Off Time | | | 300 | | ns |

Electrical Characteristics

$T_A = 25^\circ\text{C}$, $V_{IN}=12\text{V}$, $V_{EN} = 5\text{V}$, unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to $+85^\circ\text{C}$.

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|--|--|---|------|------------|---------|--------------------------------------|
| Soft-Start | | | | | | |
| T_{SS_OUT} | SS Source Time | for PGOOD pulled High | | 4 | | ms |
| Power Good Signal | | | | | | |
| V_{PG_LOW} | PGOOD Low Voltage | $I_{OL} = 1\text{mA}$ | | | 0.5 | V |
| | PGOOD Leakage Current | | | | ± 1 | μA |
| V_{PGH} | PGOOD Threshold (Low level to High level) | V_{OUT} rising | | 90 | | % |
| V_{PGL} | PGOOD Threshold (High level to Low level) | V_{OUT} rising V_{OUT} falling | | 120 85 | | % % |
| | PGOOD Threshold Hysteresis | | | 5 | | % |
| Under Voltage and Over Voltage Protection | | | | | | |
| V_{PL} | Under Voltage Threshold | V_{OUT} falling | | 70 | | % |
| T_{PL} | Under Voltage Delay Time | | | 32 | | μs |
| V_{PH} | Over Voltage Threshold | V_{OUT} rising | | 120 | | % |
| Power Stage Output | | | | | | |
| $R_{DS(ON)}$ | High-Side NFET On-Resistance | $V_{IN} = 12\text{V}$ | | 28 | | $\text{m}\Omega$ |
| | High-Side NFET Leakage | $V_{EN} = 0\text{V}$, $V_{LX} = 0\text{V}$ | | | 10 | μA |
| $R_{DS(ON)}$ | Low-Side NFET On-Resistance | $V_{LX} = 12\text{V}$ | | 11 | | $\text{m}\Omega$ |
| | Low-Side NFET Leakage | $V_{EN} = 0\text{V}$ | | | 10 | μA |
| V_{CC} Output | | | | | | |
| V_{CC} | V_{CC} output voltage | $V_{IN} \geq 6.5\text{V}$, $I_{CC} = 0\text{mA}$ | 5.09 | 5.3 | 5.51 | V |
| I_{CC} | V_{CC} current limit | $V_{IN} \geq 6.5\text{V}$ | 50 | | | mA |
| Over-current and Thermal Protection | | | | | | |
| I_{LIM} | Current Limit | | 9 | | | A |
| | Thermal Shutdown Threshold | T_J rising T_J falling | | 150 100 | | $^\circ\text{C}$ $^\circ\text{C}$ |

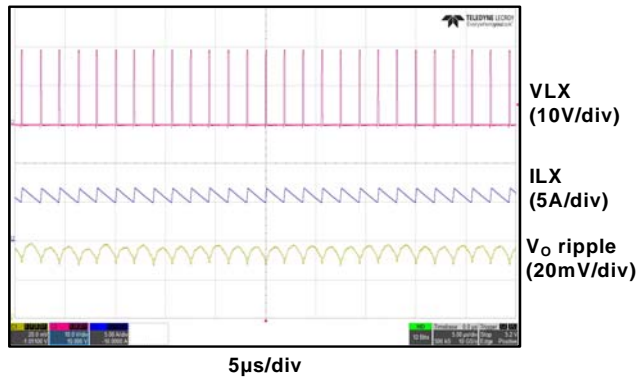
Functional Block Diagram



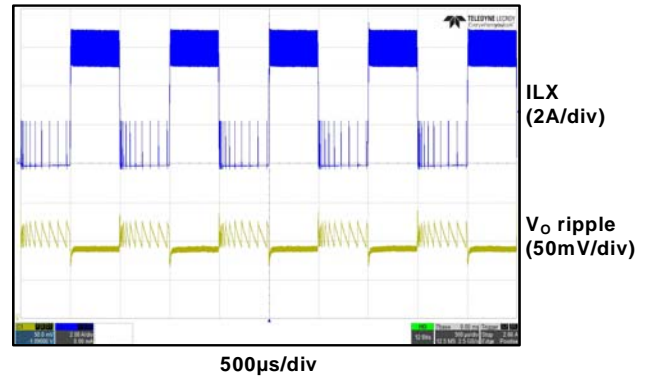
Typical Performance Characteristics

Circuit of Typical Application. $T_A = 25^\circ\text{C}$, $V_{IN} = 19\text{V}$, $V_{OUT} = 1\text{V}$, $f_s = 400\text{kHz}$ unless otherwise specified.

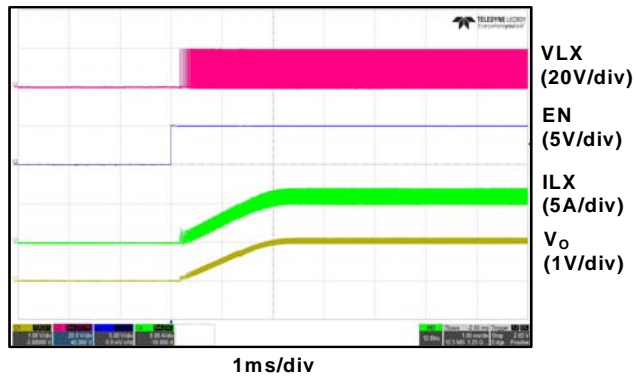
Normal Operation



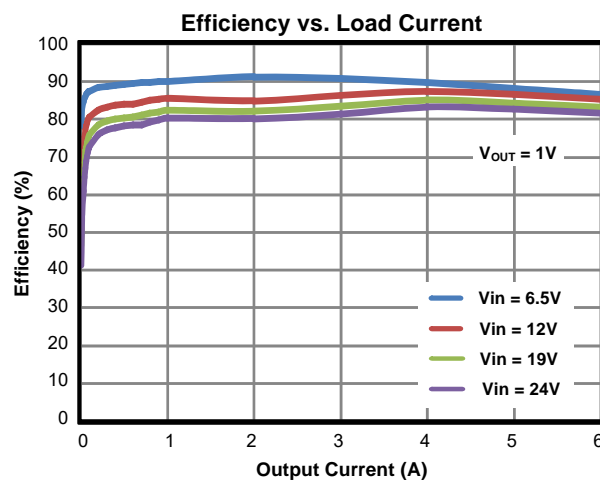
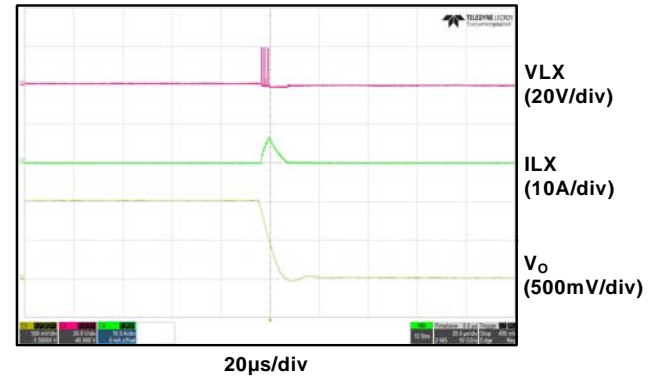
Load Transient 0A to 6A



Full Load Start-up



Short Circuit Protection



I²C Control Specification⁽³⁾⁽⁴⁾⁽⁵⁾

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|---------------------|---|------------|----------------------|------|-----|-------|
| V _{IL} | Low level input voltage | | | | 0.6 | V |
| V _{IH} | High level input voltage | | 2.9 | | | V |
| V _{hys} | Hysteresis of Schmitt trigger inputs | | 0.11 | | | V |
| V _{OL} | Low level output voltage (Open drain, 3mA sink current) | | | | 0.4 | V |
| T _{SP} | Pulse width of spikes suppressed by input filter | | 32 | | | ns |
| f _{SCL} | SCL clock frequency | | | | 400 | kHz |
| t _{HD;STA} | Hold time (repeated), START condition | | 0.6 | | | μs |
| t _{LOW} | Low period of SCL clock | | 1.3 | | | μs |
| t _{HIGH} | High period of SCL clock | | 0.6 | | | μs |
| t _{SU;STA} | Set-up time for a repeated START condition | | 0.6 | | | μs |
| t _{HD;DAT} | Data hold time | | 50 | | 900 | ns |
| t _{SU;DAT} | Data set-up time | | 100 | | | ns |
| t _r | Rise time (SDA or SCL) | | 20+0.1C _b | | 300 | ns |
| t _f | Fall time (SDA or SCL) | | 5+0.1C _b | | 300 | ns |
| t _{SU;STO} | Set-up time for STOP condition | | 0.6 | | | μs |
| t _{BUF} | Bus free time between STOP and START conditions | | 1.3 | | | μs |
| C _b | Capacitive load for each bus line | | | | 400 | pF |
| I _d | SDA driver capability | | 25 | | 100 | mA |

Notes:

3. Ensured by design. Not production tested.
4. Refer to Figure 1 for I²C timing definitions.
5. C_b = capacitance of bus line in pF.

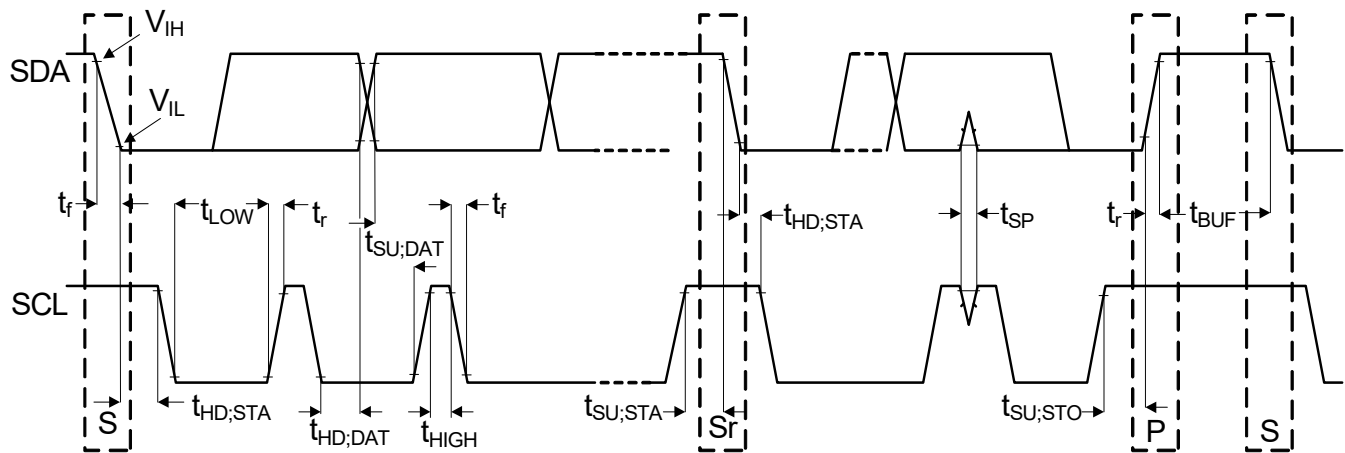


Figure 1. I²C Timing Definitions

I²C Register Maps

| Register Name | Register Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|------------------|---------------|----------------------|-------|-----------------------|-------|-------|-------|-----------------|
| Output Voltage | 00 | Odd Parity | Output Voltage [6:0] | | | | | | |
| Control A | 01 | Internal Mode | | | Output Voltage Change | PFMb | | | Protection Mode |

Summary of Default Control Bits⁽⁶⁾

| Control Bit(s) | Default | Function |
|-----------------------|-------------------|--|
| VOUT [6:0] | 0110010 | VOUT code, 7 bits VOUT [6:0]. Part default to 1.068750V. |
| Internal Mode | 0 (External Mode) | 0 case: External Mode 1 case: Internal Mode (1). If set to 1, the part switches to internal mode and VOUT register value controls output voltage. (2). The part can be set back to external control mode at any time by wiring this bit to 0. |
| Output Voltage Change | 0 | 0 case: Internal protection on 1 case: Internal protection off (1). If set to 0, when VOUT code change, the internal protection isn't turned off. (2). If set to 1, when VOUT code change, the internal protection is turned off to avoid triggering internal protection. |
| PFMb | 1 | Select PFM or PWM at light load. 0 case: PFM 1 case: PWM Part defaults to PWM. |
| Protection Mode | 1 | Select Latch-off or Auto-recovery for protection. 0 case: Auto-recovery mode 1 case: Latch-off mode Part defaults to Latch-off mode. |

Note:

6. When the system satisfies any of the following conditions, the I²C register will be reset to default settings:

- (1) No input voltage
- (2) LDO VCC is less than VCC UVLO falling threshold.
- (3) EN signal is disabled

Odd Parity Bit

The odd parity bit is set by the Master controller to be the exclusive-NOR of the output voltage [6:0] bits. It will be used by the AOZ2232CQI-02 to check that a valid data byte has been received. If odd parity is not equal to the exclusive-NOR of the output voltage [6:0] bits, the

AOZ2232CQI-02 assumes that an error has been occurred during the data transmission, and it will not send an ACK bit, nor will it reset the VOUT to the received code. (or, if the Control register will not reset the register contents as requested). The Master should try again to re-send the data. When reading back the VOUT register, the parity bit is sent back.

I²C Serial Interface Description

The AOZ2232CQI-02 serial data interface works as an I²C slave device. It supports most standard data transfer mode (100kbps) and fast transfer mode (400kbps). The serial interface provides the mean to program a precision resistor DAC to set up a VID output voltage control for the 6A DC/DC converter. A one-byte data is written by the I²C Master to the AOZ2232CQI-02 and stored in a data buffer for the VID. The content of the data buffer can also be read back by the Master.

After I²C is enabled, the AOZ2232CQI-02 starts to check the address code sent by the Master every time a START condition is detected. If a valid address code, AD[6:0], is recognized, it will send out an ACK bit by pulling down on the SDA bus during the clock pulse 9 of the SCL bus. The ACK time of the clock pulse 9 of the SCL bus can be written as below.

$$T_{ACK} = 9 \times \frac{1}{f_{SCL}}$$

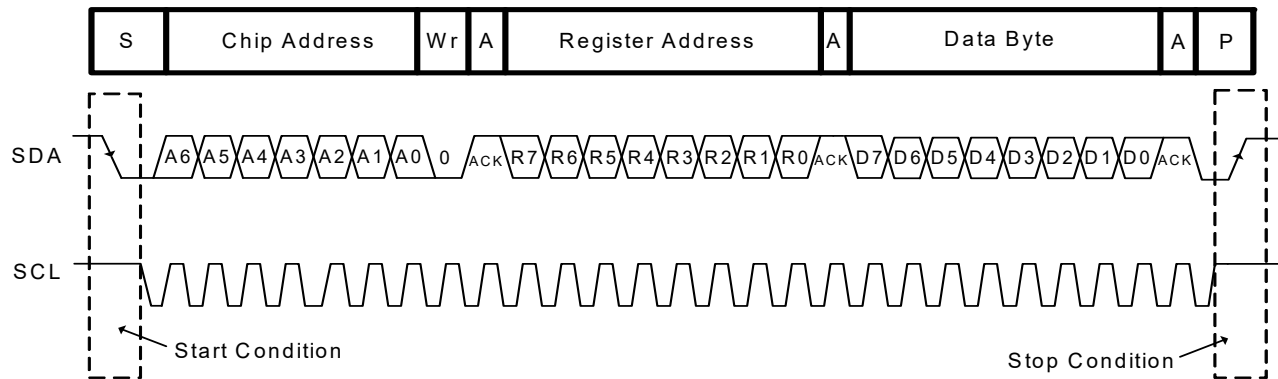


Figure 2. A Complete Write Byte Transfer

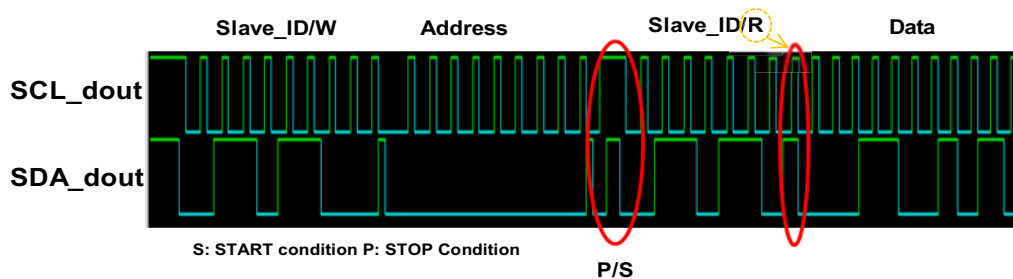


Figure 3. Single Read

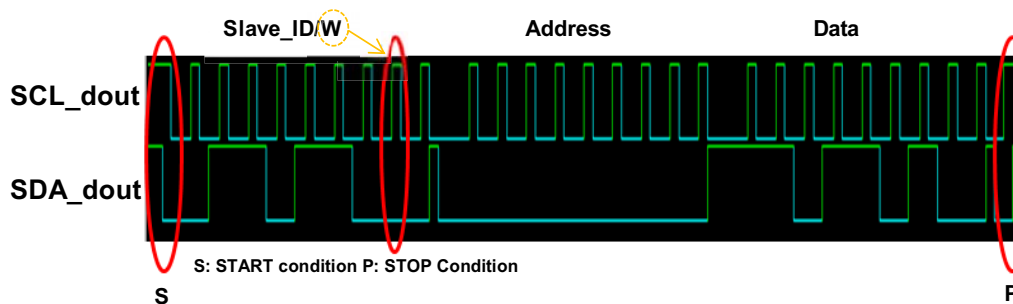


Figure 4. Single Write

If no valid address is detected, no action will be taken and no ACK will be sent. The I²C controller assumes the address is for other I²C device and it will ignore the data bits and resume the search for the next valid address transfer. Finally, the response time from entering command to changing internal function is shown as below:

$$T_R = 27 \times \frac{1}{f_{SCL}}$$

After a valid address code is confirmed, the next bit (Wr) is checked for Write ("0") or Read ("1") mode. If the requested operation is Write mode, the AOZ2232CQI-02 will evaluate the data code, D[7:0], received after the address ACK.

Once the Write data is validated, AOZ2232CQI-02 will send ACK on the SDA bus. The data code will also be transferred to the data holding buffer of the VID and the output voltage will move to the new, or ideal, value. If the data is not valid, no ACK will be sent. It will be up to the I²C Master to repeat the operation.

If the requested operation is Read mode, the AOZ2232CQI-02 will transmit the content of the VID data buffer register, or D[7:0], on the SDA bus. After the 8 data bits are transmitted and STOP detected, the AOZ2232CQI-02 will return to the normal operation regardless of ACK is received or not. It will be up to the I²C Master to re-send a Read request if the last Read operation is deemed invalid.

Detailed Description

The AOZ2232CQI-02 is a high-efficiency, easy-to-use, synchronous buck regulator with a voltage scaling control to power up MCUs requiring core voltage tune-ups. After the initial power up, the output voltage can be programmed/scaled by VID codes sent over an I²C compatible bus. The regulator is capable of supplying 6A of continuous output current with an output voltage adjustable from 0.6V to 1.790625V.

The input voltage of AOZ2232CQI-02 can be as low as 6.5V. The highest input voltage of AOZ2232CQI-02 can be 28V. Constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. True AC current mode control scheme guarantees the regulator can be stable with ceramics output capacitor. Protection features include V_{CC} under-voltage lockout, cycle-by-cycle current limit, output over voltage and under voltage protection, short-circuit protection, and thermal shutdown.

The AOZ2232CQI-02 is available in 22-pin 4mm×4mm QFN package.

Input Power Architecture

The AOZ2232CQI-02 integrates an internal linear regulator to generate 5.3V ($\pm 5\%$) V_{CC} from input. If input voltage is lower than 5.3V, the linear regulator operates at low drop-out mode; the V_{CC} voltage is equal to input voltage minus the drop-output voltage of internal linear regulator.

Enable and Soft Start

The AOZ2232CQI-02 has internal soft start feature to limit in-rush current and ensure the output voltage ramps up smoothly to regulate voltage. A soft start process begins when V_{CC} rises to 4.2V and voltage on EN pin is HIGH. The output voltage follows the internal voltage of soft-start (V_{SS}) when it is lower than initial output voltage. When V_{SS} is higher than initial output voltage, the voltage of VOUT pin is regulated by internal precise band-gap voltage. Moreover, the soft start period between EN and PGOOD is 4ms. The soft start sequence of AOZ2232CQI-02 is shown in Figure 5.

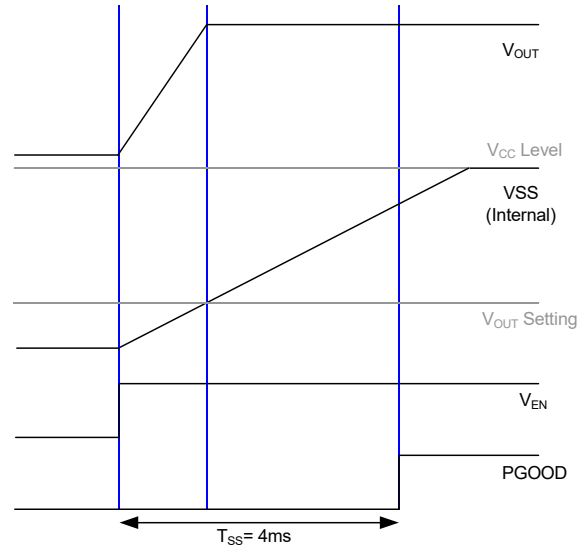


Figure 5. Soft Start Sequence of AOZ2232CQI-02

Enable

The AOZ2232CQI-02 has an embedded discharge path, including a 100k Ω resistor and an M1 NMOS device. This discharge path is activated when V_{IN} (Input Voltage) is high and V_{EN} (Enable Voltage) is low. The internal circuit of EN pin is shown in Figure 6.

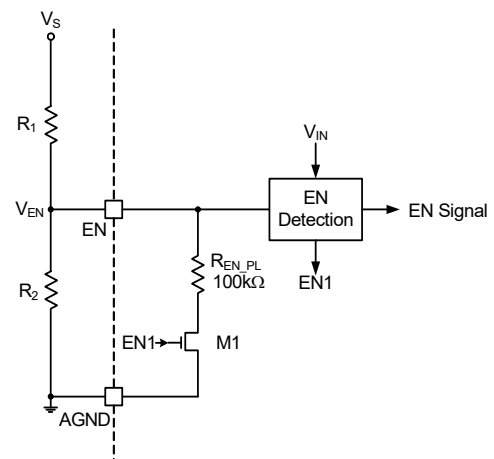


Figure 6. Enable Internal Circuit

There are two different enable control methods:

1. Connection to EN pin by an external resistive voltage divider.
2. Direct connection to EN pin by an external power source, V_S .

In the first condition, we must consider the internal pull-down resistance by using a divider circuit with an external power source V_s to get V_{EN} . The V_{EN} can be calculated by the following formula:

$$V_{EN} = \frac{R_2 // R_{EN_PL}}{R_1 + (R_2 // R_{EN_PL})} \times V_s$$

When the V_{IN} is high and the V_{EN} is high, the EN internal M1 is turned off, and then the pull down resistance is removed for V_{EN} , the V_{EN} can be re-calculated by:

$$V_{EN} = \frac{R_2}{R_1 + R_2} \times V_s$$

In the second condition, the AOZ2232CQI-02 will be turned on when the V_{EN} is higher than 1.4V, and will be turned off when the V_{EN} is lower than 0.5V. The simplified schematic and timing sequence are shown in Figure 7.

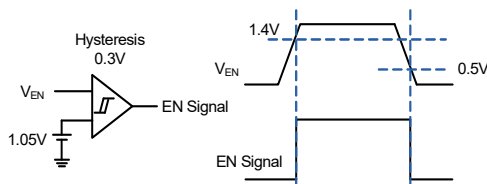


Figure 7. Enable Threshold Schematic and Timing Sequence

Constant-On-Time PWM Control with Input Feed-Forward

The control algorithm of AOZ2232CQI-02 is constant-on-time PWM control with input feed-forward. The simplified control schematic is shown in Figure 8. The high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage (V_{IN}). The one-shot is triggered when the internal VOI/DAC voltage is higher than the combined information of output voltage and the AC current information of inductor, which is processed and obtained through the sensed low-side MOSFET current once it turns-on. The added AC current information can help the stability of constant-on time control even with pure ceramic output capacitors, which have very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other V^2 constant on-time control schemes.

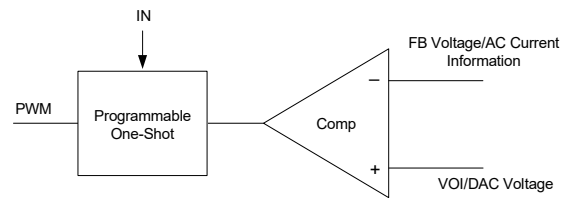


Figure 8. Simplified Control Schematic

True Current Mode Control

The constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually cannot be used as output capacitor.

The AOZ2232CQI-02 senses the low-side MOSFET current and processes it into DC current and AC current information using AOS proprietary technique. The AC current information is decoded and added on the VOUT pin on phase. With AC current information, the stability of constant-on-time control is significantly improved even without the help of output capacitor's ESR; and thus, the pure ceramic capacitor solution can be applicable. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and less board area design.

Current-Limit Protection

The AOZ2232CQI-02 has the current-limit protection by using $R_{DS(ON)}$ of the low-side MOSFET to be as current sensing. To detect real current information, a minimum constant-off time (300ns typical) is implemented after a constant-on time. If the current exceeds the current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input and output voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit.

After 16 switching cycles, the AOZ2232CQI-02 considers this is a true failed condition and thus, turns-off both high-side and low-side MOSFETs and latches off. Only when triggered, the enable can restart the AOZ2232CQI-02 again.

Table 1: Output Voltage Setting vs Register Code

| Code | Binary | VOOUT | Code | Binary | VOUT | Code | Binary | VOUT | Code | Binary | VOUT |
|------|---------|----------|------|---------|----------|------|---------|----------|------|---------|----------|
| 0 | 0000000 | 0.600000 | 32 | 0100000 | 0.900000 | 64 | 1000000 | 1.200000 | 96 | 1100000 | 1.500000 |
| 1 | 0000001 | 0.609375 | 33 | 0100001 | 0.909375 | 65 | 1000001 | 1.209375 | 97 | 1100001 | 1.509375 |
| 2 | 0000010 | 0.618750 | 34 | 0100010 | 0.918750 | 66 | 1000010 | 1.218750 | 98 | 1100010 | 1.518750 |
| 3 | 0000011 | 0.628125 | 35 | 0100011 | 0.928125 | 67 | 1000011 | 1.228125 | 99 | 1100011 | 1.528125 |
| 4 | 0000100 | 0.637500 | 36 | 0100100 | 0.937500 | 68 | 1000100 | 1.237500 | 100 | 1100100 | 1.537500 |
| 5 | 0000101 | 0.646875 | 37 | 0100101 | 0.946875 | 69 | 1000101 | 1.246875 | 101 | 1100101 | 1.546875 |
| 6 | 0000110 | 0.656250 | 38 | 0100110 | 0.956250 | 70 | 1000110 | 1.256250 | 102 | 1100110 | 1.556250 |
| 7 | 0000111 | 0.665625 | 39 | 0100111 | 0.965625 | 71 | 1000111 | 1.265625 | 103 | 1100111 | 1.565625 |
| 8 | 0001000 | 0.675000 | 40 | 0101000 | 0.975000 | 72 | 1001000 | 1.275000 | 104 | 1101000 | 1.575000 |
| 9 | 0001001 | 0.684375 | 41 | 0101001 | 0.984375 | 73 | 1001001 | 1.284375 | 105 | 1101001 | 1.584375 |
| 10 | 0001010 | 0.693750 | 42 | 0101010 | 0.993750 | 74 | 1001010 | 1.293750 | 106 | 1101010 | 1.593750 |
| 11 | 0001011 | 0.703125 | 43 | 0101011 | 1.003125 | 75 | 1001011 | 1.303125 | 107 | 1101011 | 1.603125 |
| 12 | 0001100 | 0.712500 | 44 | 0101100 | 1.012500 | 76 | 1001100 | 1.312500 | 108 | 1101100 | 1.612500 |
| 13 | 0001101 | 0.721875 | 45 | 0101101 | 1.021875 | 77 | 1001101 | 1.321875 | 109 | 1101101 | 1.621875 |
| 14 | 0001110 | 0.731250 | 46 | 0101110 | 1.031250 | 78 | 1001110 | 1.331250 | 110 | 1101110 | 1.631250 |
| 15 | 0001111 | 0.740625 | 47 | 0101111 | 1.040625 | 79 | 1001111 | 1.340625 | 111 | 1101111 | 1.640625 |
| 16 | 0010000 | 0.750000 | 48 | 0110000 | 1.050000 | 80 | 1010000 | 1.350000 | 112 | 1110000 | 1.650000 |
| 17 | 0010001 | 0.759375 | 49 | 0110001 | 1.059375 | 81 | 1010001 | 1.359375 | 113 | 1110001 | 1.659375 |
| 18 | 0010010 | 0.768750 | 50 | 0110010 | 1.068750 | 82 | 1010010 | 1.368750 | 114 | 1110010 | 1.668750 |
| 19 | 0010011 | 0.778125 | 51 | 0110011 | 1.078125 | 83 | 1010011 | 1.378125 | 115 | 1110011 | 1.678125 |
| 20 | 0010100 | 0.787500 | 52 | 0110100 | 1.087500 | 84 | 1010100 | 1.387500 | 116 | 1110100 | 1.687500 |
| 21 | 0010101 | 0.796875 | 53 | 0110101 | 1.096875 | 85 | 1010101 | 1.396875 | 117 | 1110101 | 1.696875 |
| 22 | 0010110 | 0.806250 | 54 | 0110110 | 1.106250 | 86 | 1010110 | 1.406250 | 118 | 1110110 | 1.706250 |
| 23 | 0010111 | 0.815625 | 55 | 0110111 | 1.115625 | 87 | 1010111 | 1.415625 | 119 | 1110111 | 1.715625 |
| 24 | 0011000 | 0.825000 | 56 | 0111000 | 1.125000 | 88 | 1011000 | 1.425000 | 120 | 1111000 | 1.725000 |
| 25 | 0011001 | 0.834375 | 57 | 0111001 | 1.134375 | 89 | 1011001 | 1.434375 | 121 | 1111001 | 1.734375 |
| 26 | 0011010 | 0.843750 | 58 | 0111010 | 1.143750 | 90 | 1011010 | 1.443750 | 122 | 1111010 | 1.743750 |
| 27 | 0011011 | 0.853125 | 59 | 0111011 | 1.153125 | 91 | 1011011 | 1.453125 | 123 | 1111011 | 1.753125 |
| 28 | 0011100 | 0.862500 | 60 | 0111100 | 1.162500 | 92 | 1011100 | 1.462500 | 124 | 1111100 | 1.762500 |
| 29 | 0011101 | 0.871875 | 61 | 0111101 | 1.171875 | 93 | 1011101 | 1.471875 | 125 | 1111101 | 1.771875 |
| 30 | 0011110 | 0.881250 | 62 | 0111110 | 1.181250 | 94 | 1011110 | 1.481250 | 126 | 1111110 | 1.781250 |
| 31 | 0011111 | 0.890625 | 63 | 0111111 | 1.190625 | 95 | 1011111 | 1.490625 | 127 | 1111111 | 1.790625 |

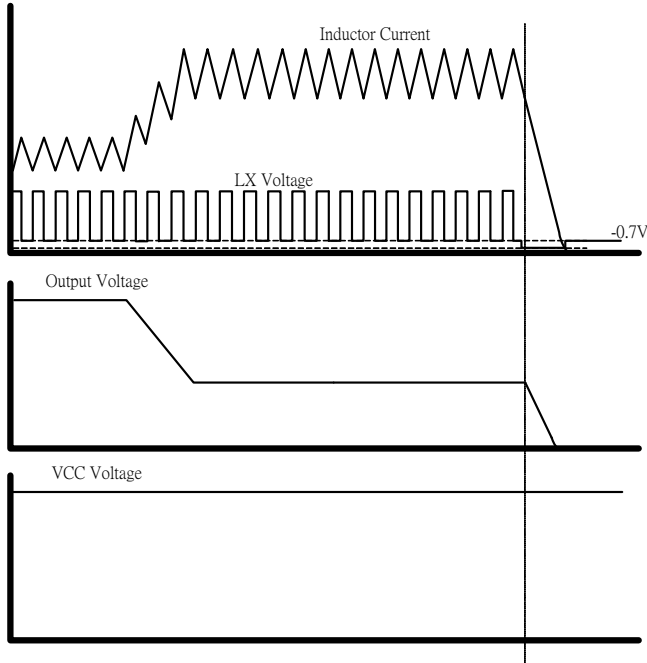


Figure 9. OCP Timing Chart

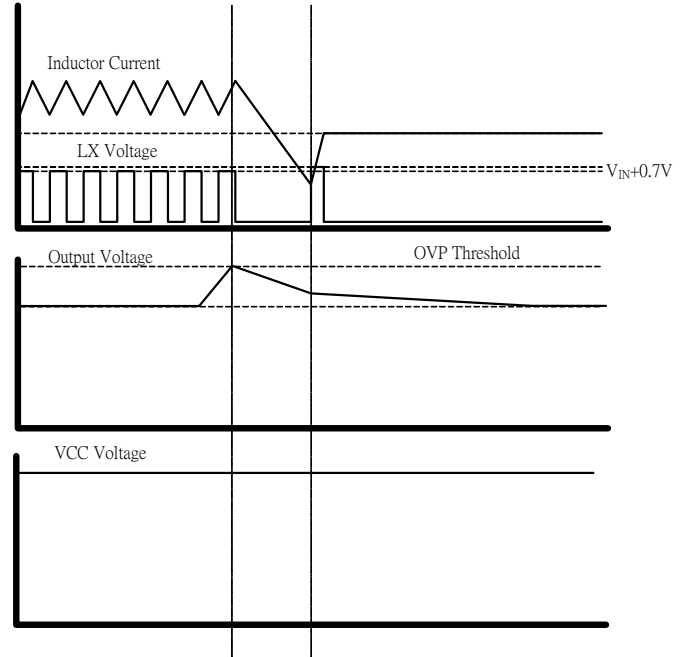


Figure 10. OVP Timing Chart

Output Voltage Under-Voltage Protection

If the output voltage is lower than 70% by over-current or short circuit, AOZ2232CQI-02 will wait for 32us(typical) and turns-off both high-side and low-side MOSFETs and latches off. Only when triggered, the enable can restart the AOZ2232CQI-02 again.

Output Voltage Over-Voltage Protection

The threshold of OVP is set 20% higher than VOI/DAC voltage. When the voltage of VOUT pin exceeds the OVP threshold, high-side MOSFET is turned-off and low-side MOSFETs is turned-on until the voltage of VOUT pin is lower than VOI/DAC voltage.

Output Voltage Registers

The AOZ2232CQI-02 has 7 bits of output voltage register control for output voltage adjusting from 0.6V to 1.790625V. Output Voltage Setting vs Register Code shows the output voltage setting for DAC voltage and register codes. When the AOZ2232CQI-02 powers up, the startup and output voltage regulation conditions are set by the external resistor divider feedback to the VOI pin from VCC voltage. Therefore, the initial output voltage can be calculated by:

$$VOI = \frac{R_5}{R_4 + R_5} \cdot V_{CC}$$

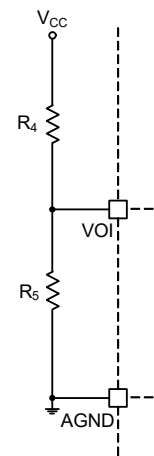


Figure 11. VOI Divided Circuit

Output Voltage Rising and Falling Time

We can adjust AOZ2232CQI-02's output voltage level by the I2C interface. The output voltage rising time and falling time is determined by our internal slew-rate control circuit. Resulted from various output voltage change points, it makes different rising and falling time. If the output voltage starts to change at the peak of output voltage, it takes less time to achieve new output voltage level than from the valley. The difference of their rising time in the same sample is approximately 1/2 of switching cycle time.

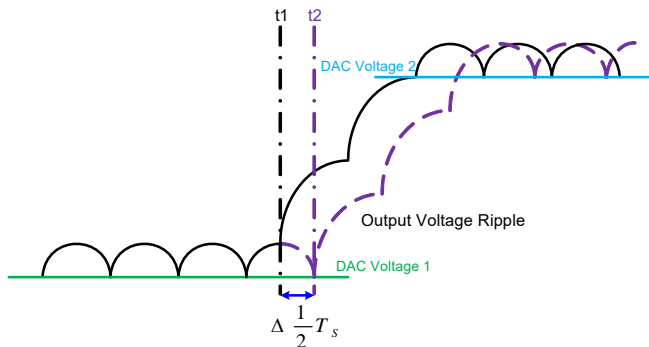


Figure 12. Variations of Output Voltage Rising Time

Application Information

The basic AOZ2232CQI-02 application circuit is shown in Typical Application section. The component selection is explained below.

Input capacitor

The input capacitor must be connected to the IN pins and PGND pin of the AOZ2232CQI-02 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 4.7uF, should be connected to the V_{CC} pin and AGND pin for stable operation of the AOZ2232CQI-02. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}} \left(1 - \frac{V_O}{V_{IN}}\right)}$$

if let m equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relation between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure13. It can be seen that when V_O is half of V_{IN} , C_{IN} is under the worst current stress. The worst current stress on C_{IN} is $0.5 \cdot I_O$.

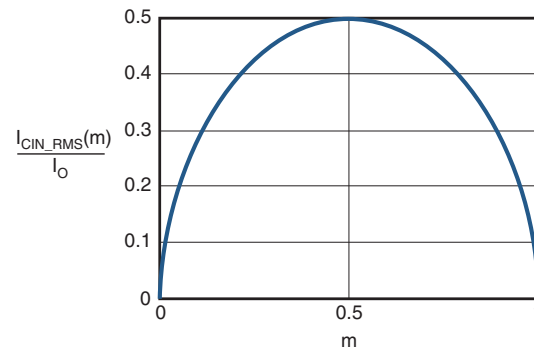


Figure 13. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times (ESR_{CO} + \frac{1}{8 \times f \times C_O})$$

where, C_O is output capacitor value and ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Thermal Management and Layout Consideration

In the AOZ2232CQI-02 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the IN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side switch is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pin of the AOZ2232CQI-02.

In the AOZ2232CQI-02 buck regulator circuit, the major power dissipating components are the AOZ2232CQI-02 and the output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by DCR of inductor and output current.

$$P_{inductor_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ2232CQI-02 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total_loss} - P_{inductor_loss}) \cdot \Theta_{JA} + T_A$$

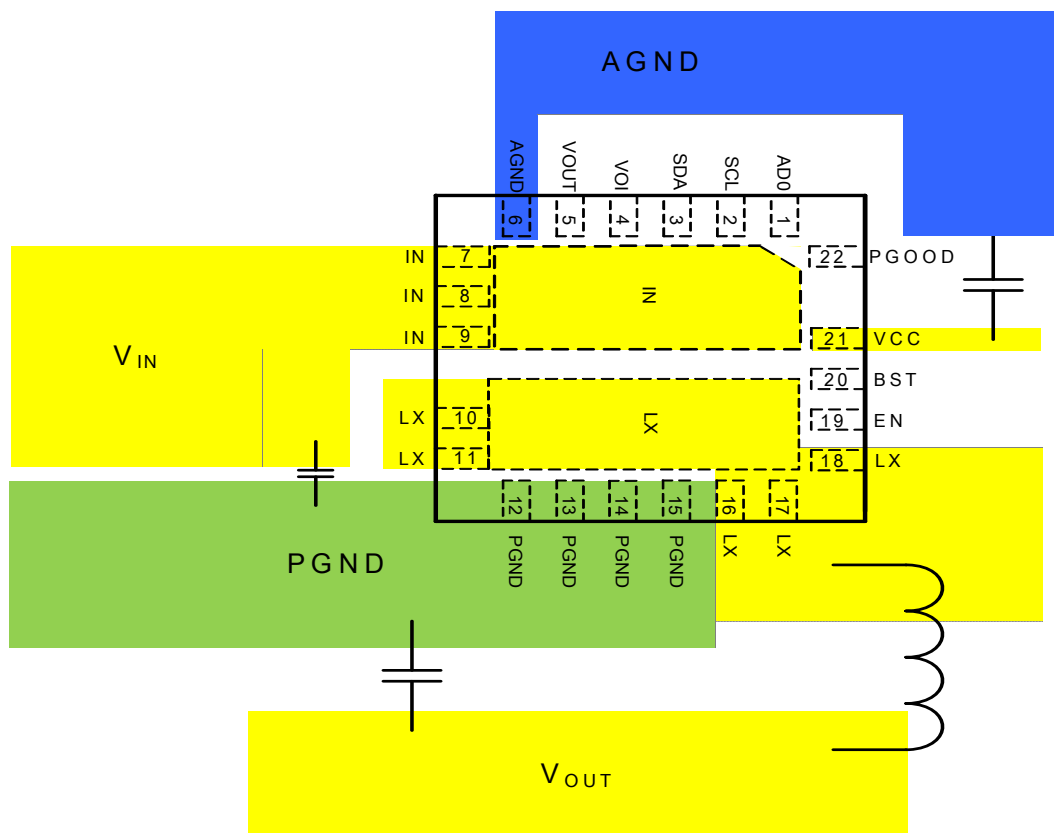
The maximum junction temperature of AOZ2232CQI-02 is 150°C, which limits the maximum load current capability.

The thermal performance of the AOZ2232CQI-02 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

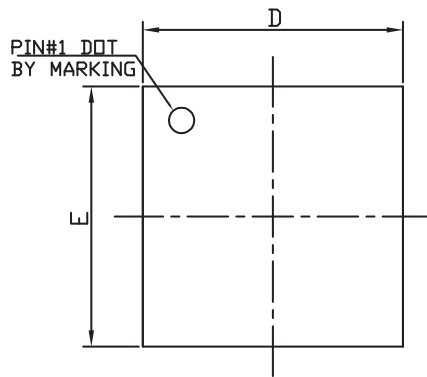
Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

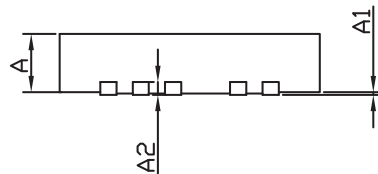
1. Connected a small copper plane to LX pin to have lower noise interference area.
2. The IN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to IN pins to help thermal dissipation.
3. Input capacitors should be connected to the IN pin and the PGND pin as close as possible to reduce the switching spikes.
4. Decoupling capacitor C_{VCC} should be connected to V_{CC} and AGND as close as possible.
5. Keep sensitive signal traces such as output trace far away from the LX pins.
6. Let digital pins such as AD0, SCL and SDA, to use AGND.
7. Let VOI pin to use AGND.
8. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.



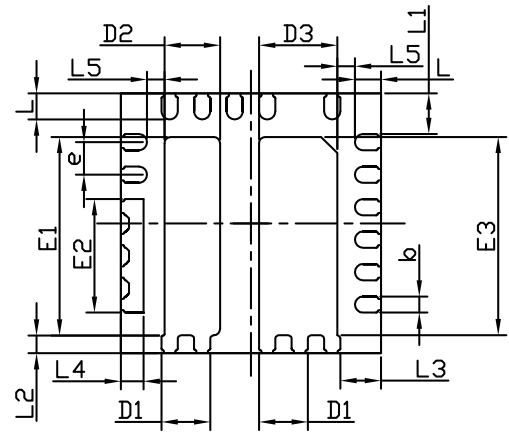
Package Dimensions, QFN4x4-22L, EP2_S



TOP VIEW

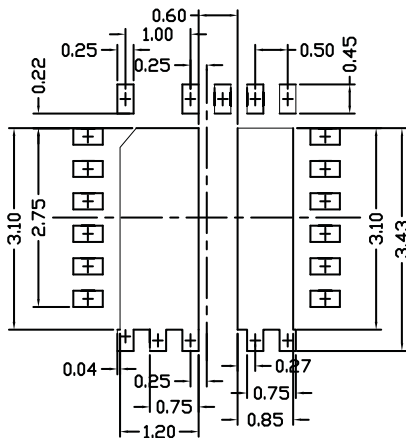


SIDE VIEW



BOTTOM VIEW

RECOMMENDED LAND PATTERN



UNIT: mm

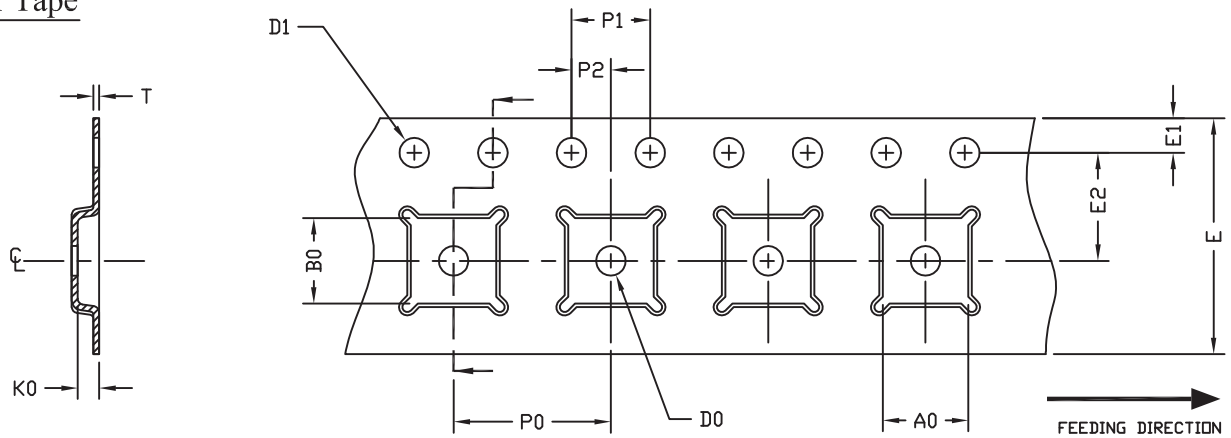
| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---------|---------------------------|------|------|----------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1 | 0.00 | --- | 0.05 | 0.000 | --- | 0.002 |
| A2 | 0.2 REF | | | 0.008 REF | | |
| E | 3.90 | 4.00 | 4.10 | 0.153 | 0.157 | 0.161 |
| E1 | 2.95 | 3.05 | 3.15 | 0.116 | 0.120 | 0.124 |
| E2 | 1.65 | 1.75 | 1.85 | 0.065 | 0.069 | 0.073 |
| E3 | 2.95 | 3.05 | 3.15 | 0.116 | 0.120 | 0.124 |
| D | 3.90 | 4.00 | 4.10 | 0.153 | 0.157 | 0.161 |
| D1 | 0.65 | 0.75 | 0.85 | 0.026 | 0.030 | 0.034 |
| D2 | 0.75 | 0.85 | 0.95 | 0.029 | 0.033 | 0.037 |
| D3 | 1.10 | 1.20 | 1.30 | 0.043 | 0.047 | 0.051 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| L1 | 0.57 | 0.62 | 0.67 | 0.022 | 0.024 | 0.026 |
| L2 | 0.23 | 0.28 | 0.33 | 0.009 | 0.011 | 0.013 |
| L3 | 0.57 | 0.62 | 0.67 | 0.022 | 0.024 | 0.026 |
| L4 | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| L5 | 0.17 | 0.27 | 0.37 | 0.007 | 0.011 | 0.015 |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| e | 0.50 BSC | | | 0.020 BSC | | |

NOTE

1. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. TOLERANCE : 0.05 UNLESS OTHERWISE SPECIFIED.
3. RADIUS ON ALL CORNER ARE 0.152 MAX., UNLESS OTHERWISE SPECIFIED.
4. PACKAGE WARPAGE: 0.012 MAX.
5. NO ANY PLASTIC FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
6. PAD PLANARITY: 0.102
7. CRACK BETWEEN PLASTIC BODY AND LEAD IS NOT ALLOWED.

Tape and Reel Dimensions, QFN4x4-22L, EP2_S

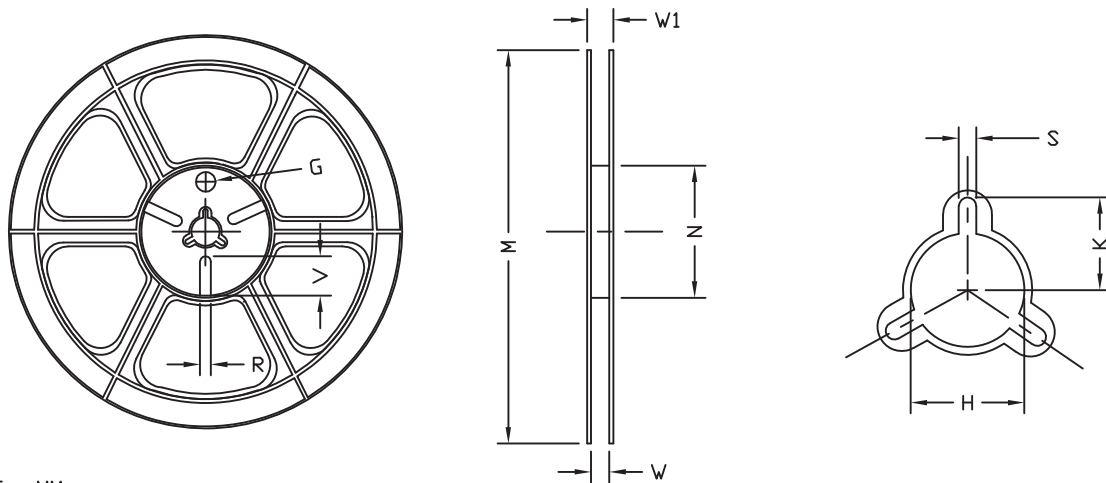
Carrier Tape



UNIT: MM

| PACKAGE | A0 | B0 | K0 | D0 | D1 | E | E1 | E2 | P0 | P1 | P2 | T |
|-------------------|---------------|---------------|---------------|--------------|----------------------|--------------|---------------|---------------|---------------|---------------|---------------|---------------|
| QFN4x4 (12 mm) | 4.35 ±0.10 | 4.35 ±0.10 | 1.10 ±0.10 | 1.50 MIN. | 1.50 +0.1 -0.0 | 12.0 ±0.3 | 1.75 ±0.10 | 5.50 ±0.05 | 8.00 ±0.10 | 4.00 ±0.10 | 2.00 ±0.05 | 0.30 ±0.05 |

Reel



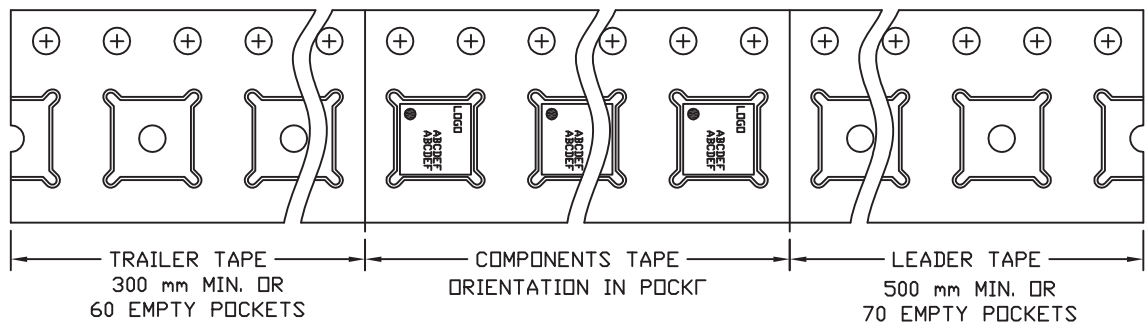
UNIT: MM

| TAPE SIZE | REEL SIZE | M | N | W | W1 | H | K | S | G | R | V |
|-----------|-----------|----------------|---------------|----------------------|----------------------|---------------|--------------|-------------|-----|-----|-----|
| 12 mm | ø330 | ø330.0 ±2.0 | ø79.0 ±1.0 | 12.4 +2.0 -0.0 | 17.0 +2.6 -1.2 | ø13.0 ±0.5 | 10.5 ±0.2 | 2.0 ±0.5 | --- | --- | --- |

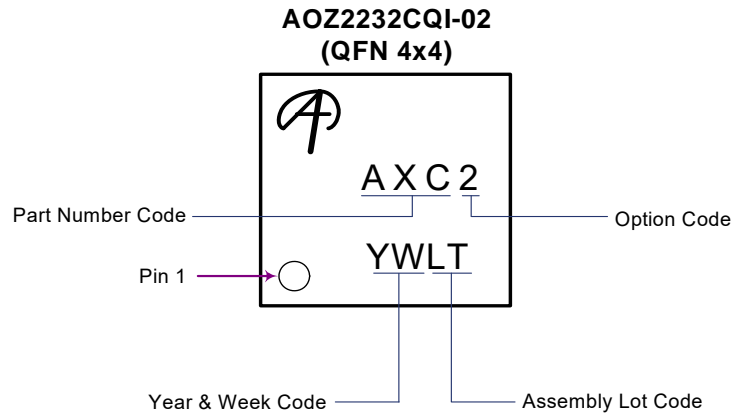
Tape

Leader / Trailer & Orientation

Unit Per Reel:
3000pcs



Part Marking



| Part Number | Part Number Code of Marking |
|---------------|-----------------------------|
| AOZ2232CQI-01 | AXC1 |
| AOZ2232CQI-02 | AXC2 |

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.