ALPHA & OMEGA SEMICONDUCTOR

AOZ32101MDV

100V, 2.5A Half-bridge Gate Driver

General Description

AOZ32101MDV is a 100V half-bridge gate driver that has an integrated bootstrap diode and is designed with shoot-through protection to drive high-side and low-side N-channel MOSFETs safety. The sufficient drive capability and fast rise/fall times support system operate at high frequencies or multiple MOSFETs in parallel.

Built in under voltage lock-out protection pulls the high/low-side output low when the supply voltage is insufficient.

Features

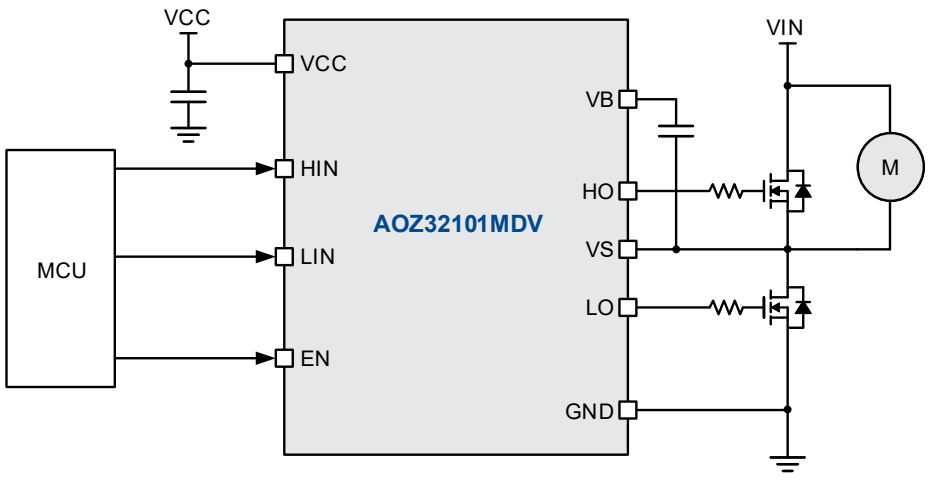
- Drives half bridge, dual N-channel MOSFET
- Integrated bootstrap diode
- 120V max. bootstrap voltage
- Input signal overlap protection
- Typical 30ns propagation delay time
- Drive 1nF load with 13ns rise/fall times with 12V VDD
- TTL compatible input
- Typical 150µA quiescent current
- Less than 5µA shutdown current
- UVLO for both high-side and low-side
- DFN 3mmx3mm 10 pin Packages

Applications

- Brushless DC motors
- Permanent magnet synchronous motors (PMSM)
- Power tools
- E-bike

GREEN Product

Typical Application



Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ32101MDV	-40 °C to +125 °C	10-Pin 3×3 DFN	Green

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

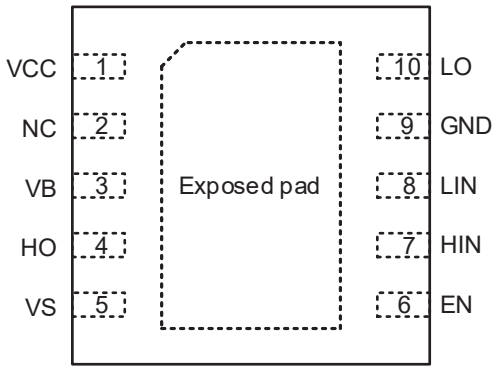


Figure 1. DFN3x3-10L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	VCC	Gate driver supply input.
2	NC	No connection.
3	VB	Bootstrap capacitor connection. An external capacitor between VB and VS for supplying high-side MOSFET is necessary.
4	HO	High-side gate driver output.
5	VS	High-side floating supply return.
6	EN	Enable/disable control.
7	HIN	Signal input for the high-side driver.
8	LIN	Signal input for the low-side driver.
9	GND	Ground.
10	LO	Low-side gate driver output.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Supply Voltage (VCC)	-0.3 V to 20 V
SW Voltage (VS)	-5 V to 105 V
Bootstrap Voltage (VB)	-0.3 V to 120 V
VB to VS	-0.3 V to 18 V
HO	-0.3 V to (VB-VS) +0.3 V
LO to GND	-0.3 V to (VCC+0.3 V)
All Other Pins	-0.3 V to 20 V
Junction Temperature (T_J)	+150 °C
Storage Temperature (T_S)	-65 °C to +150 °C
ESD Rating	1 kV

Maximum Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VCC)	+5.5 V to 18 V
SW Voltage (VS)	-1.0 V to 100 V
Voltage Slew Rate (VS)	5 V/ns
Ambient Temperature (T_A)	-40 °C to +125 °C
Package Thermal Resistance (Θ_{JA}) (Θ_{JC})	 46 °C/W 8.6 °C/W

Electrical Characteristics

T_A = 25 °C, VCC = VB-VS=12V, V_{GND}=VS = 0V, V_{EN}=3.3V, No load at HO and LO, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Current						
I_{SHDN}	VCC shutdown current	VEN=0			1	µA
I_{VCC_Q}	VCC quiescent current	LIN=HIN=0		150	180	µA
I_{VCC_O}	VCC operating current	fsw=50kHz		320	400	µA
I_{VB_Q}	Floating driver quiescent current	LIN=0, HIN=0 or 1		50	70	µA
I_{VB_O}	Floating driver operating current	fsw=50kHz		100	150	µA
I_{LK}	Leakage current	VB=VS=100V		0.1	1	µA
Inputs						
V_{IN_H}	LIN/HIN high logic input voltage		2.4			V
V_{IN_L}	LIN/HIN low logic input voltage				1	V
V_{IN_HYS}	LIN/HIN hysteresis			0.6		V
R_{IN}	LIN/HIN internal pull-down resistance			200		kΩ

Electrical Characteristics *(Continued)*

T_A = 25 °C, VCC = VB-VS=12V, V_{GND}=VS = 0V, V_{EN}=3.3V, No load at HO and LO, unless otherwise specified.

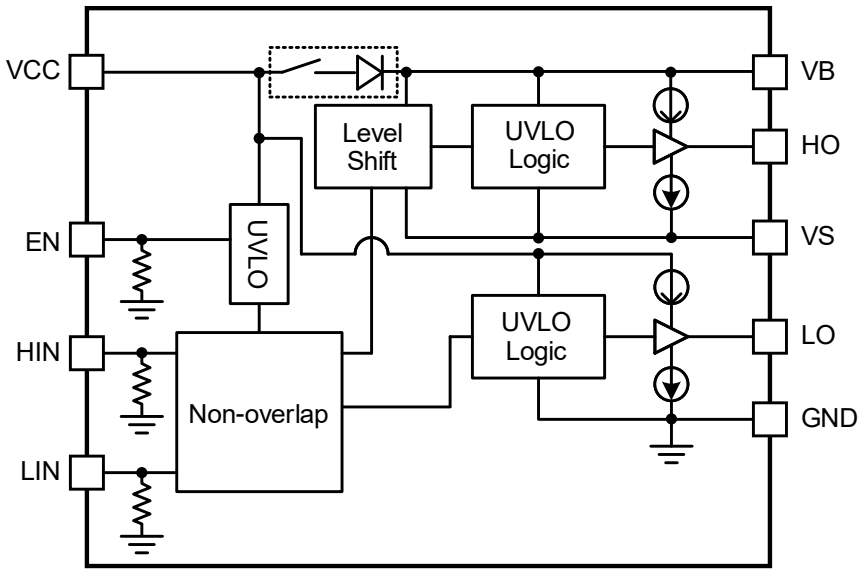
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Under Voltage Protection						
VCC_R	VCC rising threshold		4.6	5	5.4	V
VCC_F	VCC falling threshold		4.1	4.5	4.9	V
VB_R	(VB-VS) rising threshold		4.6	5	5.4	V
VB_F	(VB-VS) falling threshold		4.1	4.5	4.9	V
V_{EN_L}	EN Input Logic Low				0.6	V
V_{EN_H}	EN Input Logic High		1.5			V
V_{EN_HYS}	EN Hysteresis			100		mV
I_{EN}	EN Input Current	V_{EN}=2V, T_A=+25°C		10		µA
		V_{EN}=5V			35	µA
R_{EN}	EN internal pull-down resistance			450		kΩ
Bootstrap Diode						
V_{F1}	Bootstrap diode VF @ 100µA			0.5		V
V_{F2}	Bootstrap diode VF @ 80mA			2.7		V
R_D	Bootstrap diode dynamic R	V_F=1V and 2V		28		Ω
Low-side Gate Driver						
V_{LO_L}	Low level output voltage	I_O=100mA		0.15	0.22	V
V_{LO_H}	High level output voltage to rail	I_O=100mA		0.45	0.6	V
I_{LO_SOURCE}	Peak pull-up current	V_{LO}=0V, VCC=4.5V		0.8		A
		V_{LO}=0V, VCC=12V		2		A
		V_{LO}=0V, VCC=16V		2.5		A
I_{LO_SINK}	Peak pull-down current	V_{LO}=VCC=4.5V		1.2		A
		V_{LO}=VCC=12V		3		A
		V_{LO}=VCC=16V		3.2		A
Floating Gate Driver						
V_{HO_L}	Low level output voltage	I_O=100mA		0.15	0.22	V
V_{HO_H}	High level output voltage to rail	I_O=100mA		0.45	0.6	V
I_{HO_SOURCE}	Peak pull-up current	V_{HO}=0V, VB-VS=5V		0.8		A
		V_{HO}=0V, VCC=12V		2		A
		V_{HO}=0V, VCC=16V		2.5		A
I_{HO_SINK}	Peak pull-down current	V_{HO}=VB-VS=5V		1.2		A
		V_{HO}=VCC=12V		3.1		A
		V_{HO}=VCC=16V		3.5		A

Electrical Characteristics *(Continued)*

T_A = 25 °C, VCC = VB-VS=12V, V_{GND}=VS = 0V, V_{EN}=3.3V, No load at HO and LO, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Switching Characteristics						
Low-side Gate Driver						
t_{PDF_L}	Turn-off propagation delay LIN falling to LO falling			20		ns
t_{PDR_L}	Turn-on propagation delay LIN rising to LO rising			20		ns
t_{R_L}	LO rise time	C_L=1nF		12		ns
t_{F_L}	LO fall time	C_L=1nF		9		ns
Floating Gate Driver						
t_{PDF_H}	Turn-off propagation delay HIN falling to HO falling			20		ns
t_{PDR_H}	Turn-on propagation delay HIN rising to HO rising			18		ns
t_{R_H}	HO rise time	C_L=1nF		12		ns
t_{F_H}	HO fall time	C_L=1nF		9		ns
T_{off_H}	HO minimun off time			550	650	ns

Functional Block Diagram



Timing Diagram

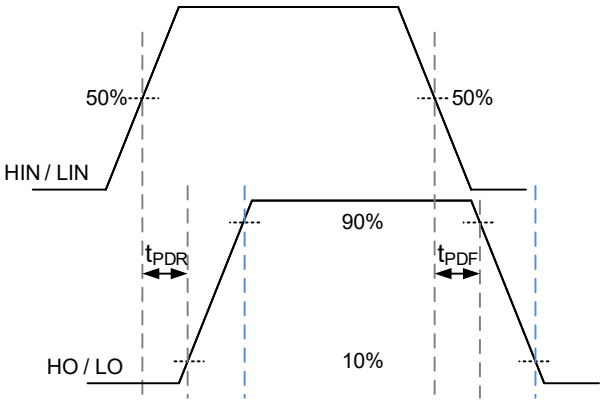


Figure 2. Timing Diagram for AOZ32101MDV

Detailed Description

VCC Power Up and UVLO

In order to ensure the normal operation of the gate driver, if the EN pin is pulled high (normal working state), the gate driver will not work before VCC is higher than the UVLO rising threshold (about 5V), until VCC>5V, the gate driver can work normally. When VCC drops to the UVLO falling threshold (about 4.5V), gate driver shuts down.

VB UVLO

The voltage of the Bootstrap capacitor(VB-VS) is supplied to the high-side gate driver. VB-VS must be greater than (VB-VS) rising threshold to make the high-side gate driver start working. If it is less than (VB-VS) falling threshold, there will be no output.

Bootstrap Circuit

Different from the traditional bootstrap architecture, in addition to the diode on the bootstrap path, AOZ32101MDV also adds a switch (S1) to limit the current. When the charging current exceeds 100mA, it is limited to 100mA. The purpose is to limit the large current of the bootstrap charging moment. In addition, if the charging current is too large, the reverse recover current of the diode will also be too large. The above two reasons may cause damage to the circuit, so the current limiting function can effectively protect the bootstrap diode.

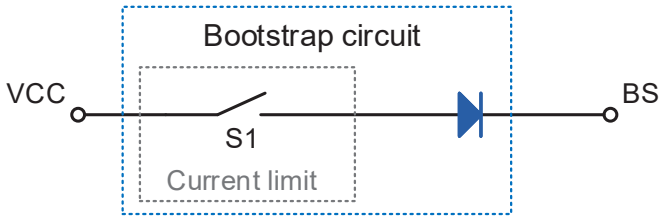


Figure 3. Bootstrap Circuit Architecture

EN Pin

The EN pin is used to enable the gate driver. When the voltage of the EN pin is greater than the EN Logic High voltage, the gate driver works normally. When the EN pin is floating or connected to GND, the gate driver does not work.

The EN pin is internally connected to GND through a 450KΩ pull-down resistor. When the EN pin is not used, the EN pin can be connected to VCC through an external pull-up resistor. The recommended resistor value is 10KΩ.

In addition, it is recommended to input the HIN/LIN signal after the EN pin voltage is higher than VEN_H, and to turn off the HIN/LIN signal before the EN pin voltage is lower than VEN_L.

It is recommended that the EN signal transitions from 2V to 0V in a time not exceeding 1ms.

Control Logic

When EN is pulled high, HO and LO follow their respective HIN and LIN signals through the gate driver to drive MOSFETs, and the internal circuit will also judge whether the HIN/LIN signals are high at the same time to avoid shoot-through of High/Low-side MOSFETs. The truth table of the control logic is as follows.

Table 1. Truth Table of the Control Logic

EN	HIN	LIN	HO	LO
L	L	L	L	L
	H	L	L	L
	L	H	L	L
	H	H	L	L
H	L	L	L	L
	H	L	H	L
	L	H	L	H
	H	H	L	L

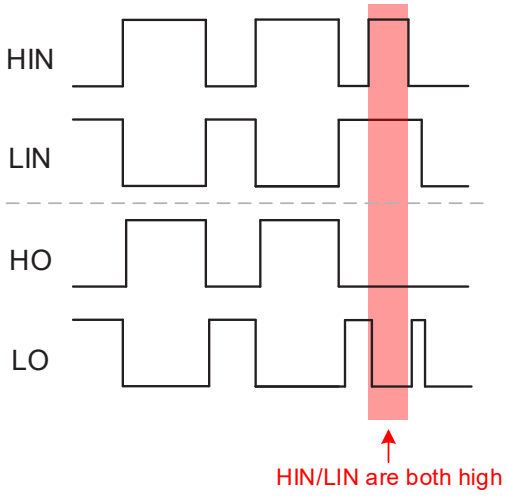


Figure 4. Overlap Prevention

Application Circuit and Layout Guidelines

The AOZ32101MDV has a driving capability of over 2A. A larger driving capability implies that there will be greater noise generated in the circuit when the MOSFET switches on and off moments. If the input voltage increases or the load becomes heavier, the noise will also increase.

GND is the reference potential for the entire system, while VS is the reference potential for the high side driver. If the spikes generated by the switch are too large, it may potentially affect the system.

In order to improve the stability of the system, you can refer to the following circuits and layout when designing the circuit.

1. Connecting a low ESR bypass capacitor in parallel between (VCC to GND)(C1) and (VB to VS)(C2) can effectively reduce the noise in the driver's power supply. The recommended value is 10nF. This bypass capacitor must be placed close to the device leads.
2. EN, HIN, LIN are signal pins. It is recommended to add an RC filter circuit to minimize the impact of noise on the signals received by the driver. The suggested values for R and C are R=10Ω and C=33pF. If the application has a very small duty cycle and there is signal distortion, the values of R and C can be reduced.
3. If the application has a high input voltage or a relatively heavy load, it is recommended to add diodes between (HO to VS)(D1) and (LO to GND)(D2). When GND and VS have large negative voltages, the voltage can be clamped must be located close to the device pins.

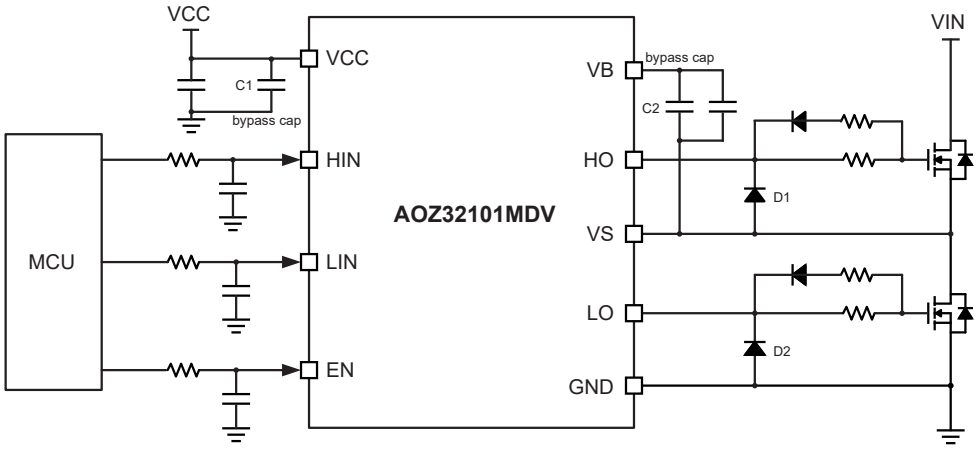


Figure 5. Recommended Application Circuit

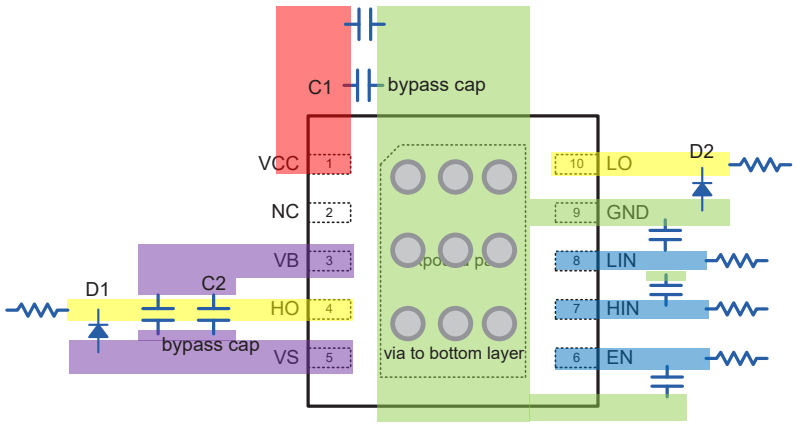
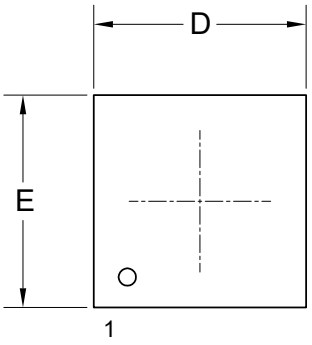
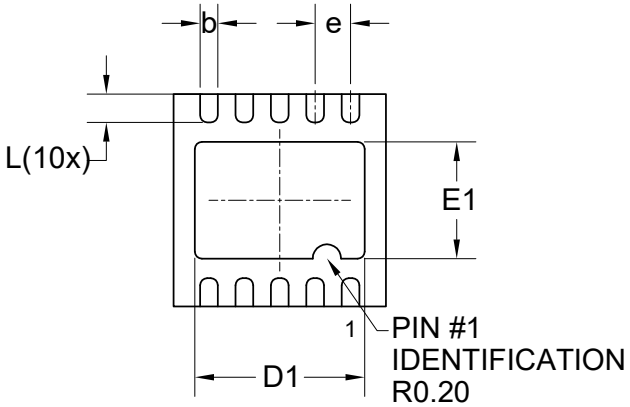


Figure 6. Recommended PCB Layout

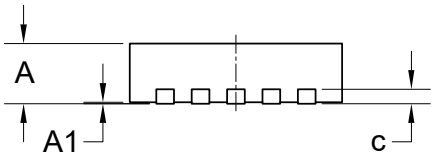
Package Dimensions, DFN3x3-10L



TOP VIEW

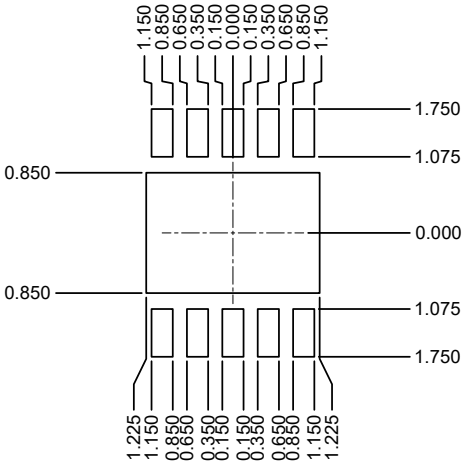


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



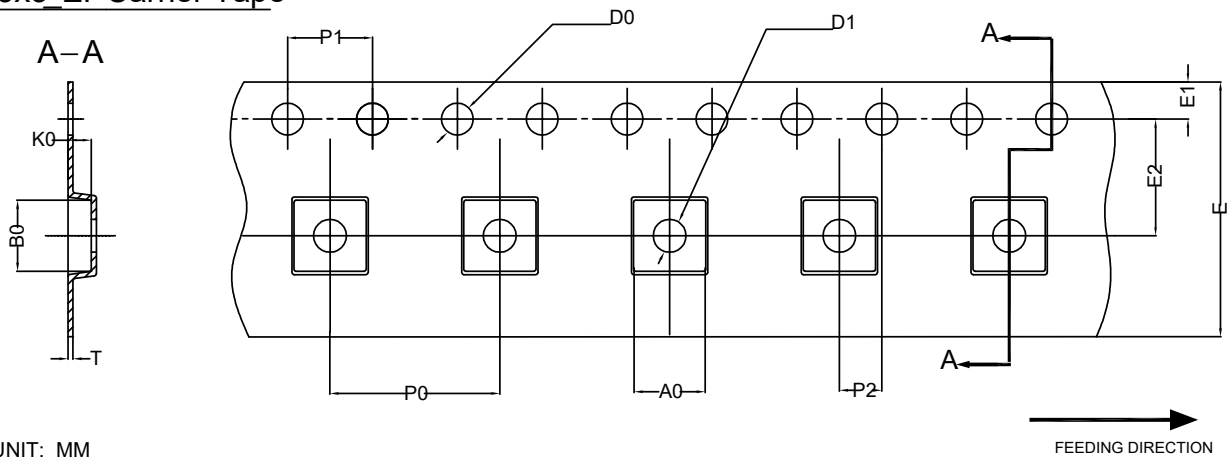
SYMBOL	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	---	0.05	0.000	----	0.002
b	0.20	0.25	0.30	0.008	0.010	0.012
c	0.203 REF.			0.008 REF.		
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.30	2.40	2.50	0.091	0.094	0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	1.55	1.65	1.75	0.061	0.065	0.069
e	0.50 BSC			0.002 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

UNIT: mm

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, DFN3x3-10L

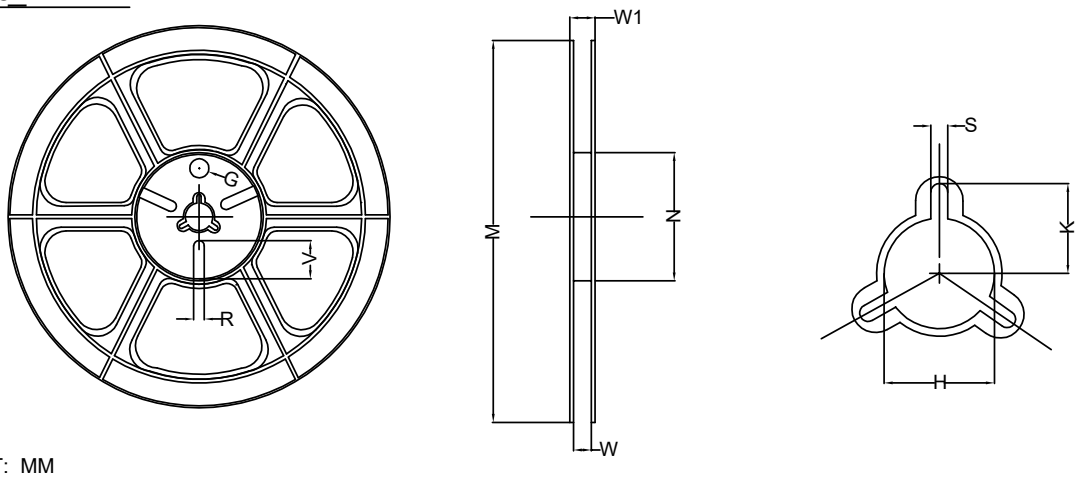
DFN3x3_EPCarrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN3x3_EP	3.40 ±0.10	3.35 ±0.10	1.10 ±0.10	1.50 +0.10 -0	1.50 +0.10 -0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

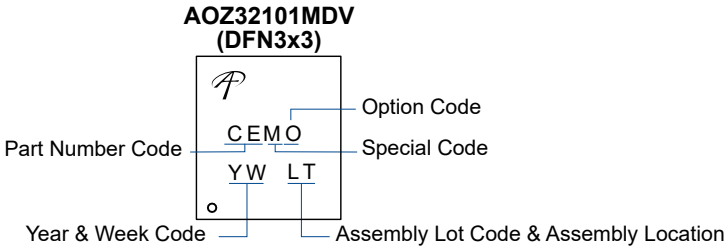
DFN3x3_EP Reel



UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	Ø330	Ø330.00 ±0.50	Ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	Ø13.00 +0.50 -0.20	10.60	2.00 ±0.50	---	---	---

Part Marking



Part Number	Description	Code
AOZ32101MDV	Green Product	CEM0

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.