AOZ52177QI

High-Current, High-Performance Smart Power Stage

General Description

The AOZ52177QI is a general-purpose Smart Power Stage (SPS) consisting of two asymmetrical MOSFETs and an integrated driver for high current, high frequency DC-DC converters.

The AOZ52177QI provides an output current signal (IMON), which reports the real-time module current with a gain of 5 mV/A. The IMON signal can be directly used to replace inductor DCR sensing or resistor sensing in multiphase voltage regulator systems without the need for temperature compensation.

The AOZ52177QI also includes an accurate module temperature monitor (TMON). TMON is a voltage sourced signal with a gain of 8 mV/°C.

The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra-low ON resistance to minimize conduction loss. The standard 5 mm x 6 mm QFN package is optimally designed to minimize parasitic inductance for minimal EMI signature.

Features

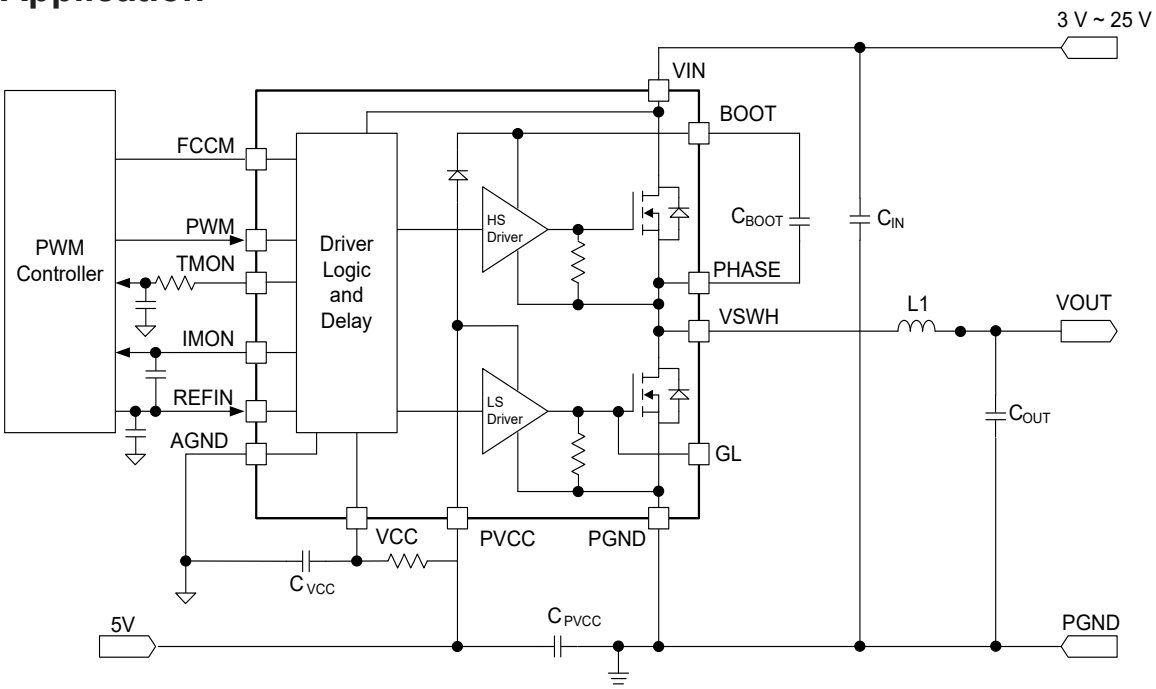
- 3 V to 25 V power supply range
- 70 A continuous output current
  - Up to 100 A for 10 ms instantaneous current
  - Up to 150 A for 10 µs instantaneous current
- Optimized for switching frequency up to 1.5 MHz
- Integrated current monitor (5 mV/A) with typical 5% accuracy over temperature
- Integrated temperature monitor (8 mV/°C) with 2% accuracy
- Fault Indicator
- Under-Voltage LockOut (UVLO) on VCC
- Over-Current Protection
- Zero Current Detect Function
- Over Temperature Protection
- Standard QFN5x6-39L package

Applications

- Server systems
- High end CPU/GPU Power Stage
- Communications Infrastructure

GREEN Product

Typical Application

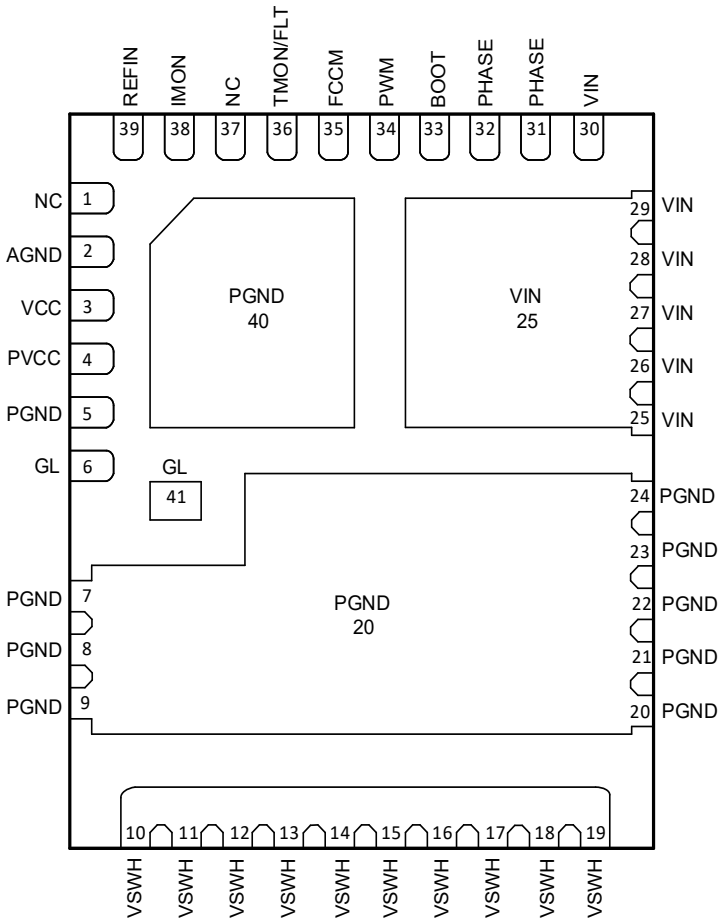


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ52177QI	-40 °C to 125 °C	QFN5x6-39L	RoHS

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

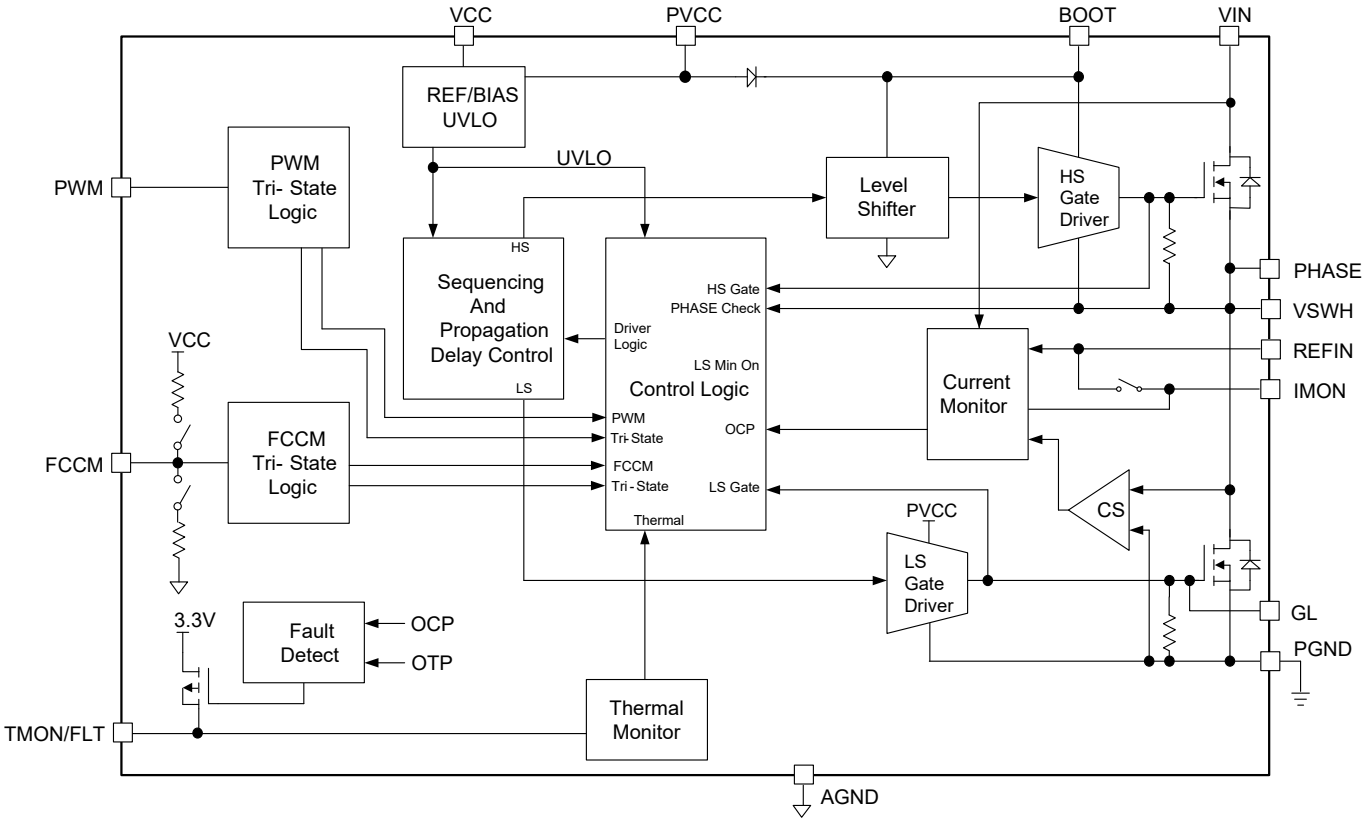


QFN5x6-39L
(Top Transparent View)

Pin Description

Pin Number	Pin Name	Pin Function
1	NC	No connect
2	AGND	Signal Ground.
3	VCC	5 V Bias for Internal Logic Blocks. Ensure to position a 1 µF MLCC directly between VCC and AGND (Pin 2).
4	PVCC	5 V Power Rail for High-Side and Low-Side MOSFET Drivers. Ensure to position a 1 µF MLCC directly between PVCC and PGND (Pin 5).
5	PGND	Power Groundfor High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1µF directly between PGND and PVCC (Pin4).
6, 41	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
7, 8, 9, 20, 21, 22, 23, 24, 40	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
10, 11, 12, 13, 14, 15, 16, 17, 18, 19	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET.
25, 26, 27, 28, 29, 30	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
31, 32	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 33).
33	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100 nF ceramic capacitor between BOOT and the PHASE (Pin 32).
34	PWM	PWM input signal from Controller IC. This input is compatible with 3.3 V and 5 V Tri-State logic level.
35	FCCM	Continuous conduction mode of operation is triggered when FCCM = High. Discontinuous mode is allowed and diode emulation mode is active when FCCM = Low. When FCCM is tri-stated, SPS enters a low power shutdown mode
36	TMON/FLT	Temperature Monitor and Fault Flag Pin. TMON/FLT will be pulled HI (~3.3 V) to indicate an Over-Temperature fault. For multi-phase application, the TMON/FLT pin can be connected together as a common bus. The highest voltage representing the highest temperature among all phases will be sent to the PWM controller. No more than 470 pF total capacitance can be directly connected across TMON/FLT and AGND (Pin 2). A higher capacitance load is allowed with a series resistor (~1 kΩ) for up to 1 nF. At 0°C and in normal operation, the output voltage is 0.6V with a temperature coefficient value of 8 mV/°C. There is an internal pull up source to 3.3 V when a fault condition occurs.
37	NC	No connect
38	IMON	Current Monitor output signal referenced to REFIN (Pin 39). Connect the IMON output to the appropriate Current Sense input of the controller. No more than 47 pF capacitance can be directly connected across IMON and REFIN pins. With a 100 Ω series resistor, up to 470 pF may be used.
39	REFIN	Input for external reference voltage for IMON (Pin 38). This voltage should be between 0.7 V and 2.0 V. Nominal value is 1.2 V. Place a low ESR ceramic capacitor (~ 0.1 µF) from this pin to AGND (Pin 2). Connect REFIN to the appropriate Current Sense Reference output from the controller.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3 V to 6 V
High Voltage Supply (VIN)	-0.3 V to 30 V
Control Inputs (PWM, FCCM)	-0.3 V to (VCC + 0.3 V)
Output (TMON/FLT, IMON)	-0.3 V to (VCC + 0.3 V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3 V to 35 V
Bootstrap Voltage Transient (1) (BOOT-PGND)	-8 V to 40 V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3 V to 6 V
BOOT Voltage Transient (1) (BOOT-PHASE/VSWH)	-0.3 V to 9 V
Switch Node Voltage DC (PHASE/VSWH)	-0.3 V to 30 V
Switch Node Voltage Transient (1) (PHASE/VSWH)	-8 V to 38 V
Low-Side Gate Voltage DC (GL)	(PGND - 0.3 V) to (PVCC + 0.3 V)
Low-Side Gate Voltage Transient (1) (GL)	(PGND - 2.5 V) to (PVCC + 0.3 V)
VSWH Current DC	70 A
VSWH Current 10ms Pulse	100 A
VSWH Current 10us Pulse	150 A
Storage Temperature (TS)	-65°C to +150°C
Max Junction Temperature (TJ)	150°C
ESD Rating (2)	±2 kV HBM ±1 kV CDM

Notes:
1. Peak voltages can be applied for 10 ns per switching cycle.
2. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5 Ω in series with 100 pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	3 V to 25 V
Low Voltage/ MOSFET Driver Supply (VCC, PVCC)	4.5 V to 5.5 V
Control Inputs (PWM, FCCM)	0 V to VCC
Output (TMON/FLT, IMON)	0 V to VCC
Operating Frequency	200 kHz to 1.5 MHz

Electrical Characteristics[3]

T_J = 25°C to 125°C. Typical values reflect 25°C ambient temperature; VIN = 12 V, VCC = PVCC = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
V_{VIN}	Power Stage Power Supply		3		25	V
V_{CC}	Low Voltage Bias Supply	PVCC = VCC	4.5		5.5	V
$R_{\theta JC}$[4]	Thermal Resistance	PCB Temp = 100°C		1.5		°C/W
$R_{\theta JA}$[4]		Fsw = 600 kHz, Vo = 1 V. AOS Demo Board		12		°C/W
Input Supply and UVLO						
V_{CC_UVLO}	VCC Under-Voltage Lockout	VCC Rising	3.4	3.8	4.2	V
V_{CC_HYST}		VCC Hysteresis		400		mV
t_{VCC_DEL}	VCC Power On Delay	From VCC UVLO release		100		µs
I_{VCC}	Control Circuit Bias Current	FCCM = H or L		4		mA
		FCCM = Floating		4		mA
I_{PVCC}	Drive Circuit Operating Current	FCCM = Floating			1	µA
		PWM = 300 kHz, 20% Duty Cycle		13		mA
		PWM = 600 kHz, 20% Duty Cycle		26		mA
PWM Input						
V_{PWMH}	PWM Logic High Input Voltage				2.85	V
V_{PWML}	PWM Logic Low Input Voltage		0.65			V
R_{PWM_DOWN}	PWM Pin Input Current	Pull down		16		kΩ
R_{PWM_UP}		Pull up		33		kΩ
V_{PWM_TRI}	PWM Tri-State Window		1.1		2.1	V
V_{PWM_FLOAT}	PWM Tri-State Voltage Clamp	PWM = Floating	1.5	1.7	1.9	V
t_{PWM_SKIP}	Minimum PWM Pulse Detection				10	ns
t_{PWMH_MIN}	Forced Minimum High-side On Pulse			20		ns
t_{PWML_MIN}	Forced Minimum Low-side on Pulse			60		ns
FCCM Input						
V_{FCCMH}	FCCM Logic High Input Voltage				2.85	V
V_{FCCML}	FCCM Logic Low Input Voltage		0.65			V
R_{FCCM_DOWN}	FCCM Input Resistance	Pull down		100		kΩ
R_{FCCM_UP}		Pull up		200		kΩ
V_{FCCM_TRI}	FCCM Tri-State Window		1.1		2.1	V
V_{FCCM_FLOAT}	FCCM Tri-State Voltage Clamp	FCCM = Floating	1.5	1.7	1.9	V
t_{PD_EN}	Propagation Delay for PWM Operation	FCCM from Tri-State to H or L		4		µs
t_{PD_DIS}	Propagation Delay for Disable	FCCM from H or L to Tri-State		5		µs

Electrical Characteristics[3]

T_J = 25°C to 125°C. Typical values reflect 25°C ambient temperature; VIN = 12 V, VCC = PVCC = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Zero Cross Detect (ZCD) Function						
I_{ZCD_OFS}	ZCD Current Threshold Offset	PWM = L, Inductor = 150 nH, VOUT = 0.6 V, F_{SW} = 600 kHz		2		A
t_{ZCD_BLK}	ZCD Blanking Time	PWM = L		250		ns
Gate Driver Timing						
t_{PDLU}	PWM to High-Side Gate	PWM: H → L, VSWH: H → L		25		ns
t_{PDLL}	PWM to Low-Side Gate	PWM: L → H, GL: H → L		20		
t_{PDHU}	Low-side to High-Side Gate Deadtime	GL: H → L, GH[5]: L → H		15		
t_{PDHL}	High-Side to Low-side Gate Deadtime	VSWH: H → 1V, GL: L → H		8		
t_{TSSHD}	Tri-State Shutdown Delay	PWM: L → V_{PMW_TRI}, GL: H → L and PWM: H → V_{PMW_TRI}, VSWH: H → L	15		50	
t_{TSEXIT}	Tri-State Propagation Delay	PWM: V_{PMW_TRI}, → H, VSWH: L → H PWM: V_{PMW_TRI}, → L, GL: L → H			30	
IMON Timing and Operating Range, and Accuracy						
t_{FALL_BLK}	VSWH Falling Blanking Time			250		ns
t_{PRO_DEL}	IL to IMON Propagation Delay	L = 150 nH, FSW = 600 kHz, VOUT = 1.8 V IMON Valley to IL Valley		60	75	ns
V_{REFIN}	REFIN Voltage Range		0.7	1.2	2.0	V
V_{IMON}	IMON Voltage Range		0.3		3	V
C_{IMON}	Max IMON Output Capacitance Allowed	Across IMON and REFIN	10		47	pF
		With 100 Ω resistor in series			470	pF
A_{IMON}	IMON Gain	CCM		5		mV/A
V_{IMON_ACC}	IMON Accuracy	-10A < IOUT < 10A	-1		1	A
		10A < IOUT < 80A		+/-3		%
V_{IMON_OFF}	Current-sense offset	VCS = 1.2 V, TJ = 25°C	-2		+2	mV
TMON Operating Range and Over-Temperature Threshold						
A_{TMON_SLP}	TMON Slope Gain	No Load	7.8	8	8.2	mV/°C
V_{TMON_25C}	TMON Voltage at 25°C	$V(T_{JCT})$ = 0.6 V + (8mV x T_{JCT})	0.784	0.8	0.816	V
V_{TMON_125C}	TMON Voltage at 125°C	$V(T_{JCT})$ = 0.6 V + (8mV x T_{JCT})	1.56	1.6	1.64	V
I_{TMON_SOUR}	TMON Sourcing Current	TMON = 0 V		400		µA
I_{TMON_SINK}	TMON Sinking Current	TMON = 3.3 V		25		µA
T_{OTP}	Over-Temperature Threshold	Temperature Rising	135	145	155	°C
T_{OTP_HYST}	Over-Temperature Hysteresis			20		°C

Electrical Characteristics[3]

T_J = 25°C to 125°C. Typical values reflect 25°C ambient temperature; VIN = 12 V, VCC = PVCC = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Current Limit						
I_{LIM}	Over Current Limit			120		A
I_{LIM_HYS}	Over Current Limit Hysteresis			15		A
N_{OC_COUNT}	OC Counts before Reporting Fault and HS Latches Off			10		Counts
Fault Output Indicator						
I_{TMON_FLT}	TMON/FLT Output Current at Fault Conditions	TMON/FLT = 2.5 V	4			mA
t_{TMON_FLT}	TMON/FLT Fault Report Delay			22		ns

Notes:
3. All voltages are specified with respect to the corresponding AGND pin.
4. Characterization value. Not tested in production.
5. GH is an internal pin.

Timing Diagrams

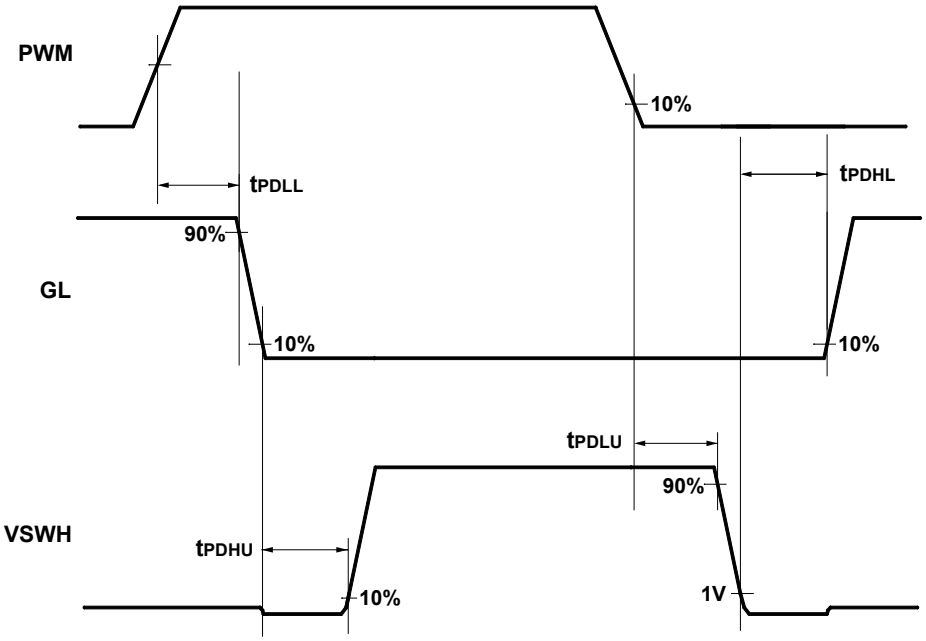


Figure 1. PWM Logic Input Timing Diagram

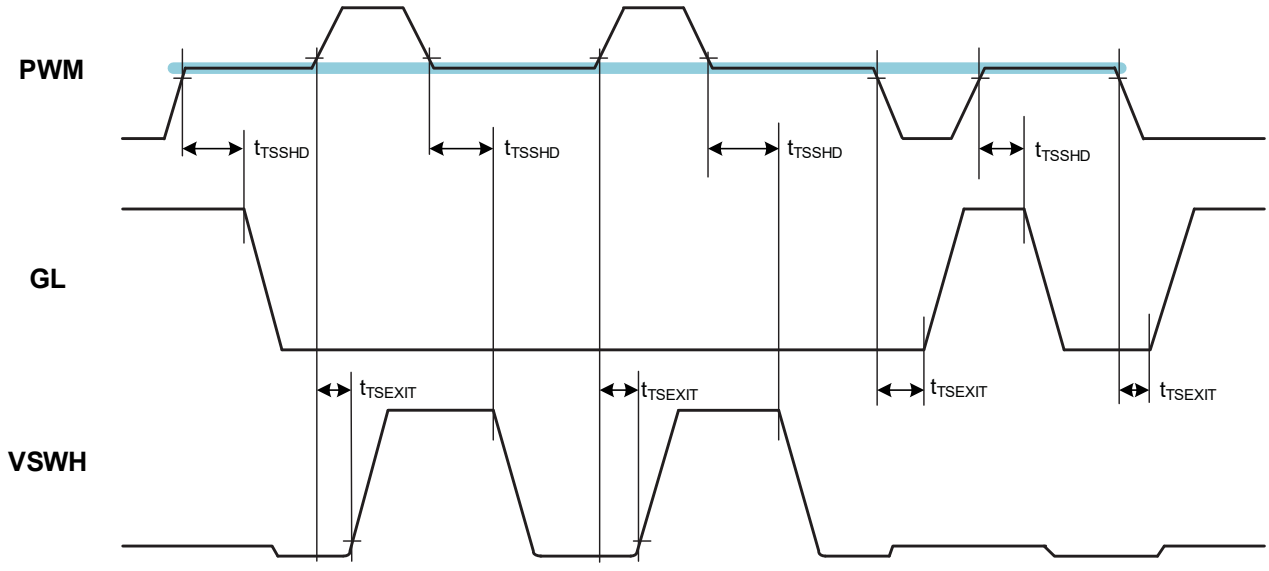


Figure 2. PWM Tri-State Hold Off and Exit Timing Diagram

Application Information

AOZ52177QI is a fully integrated smart power module designed to work over an input voltage range of 3V to 25V with 5V supplies for gate drive and internal control circuits. This smart power stage module features accurate current monitoring (IMON) which provides both High-Side and Low-Side MOSFET current information in both constant current and diode emulated mode operation. It also features temperature monitoring (TMON) which provides continuous thermal reading of the module temperature. Additional features such as Control Circuit Input Voltage (VCC) UVLO and light load efficiency control.

The High-Side and Low-Side MOSFETs are combined into one package with the pin configuration optimized for power routing with minimum parasitic inductance. The MOSFETs are individually tailored for efficient operation in low duty cycle synchronous buck converter applications. In addition, a high current driver is also included in the package to minimize the gate drive loop delay resulting in extremely fast switching

Powering the Module and the Gate Drives

An external 5V supply (PVCC) is required for driving the MOSFETs. The MOSFETs are designed with low gate thresholds so that lower drive voltage can be used to reduce the switching and drive losses without compromising the conduction losses. The integrated gate driver is capable of supplying high peak current into the gate of Low-Side MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 1µF or higher is recommended from PVCC to PGND. For effective filtering it is strongly recommended to have a direct connection from this capacitor to PGND.

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor between BOOT pin and the switching node (PHASE). It is recommended that this capacitor *Cboot* should be connected as close as possible to the device across PHASE (Pin 19) and BOOT (Pin 20). Rboot is an optional external resistor that can be used by designers to slow down the turn on speed of the High-Side MOSFET. Selecting the *Rboot* value is a compromise between switching speed and the amplitude of power switching node (VSWH) voltage spikes. Typical values of *Rboot* are between 1Ω and 5Ω.

Power-On Reset (POR)

During initial start-up, VCC voltage rise is monitored. Once the rising VCC voltage exceeds 3.4V (V_{VCC_UVLO}) and FCCM is High or Low, normal operation of the driver is enabled. The PVCC voltage is not being monitored as it should be connected to VCC. VCC POR is gated to the TMON/FLT pin, which resumes normal TMON operation 8µs after VCC is above their POR levels and no other faults occur.

The AOZ52177QI must be powered up before the PWM input is applied. During start-up it is necessary for the PWM signal to go through a proper soft start sequence to minimize inrush current in the converter. Powering the module with a full duty cycle PWM signal applied may lead to a number of undesirable consequences.

FCCM Input

FCCM is a Tri-State compatible input. When FCCM = Low, Discontinuous Conduction Mode (DCM) is allowed, and diode emulation is active when with the built-in Zero Cross Detection (ZCD) features. When FCCM = High, AOZ52177QI enters Continuous Conduction Mode (CCM) mode, where VSWH follows the state of PWM. When FCCM = Floating, the driver shuts down to a low power state.

The FCCM Threshold in Table 1 lists the thresholds for high-level and low-level logic, as well as Tri-State operation.

Table 1. FCCM Input and Tri-State Thresholds

Parameters	V_{FCCMH}	V_{FCCML}	$V_{TRI(L)}$	$V_{TRI(H)}$
Thresholds	2.85 V	0.65 V	1.1 V	2.1 V

PWM Input

The AOZ52177QI is compatible with 3.3V and 5V PWM input logic and supports Tri-State PWM. When the input is high impedance or left open, both the gate drive outputs will be turned off and the Low-Side and High-Side gates are actively held low. The PWM Threshold in Table 2 lists the thresholds for high-level and low-level logic, as well as Tri-State operation.

Table 2. PWM Input and Tri-State Thresholds

Parameters	V_{PWMH}	V_{PWMH}	$V_{TRI(L)}$	$V_{TRI(H)}$
Thresholds	2.85 V	0.65 V	1.1 V	2.1 V

The AOZ52177QI is compatible with standard multiphase controllers as well as other controller IC's utilizing 5 V and 3.3V PWM logic. If the PWM input is being pulled into and remains in the Tri-State window for a set hold-off time (t_{TSEXIT}), the driver will force both MOSFETs to their off state. When the PWM signal moves outside the Tri-State window, the driver immediately resumes operation and drives the MOSFETs according to the PWM input.

This feature allows the controller to use PWM as a method of forcing both MOSFETs to be off. For the condition that the PWM input is floating, the pin will be pulled into the Tri-State Clamp Voltage (V_{PWM_FLOAT}) internally, thus forcing both MOSFETs to a safe off state. Table 3 shows the logic truth table for PWM and FCCM inputs.

Table 3. GH and GL Operation Truth Table

FCCM	PWM	GH[6]	GL
Tri-State	X	0	0
0	1	1	0
0	0	0	1
1	1	1	0
1	0	0	1
X	Tri-State	0	0

Note:
6. GH signal is not available on package level

Current Monitoring (IMON)

An accurate Current Sense Amplifier monitors the current through the Low-Side MOSFET. A voltage signal proportional to that current appears at the IMON (Pin 25), relative to REFIN (Pin 24), at a current sense gain of 5 mV/A. Both IMON and REFIN should be connected to the appropriate current sense inputs of the controller. This IMON signal effectively eliminates the needs of using external sense resistor or inductor DCR sensing.

Figure 3 shows the Low-Side MOSFET current sense mechanism. After the falling edge of the PWM, there are two delays:

1. The expected propagation delay from PWM to VSWH (t_{PDLU})
2. The blanking delay to allow time for the transition to settle (t_{FALL_BLK})

The IMON signal approximates the actual inductor current waveform.

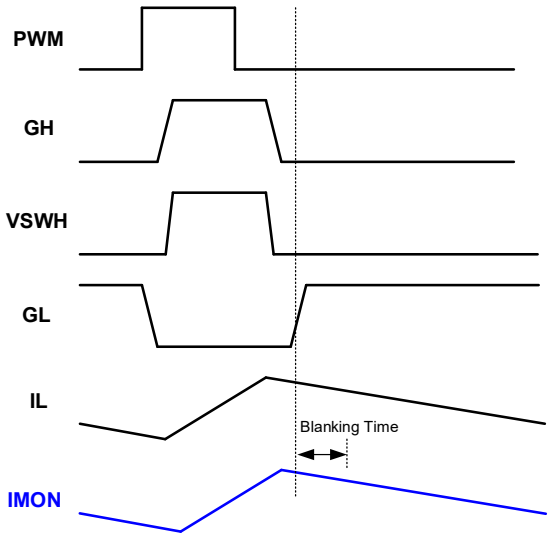


Figure 3. Commutating Current Re-Construction at IMON

Temperature Monitoring (TMON/FLT)

AOZ52177QI monitors its internal temperature and provides a signal proportional to that temperature on the TMON/FLT pin. TMON/FLT has a voltage of 600 mV at 0 °C and temperature gain of 8 mV/°C (A_{TMON_SLP}). Figure 4 shows a simplified functional representation. The top section represents the protection fault that will pull the output high. The mid-section shows the symbolic sensor and the output buffer. The bottom section will set the initial state of TMON/FLT before the module is active. The TMON/FLT pin is configured internally such that a user can tie multiple pins together externally and the resulting TMON/FLT bus will assume the voltage of the highest contributor (representing the highest temperature).

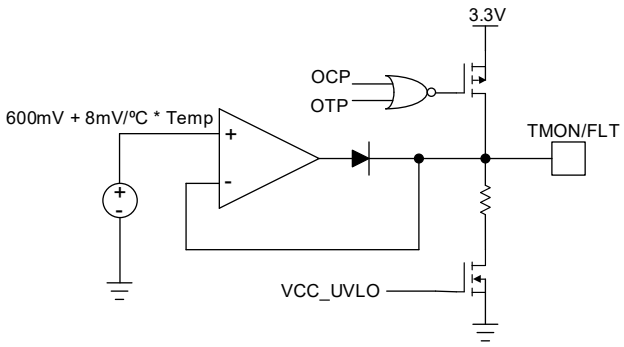


Figure 4. Temperature Monitor Internal Circuit

Zero Cross Detect (ZCD)

ZCD will detect the valley current when Low-Side MOSFET is on. If the current is less than 2 A (I_{ZCD_OFS}), the Low-Side MOSFET will be turned off independent of PWM logic level. This is an automatic light load mechanism and suitable for most analog PWM controllers.

Over Temperature Protection (OTP)

If the internal temperature exceeds the Over-Temperature threshold (T_{OTP}), the TMON/FLT (Pin 36) is pulled to 3.3 V after 100 ns ($t_{TMON/FLT}$) delay. Both High-Side and Low-Side MOSFETs are turned off under OTP condition. The TMON/FLT will remain in the fault mode until the junction temperature drops below the hysteresis threshold (T_{OTP_HYST}). At that point, the TMON/FLT and IMON pins resume normal operation.

Over Current Protection (OCP)

An Over Current Protection (OCP) fault is detected when the current running through the power stage exceeds 120 A (I_{LIM}). When the OCP is detected, the High-Side MOSFET ON time will be truncated to a maximum of 400 ns for

every switching cycle. If the OCP event is trigged 10 times (N_{OC_COUNT}) consecutively, TMON/FLT (Pin 1) will be internally pulled to 3.3 V to indicate a fault condition.

The FAULT flag will be released by a power reset or the output current is 15 A less than the OCP threshold.

FAULT Reporting

These 4 protection functions will trigger the fault reporting at TMON/FLT (Pin 1):

1. VCC Under-Voltage Lock-Out (UVLO)
2. Over-Current Protection (OCP)
3. Over-Temperature Protection (OTP)

For UVLO function, TMON/FLT will be pulled down to ground to indicate under voltage fault condition.

For OCP and OTP reporting, TMON/FLT will be pulled high to 3.3 V to indicate the fault condition. At the same time, both High-Side and Low-Side MOSFETs will be turned off to protect the module from over-heating. The PWM controller should quickly recognize when it is outside normal operating conditions.

All of the above faults are summarized in Table 4.

Table 4. GH and GL Operation Truth Table

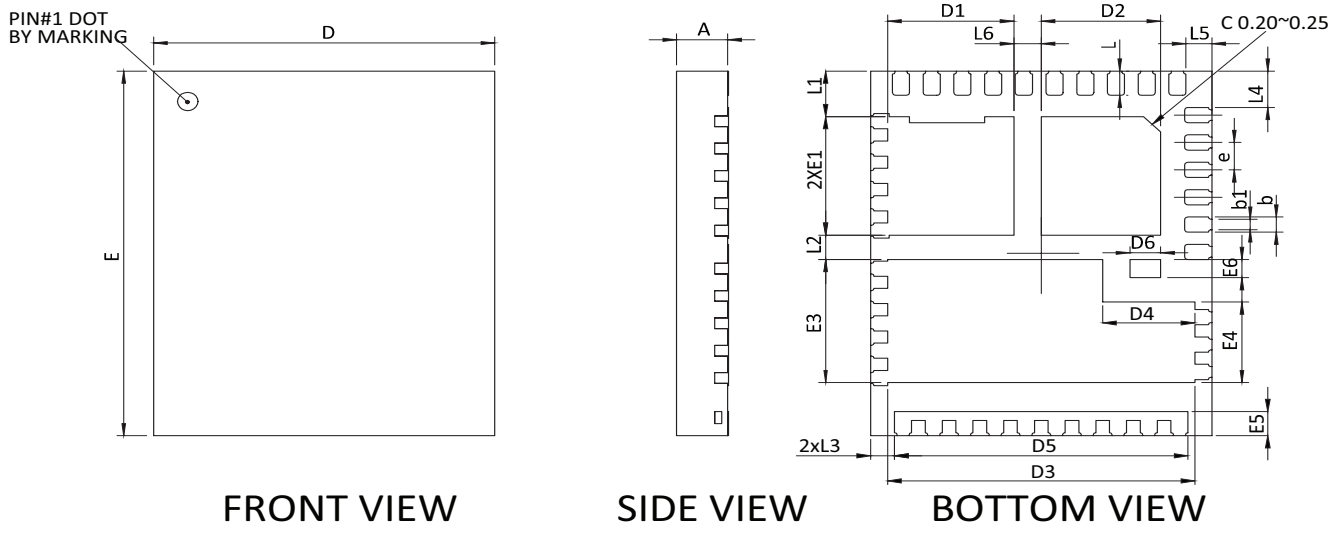
Fault	Respose
VCC UVLO	Fault Flag pulled down only
OCP	Fault Flag pulled to 3.3 V after 10 consecutive occurrences High-Side MOSFET maximum on time = 400 ns
OTP	Fault Flag pulled to 3.3 V Both MOSFETs are off

Protection Feature and Function Summary

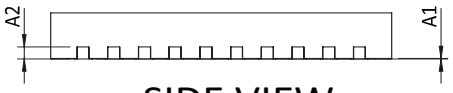
Table 5. Protection Feature and Function Summary

Protection	Entry Condition	Action	Release Condition
Over Current Protection (OCP) See Protection Case	• IMON peak senssing • 10 consecutive occurences of over current condition	• TMON/FLT pull up to 3.3 V after 10 consecutive occurences of over current condition • IMON continue to generate current information	• Power reset (UVLO_VCC) or • 3 consecutive cycles of load current below OCP falling threshhold or • PMW to tri-state for 2 µs
Zero Current Detection (ZCD)	• IMON valley sensing • Inductor current < 2A as reported by IMON • Blanking time of (LS on state) is 250 ns	• LS off until next cycle	• PWM rising
Over Temparature Protection (OTP)	• TMON sensing • TMON voltage above 1.69 V (136°C)	• Turn off both HS and LS • TMON/FLT pull up to 3.3 V	• TMON voltage below 1.57 V (121°C)
Driver IC Supply UVLO (VCC_UVLO)	• VCC sensing • VCC voltage below 3.4 V • No PVCC sensing	• HS, LS, TMON & IMON are disabled • TMON/FLT pull low • IMON Shorted to REFIN	• VCC voltage above 3.8 V (400 mV Hysteresis)

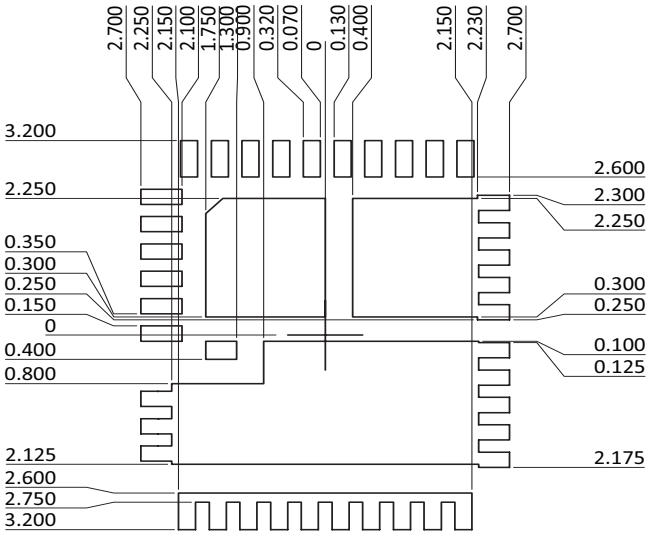
Package Dimensions, QFN5x6-39L



FRONT VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW



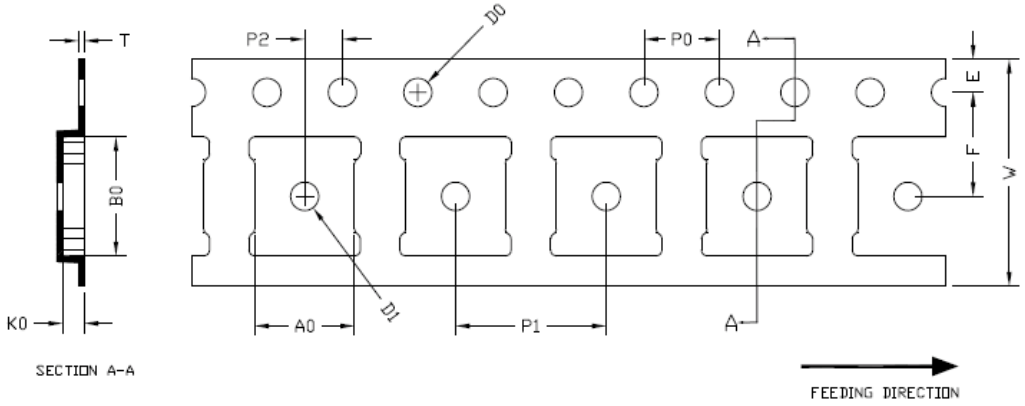
RECOMMANDED LAND PATTERN

SYMBOLS	DIMENSION IN MM.			DIMENSION IN INCH.		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20REF			0.008REF		
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	1.75	1.85	1.95	0.069	0.073	0.077
D2	1.65	1.75	1.85	0.065	0.069	0.073
D3	4.40	4.50	4.60	0.173	0.177	0.181
D4	1.26	1.36	1.46	0.050	0.054	0.057
D5	4.20	4.30	4.40	0.165	0.169	0.173
D6	0.35	0.45	0.55	0.014	0.018	0.022
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	1.85	1.95	2.05	0.073	0.077	0.081
E3	1.93	2.03	2.13	0.076	0.080	0.084
E4	1.20	1.30	1.40	0.047	0.051	0.055
E5	0.30	0.40	0.50	0.012	0.016	0.020
E6	0.20	0.30	0.40	0.008	0.012	0.016
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.65	0.75	0.85	0.026	0.030	0.033
L2	0.30	0.40	0.50	0.012	0.016	0.020
L3	0.25	0.35	0.45	0.010	0.014	0.018
L4	0.50	0.60	0.70	0.020	0.024	0.028
L5	0.28	0.38	0.48	0.011	0.015	0.019
L6	0.30	0.40	0.50	0.012	0.016	0.020
b	0.15	0.25	0.35	0.006	0.010	0.014
b1	0.08	0.18	0.28	0.003	0.007	0.011
e	0.45BSC			0.018BSC		

NOTE
1.CONTROLLING DIMENSION IS MILLIMETER.
2.CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN5x6-39L

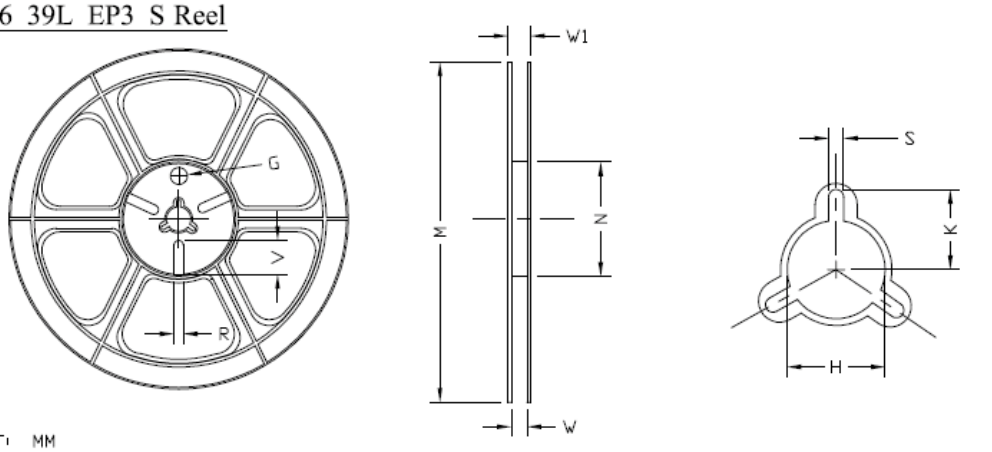
QFN5x6_39L_EP3_S Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E	F	P0	P1	P2	T
QFN5X6	5.30 ±0.10	6.30 ±0.10	1.15 ±0.10	ø1.50 +0.10 −0.00	ø1.50 +0.20 −0.00	12.00 +0.30 −0.10	1.75 ±0.10	5.50 ±0.05	4.00 ±0.10	8.00 ±0.10	2.00 ±0.05	0.30 ±0.03

QFN5x6_39L_EP3_S Reel



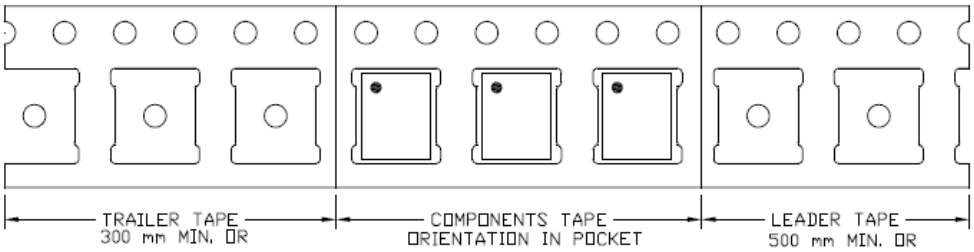
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330 ±0.50	ø97.00 ±0.10	13.0 ±0.30	17.40 ±1.00	ø13.0 +0.5 −0.2	10.6	2.00 ±0.50	---	---	---

QFN5x6_39L_EP3_S Tape

Leader / Trailer & Orientation

Unit Per Reel: 3000pcs



Part Marking