AOZ52371QI

High-Current, High-Performance Smart Power Stage

General Description

The AOZ52371QI is a general-purpose Smart Power Stage (SPS) for computing notebook CPU power, consisting of two asymmetrical MOSFETs and an integrated driver for high current, high frequency, and DC-DC converter.

The AOZ52371QI provides an output current signal (IMON). The IMON signal can be directly used to replace inductor DCR sensing or resistor sensing in the multiphase voltage regulator systems without the need for temperature compensation.

The AOZ52371QI also includes an accurate module thermal monitor (TMON). TMON is a voltage sourced PTAT signal with a gain of 8 mV/°C.

The MOSFETs are individually optimized for operation in the synchronous buck configuration. The high side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The low side MOSFET has ultra-low ON resistance to minimize conduction loss. The standard 5 mm × 5 mm QFN package is optimally designed to minimize parasitic inductance for minimal EMI signature.

Features

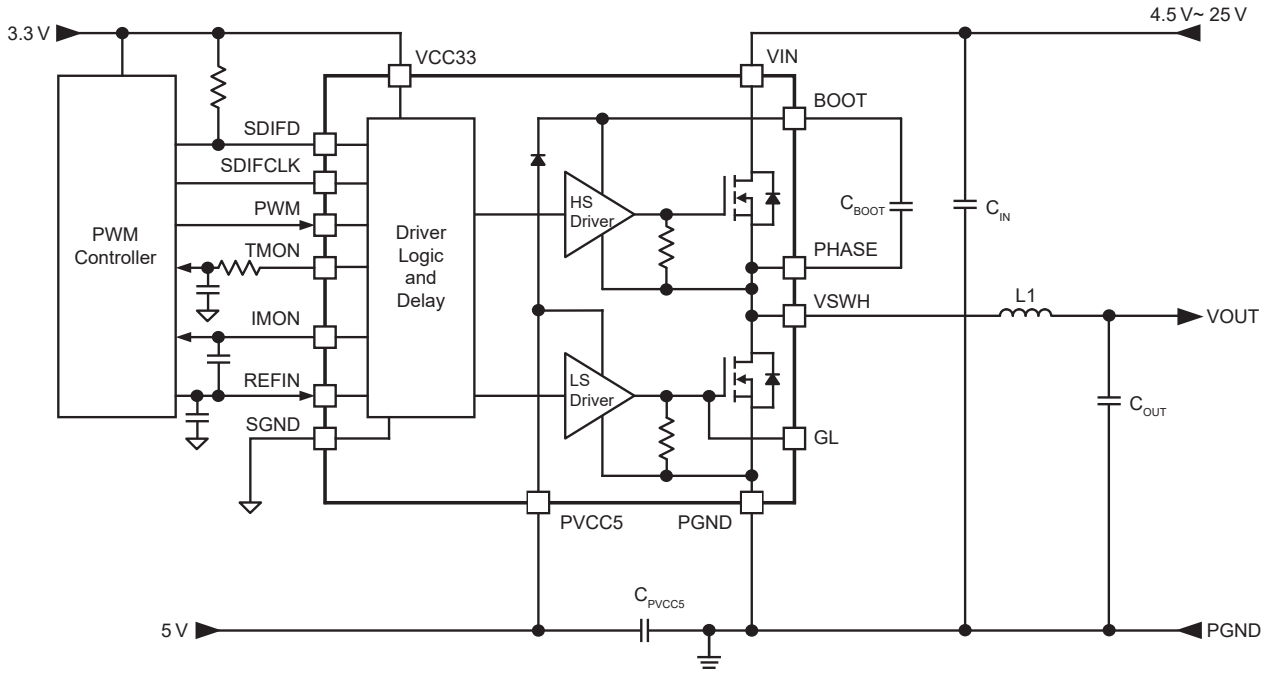
- 4.5 V to 25 V power supply range
- 60 A continuous output current
  - Up to 80 A for 10 ms on pulse
  - Up to 120 A for 10 µs on pulse
- Optimized for switching frequency up to 1 MHz
- Integrated current monitor output signal
- Integrated temperature monitor output signal
- Fault Indicator
- VCC33 and PVCC5 Under-Voltage Lockout (UVLO)
- Zero Current Detect Function
- Over Temperature Protection
- Standard 5 mm x 5 mm QFN-30L package

Applications

- Notebook computer
- Graphic card
- Communications Infrastructure

Green Product

Typical Application

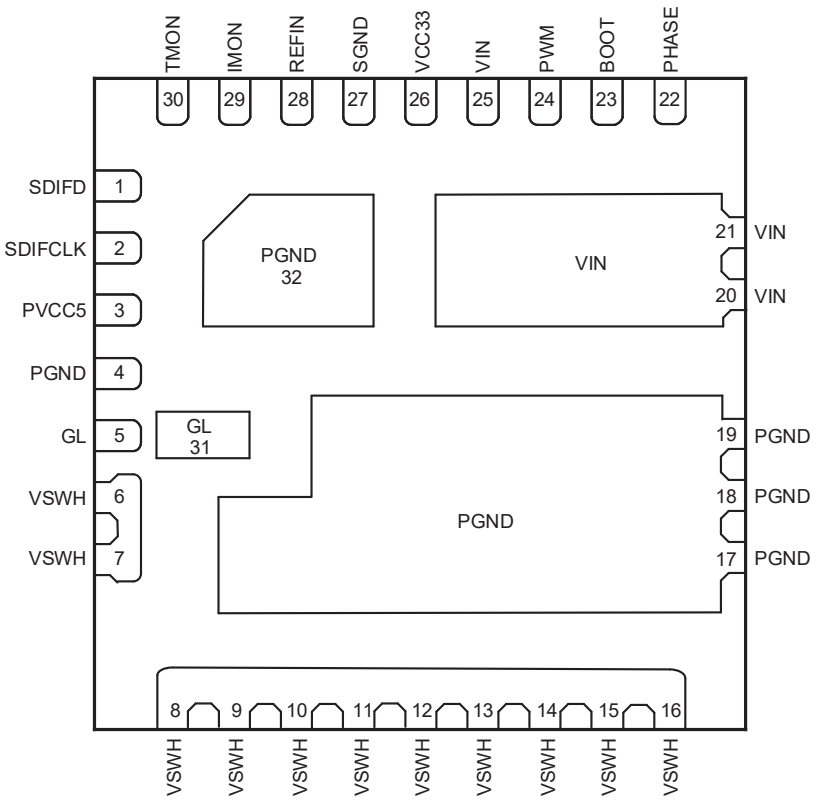


Ordering Information

Part Number	AmbientTemperature Range	Package	Environmental
AOZ52371QI	-40°C to +125°C	QFN5x5-30L	RoHS

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



QFN5X5-30L
Top View

Pin Description

Pin Number	Pin Name	Pin Function
1	SDIFD	Serial Digital Interface data input and output. Connect 1 kΩ to 3.3 V.
2	SDIFCLK	Serial Digital Interface clock input.
3	PVCC5	5 V Power Rail for High-Side and Low-Side MOSFET. Place a high quality low ESR ceramic capacitor (~ 1 µF / X7R) directly between PVCC5 and PGND (Pin 4).
4, 32	PGND	Power Ground for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1 µF directly between PGND and PVCC5 (Pin 3).
5, 31	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET.
17, 18, 19	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
20, 21, 25	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
22	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 23).
23	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100 nF ceramic capacitor between BOOT and the PHASE (Pin 22).
24	PWM	PWM input signal from Controller IC. This input is compatible with 3.3 V Tri-State logic level.
26	VCC33	3.3 V Bias for Internal Logic Blocks. Place a high quality low ESR ceramic capacitor (~ 1 µF / X7R) directly between VCC33 and SGND (Pin 27).
27	SGND	Signal Ground.
28	REFIN	Input for external reference voltage for IMON (Pin 28). This voltage should be between 0.8 V and 1.3 V. Connect this pin to the appropriate current sense input of the controller. Place a low ESR ceramic capacitor (~ 0.1 µF) from REFIN to SGND (Pin 27).
29	IMON	Current Monitor output signal referenced to REFIN (Pin 28). This pin is pulled high to VCC33 to indicate an over-temperature and/or PVCC5 UVLO fault. This pin is pulled to REFIN (Pin 28) to indicate VCC33 UVLO condition. Connect the IMON output to the appropriate current sense input of the controller. No more than 56 µF capacitance can be directly connected across the IMON and REFIN.
30	TMON	Temperature Monitor output signal. For multiphase, the TMON pins can be connected together as a common bus. The highest voltage indicating highest temperature is sent to the controller. No more than 470 pF total capacitance can be directly connected across TMON and SGND (Pin 27). Higher capacitance is allowed with a series resistor, such as 1 kΩ for a 100 nF load.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (PVCC5)	-0.3 V to 6 V
Low Voltage Supply (VCC33)	-0.3 V to 4.3 V
High Voltage Supply (VIN)	-0.3 V to 30 V
Control Inputs (PWM, SDIFD, SDIFCLK, REFIN)	-0.3 V to (VCC33+0.3 V)
Output (TMON, IMON)	-0.3 V to (VCC33+0.3 V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3 V to 33 V
Bootstrap Voltage Transient (1) (BOOT-PGND)	-8 V to 40 V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3 V to 6 V
BOOT Voltage Transient (1) (BOOT-PHASE/VSWH)	-0.3 V to 9 V
Switch Node Voltage DC (PHASE/VSWH)	-0.3 V to 30 V
Switch Node Voltage Transient (1) (PHASE/VSWH)	-8 V to 38 V
Low-Side Gate Voltage DC (GL)	(PGND-0.3 V) to (PVCC5+0.3 V)
Low-Side Gate Voltage Transient (2) (GL)	(PGND-2.5 V) to (PVCC5+0.3 V)
VSWH Current DC	60 A
VSWH Current 10 ms Pulse	80 A
VSWH Current 10µs Pulse	120 A
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
ESD Rating (3)	±2 kV HBM

Notes:

1. Peak voltages can be applied for 10 ns per switching cycle.
2. Peak voltages can be applied for 20 ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precaution is required. Human body model rating: 1.5 Ω in series with 100 pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	4.5 V to 25 V
Low Voltage Supply (VCC33)	3.135 V to 3.465 V
MOSFET Driver Supply (PVCC5)	4.75 V to 5.25 V
Control Inputs (PWM, SDIFD, SDIFCLK, REFIN)	0 V to VCC33
Output (TMON, IMON)	0 V to VCC33
Operating Frequency	200 kHz to 1 MHz

Electrical Characteristics[4]

T_J = 25°C to 125°C. Typical values reflect 25°C ambient temperature; VIN = 12V, VCC33 = 3.3V, PVCC5 = 5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General						
V_{IN}	Power Stage Power Supply		4.5		25	V
V_{PVCC5}	Low Voltage Driver Supply		4.75		5.25	V
V_{VCC33}	Low Voltage Controller Supply		3.135		3.465	V
$R_{\Theta JC}$ [5]	Thermal Resistance	PCB Temp = 100°C		2.5		°C/W
$R_{\Theta JA}$ [5]		Fsw = 300kHz, VOUT = 1V AOS Demo Board		12.5		°C/W
Input Supply and UVLO						
V_{PVCC5_UVLO}	PVCC5 Under-Voltage Lockout	PVCC5 Rising	3.90	4.20	4.45	V
V_{PVCC5_HYST}		PVCC5 Hysteresis		325		mV
V_{VCC33_UVLO}	VCC33 Under-Voltage Lockout	VCC33 Rising	2.50	2.75	2.95	V
V_{VCC33_HYST}		VCC33 Hysteresis		275		mV
V_{VCC33_BO}	VCC33 Brownout	VCC33 > Max (V_{PWM_H})	2.95	3.10	3.20	V
t_{VCC33_DEL}	VCC33 Power On Delay	From VCC33 UVLO release		220		µs
I_{VCC33}	Control Circuit Bias Current	PWM = 1.65 V		5		µA
		PWM = 300 kHz		1.6		mA
I_{PVCC5}	Drive Circuit Operating Current	PWM = 1.65 V		8		µA
		PWM = 300 kHz		10		mA
PWM Input						
V_{PWM_H}	PWM Logic High Input Voltage	PWM Rising	2.65			V
V_{PWM_L}	PWM Logic Low Input Voltage	PWM Falling			0.60	V
V_{TRI}	PWM Tri-State Window		1.20		2.20	V
SDIFCLK and SDIFD Input						
$V_{SDIFCLK\_H}$	SDIFCLK Logic High Input Voltage		1.90	1.725		V
$V_{SDIFCLK\_L}$	SDIFCLK Logic Low Input Voltage			1.275	1.10	V
$V_{SDIFCLK\_HYS}$	SDIFCLK Logic Hysteresis Voltage			450		mV
V_{SDIFD_H}	SDIFD Logic High Input Voltage		1.90	1.725		V
V_{SDIFD_L}	SDIFD Logic Low Input Voltage			1.275	1.10	V
V_{SDIFD_HYS}	SDIFD Logic Hysteresis Voltage			450		mV
V_{SDIFD_OUT}	SDIFD Low Output Voltage	I_{SDIFD} = 1mA		0.2		V

Electrical Characteristics[4]

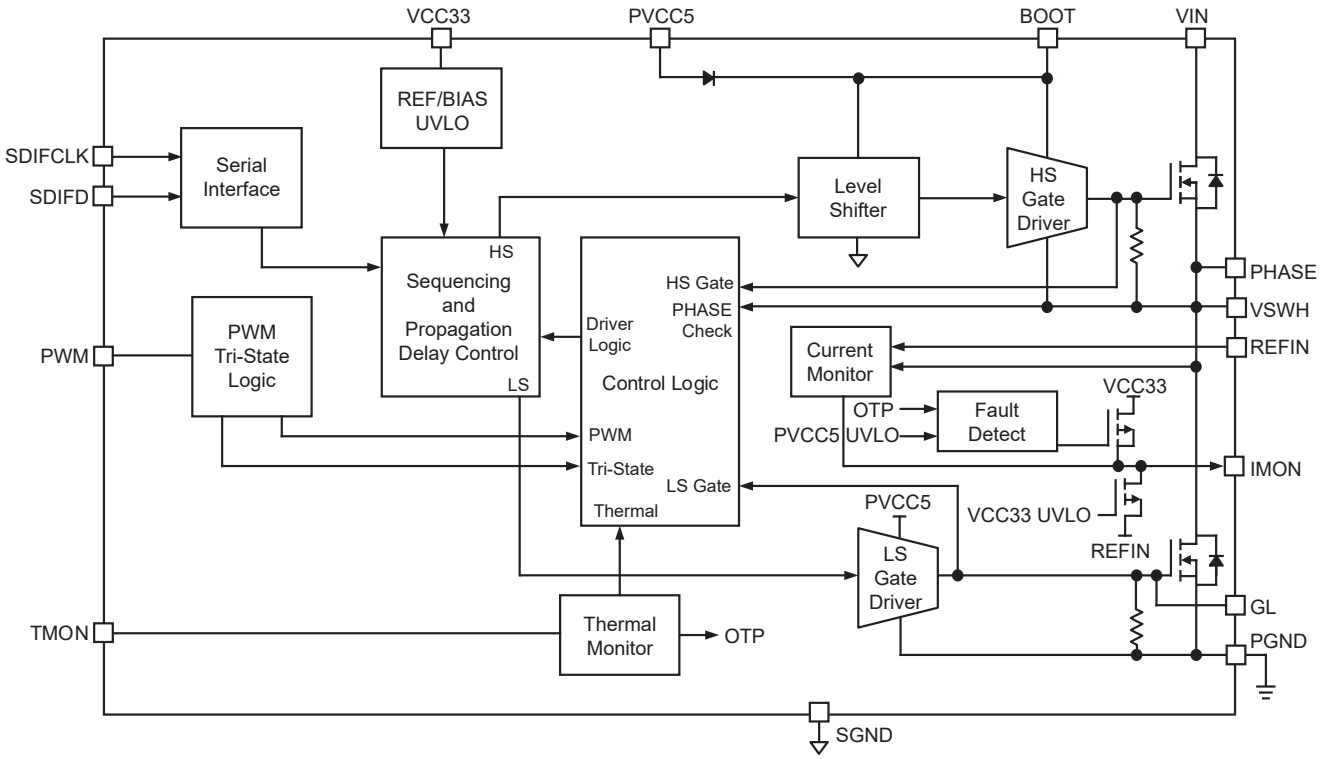
T_J = 25°C to 125°C. Typical values reflect 25°C ambient temperature; VIN = 12 V, VCC33 = 3.3 V, PVCC5 = 5 V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Current Monitor IMON						
V_{REFIN}	REFIN Voltage Range		0.8	1.2	1.3	V
A_{IMON_GAIN}	IMON Current Gain Accuracy	IOUT ≥ 10A, 0°C < T_J < 125°C		± 3		%
		IOUT ≥ 10A, -40°C < T_J < 0°C		± 5		%
V_{IMON_HOT}	IMON High at Over Temperature			3.3		V
Temperature Monitor TMON						
T_{OTP}	Over Temperature Protection Threshold			150		°C
T_{OTP_HYST}	Over Temperature Protection Threshold Hysteresis			15		°C
A_{TMON_SLP}	TMON Temperature Coefficient Slope			8		mV/°C
V_{TMON_25C}	TMON Voltage at 25 °C	$V(T_J)$ = 0.6 V + (8 mV * T_J)		0.8		V
Gate Driver Timings						
t_{PDLU}	PWM to High-Side Gate Delay	PWM: H → L to VSWH: H → L		25		ns
t_{PDLL}	PWM to Low-Side Gate Delay	PWM: L → H to GL: H → L		30		ns
t_{PDHU}	Low-Side to High-Side Gate Deadtime	GL: H → L to VSWH: L → H		6		ns
t_{PDHL}	High-Side to Low-Side Gate Deadtime	VSWH: H → 1 V to GL: L → H		6		ns
t_{TSSHD}	Tri-State Shutdown Delay	PWM: H → V_{TRI} to GL: H → L and PWM: L → V_{TRI} to VSWH: H → L		45		ns
t_{TSEXIT}	Tri-State Exit Propagation Delay	PWM: V_{TRI} → H to VSWH: L → H		70		ns
		PWM: V_{TRI} → L to GL: L → H		25		ns

Notes:

4. All voltages are specified with respect to the corresponding SGND pin
5. Characterization value. Not tested in production.

Functional Block Diagram



Timing Diagram

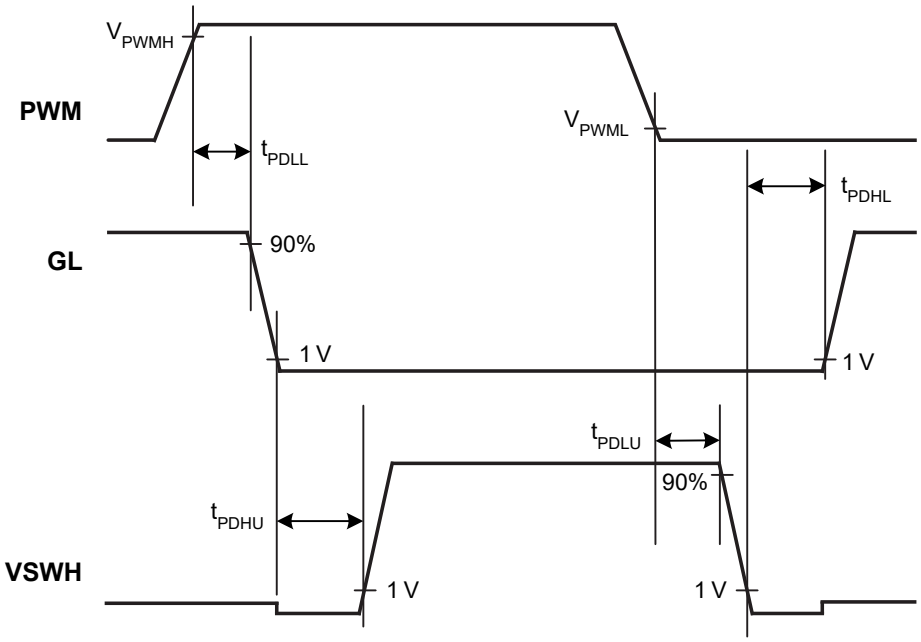


Figure 1. PWM Input Timing Diagram

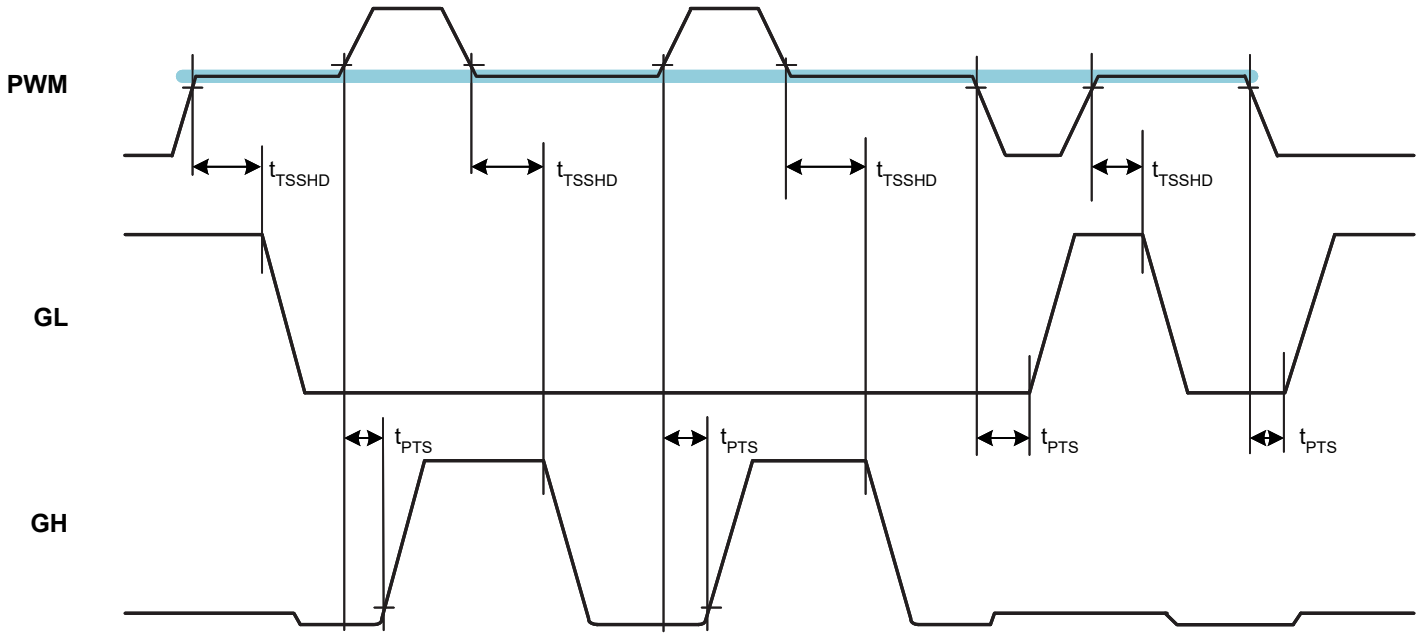


Figure 2. PWM Tri-State Hold Off and Exit Timing Diagram

Typical Characteristics

T_A = 25°C, VIN = 12V, PVCC5 = 5V, VCC33 = 3.3V, unless otherwise specified.

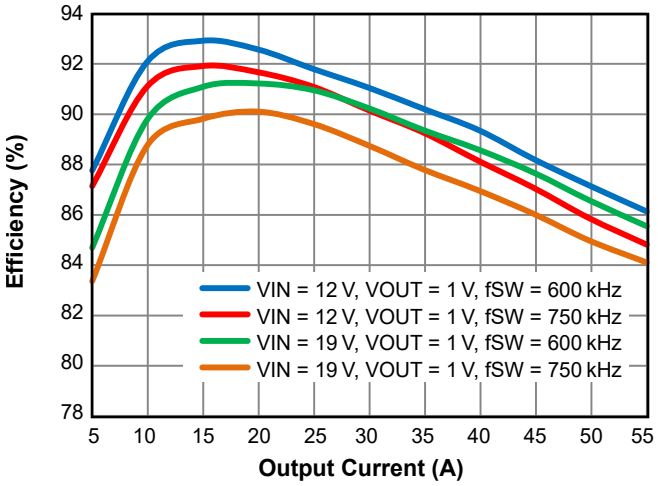


Figure 3. Efficiency vs Load Current

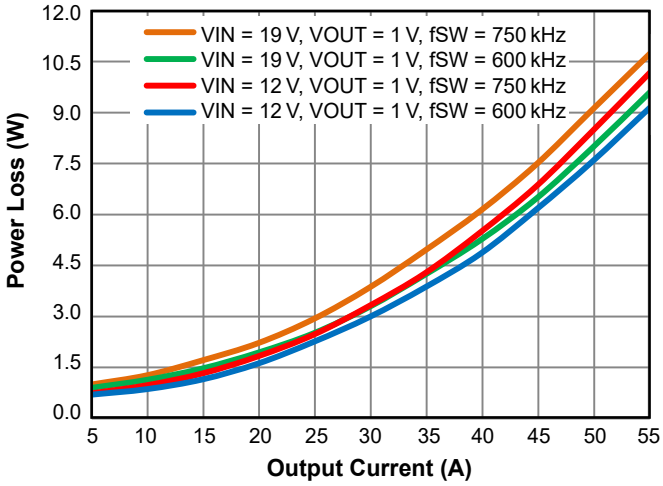


Figure 4. Power Loss vs Load Current

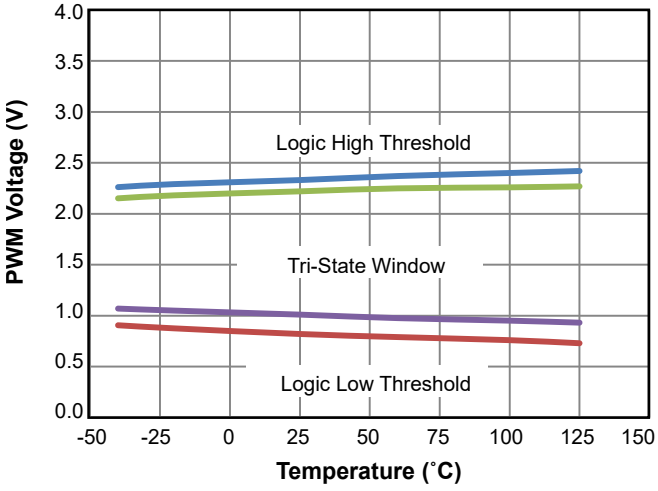


Figure 5. PWM Threshold vs. Temperature

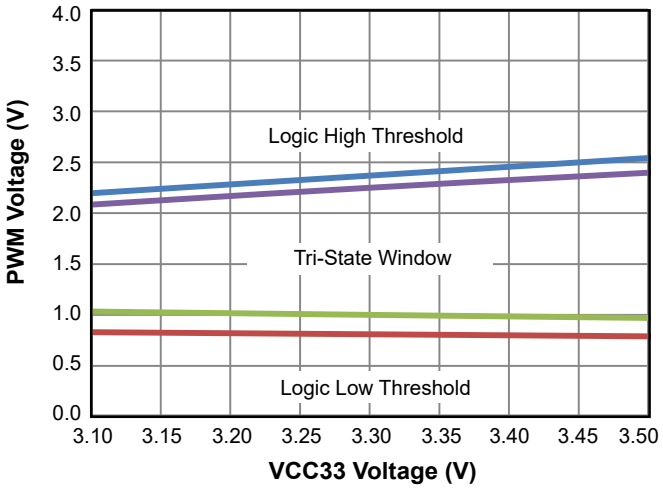


Figure 6. PWM Threshold vs. VCC33

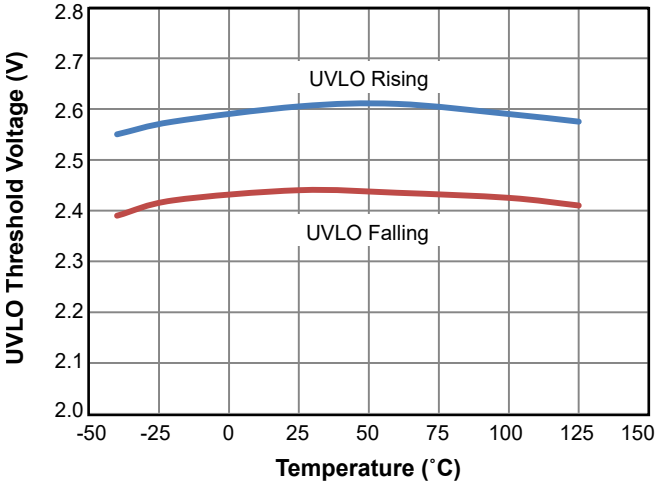


Figure 7. VCC33 ULVO Threshold vs. Temperature

Typical Characteristics

T_A = 25°C, VIN = 12 V, PVCC5 = 5 V, VCC33 = 3.3 V, unless otherwise specified.

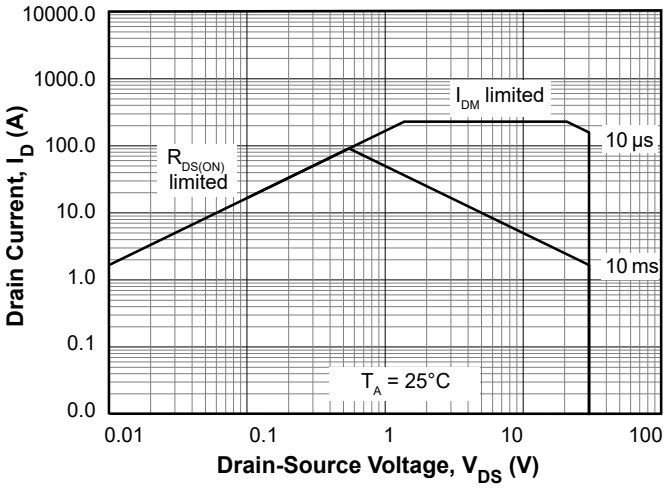


Figure 8. High-Side MOSFET SOA

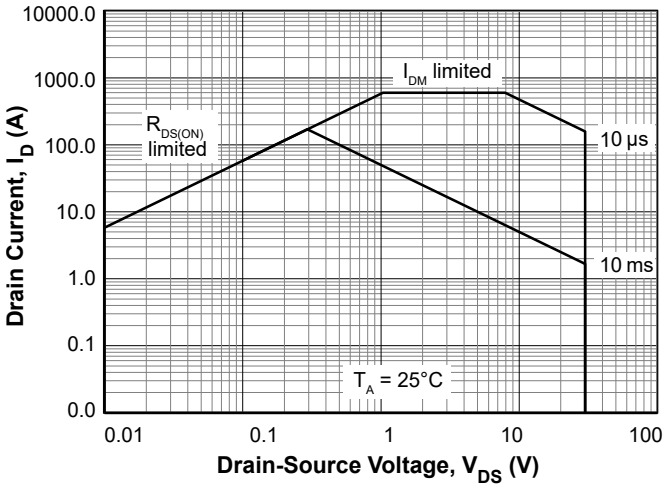


Figure 9. Low-Side MOSFET SOA

Detailed Description

AOZ52371QI is a fully integrated smart power module designed to work over an input voltage range of 4.5 V to 25 V with 5 V supplies for gate drive and 3.3 V supplies for internal control circuits. A number of industry leading features are employed in this smart power stage module such as IMON outputs Low-Side MOSFET current information. Other features such as thermal reporting, High-Side MOSFET device short, Bias Voltage (VCC33 and PVCC5) Under-Voltage Lockout (UVLO), and Low-Side MOSFET operation control for light load efficiency, are available to make the AOZ52371QI a highly versatile power module. The High-Side and Low-Side MOSFETs are combined in one package with the pin outs optimized for power routing with minimum parasitic inductance. The MOSFETs are individually tailored for efficient operation as either high-side or low-side switches in a low duty cycle synchronous buck converter. In addition, a high current driver is also included in the package which minimizes the gate drive loop resulting in extremely fast switching.

Power-On Reset (POR)

The VCC33 voltage rise is monitored during initial start-up. If the rising VCC33 voltage exceeds 2.75 V (typical), and the rising PVCC5 voltage exceeds 4.2 V, normal operation of the driver is enabled after correct initialization by the controller. The PWM signals are passed through to the gate drivers, the TMON output is valid and the (IMON-REFIN) output starts at zero, and becomes valid on the first Low-Side MOSFET gate (GL) signal. The driver operation is disabled if either VCC33 or PVCC5 drops below its falling threshold.

Tri-State PWM Input

The AOZ52371QI supports a 3.3 V PWM Tri-State input and is compatible with digital multiphase controllers and other control ICs using 3.3 V PWM logic (Controller's VCC and SPS's VCC33 should share the same rail). If the pin is pulled into the Tri-State window and remains there for a set hold-off time, the driver forces both MOSFETs to their off states. When the PWM signal moves outside the shutdown window, the driver immediately resumes driving the MOSFETs according to the PWM commands. This feature is used by the PWM controllers as a method of forcing both MOSFETs off.

There is no internal resistor divider to drive PWM to the Tri-State voltage. The multiphase controller must externally drive PWM to the Tri-State voltage (V_{TRI}) and not leave PWM at high impedance state.

Bootstrap Function

The AOZ52371QI features an internal NFET that is controlled to function as a bootstrap diode. Place a high-quality ceramic capacitor in close proximity across the BOOT and VSWH pins. The bootstrap capacitor can range between 0.1 µF and 0.22 µF (0402~0603 and X5R~X7R) for normal buck switching applications. A boot resistor can be used in series with the capacitor as MOSFET performance and operating conditions dictate.

Shoot-Through Protection

Before PVCC5 and VCC33 POR, the under-voltage protection (UVLO) function is activated and both GH and GL are held active low (High-Side and Low-Side MOSFETs are off). If the driver has no bias voltage applied (either VCC33 or PVCC5 are missing) and is unable to actively hold the MOSFETs off, an integrated 20 kΩ resistor from the High-Side MOSFET gate to source helps keep the High-Side MOSFET device in its off state. This shoot-through protection can be especially critical in applications in which the input voltage rises before the AOZ52371QI VCC33 and PVCC5 supplies.

After POR and a 220 µs delay, the PWM signal controls both High-Side and Low-Side MOSFETs.

During switching operation, the AOZ52371QI dead time is optimized for high efficiency and ensures that simultaneous conduction of both MOSFETs cannot occur.

Serial Digital Interface (SDIF) Bus

The SDIF is a two-wire bus consisting of a clock and data line, designed for communication between Renesas Digital Multiphase Controllers and compatible Smart Power Stages. SDIFCLK operates unidirectionally, from controller to SPS, in a push-pull configuration that is held low when not in use. SDIFD is a bi-directional line configured as an open drain pin connected to VCC33 through a single 1 kΩ pull-up resistor placed near the controller. Typically, the bus operates at 1 MHz with frequencies up to 2 MHz allowed.

During operation, SDIF is used primarily to optimize the system level power consumption by commanding SPS into one of several power states based on CPU activity. The bus also gives permission for a SPS to report its temperature on the TMON back to the controller. This allows for individual power stage temperatures rather than only the maximum temperature to be monitored. Additionally, the controller will read calibration data from the SPS at startup to optimize the inductor current information reported on the IMON pin.

Current Monitoring

The Low-Side MOSFET current is monitored and a signal proportional to that current is the output on the IMON pin (relative to the REFIN pin) without thermal and VCC33 compensations, which are done inside the controller after SDIF bus polls the information from SPS. Connect the IMON and REFIN pins to the appropriate current sense input pin of the controller. This method does not require external R_{SENSE} or DCR sensing of the inductor current.

Figure 10 depicts the low-side current sense concept. After the falling edge of the PWM, there are two delays: one that represents the expected propagation delay from PWM to GH/VSWH and a second blanking delay to allow time for the transition to settle; typical total time is ~350 ns. The IMON output (within controller) approximates the actual I_L waveform.

The High-Side MOSFET current is not monitored in the same way, so no valid measured current is available while PWM is high (including the short delays before and after). During this time, the IMON outputs the last valid Low-Side MOSFET current before the sampling stopped. On start-up after POR, the IMON outputs zero (relative to REFIN, which represents zero current) until the switching begins and the current can be properly measured.

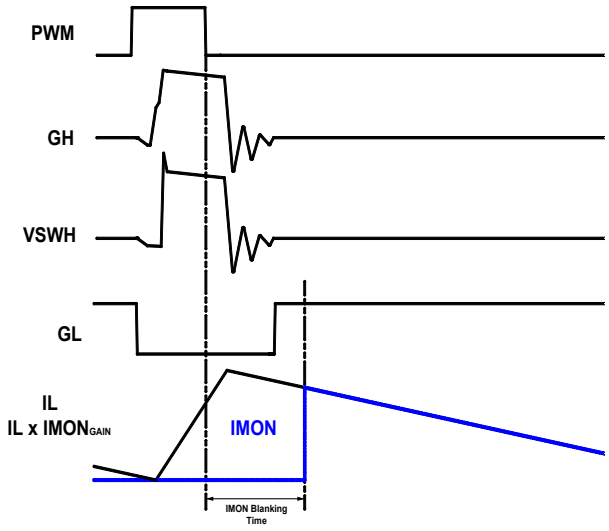


Figure 10. IMON Signal Reconstruction of Inductor Current

Thermal Monitoring

The AOZ52371QI monitors its internal temperature and provides a signal proportional to that temperature on the TMON pin. TMON has a voltage of 600 mV at 0°C and reflects temperature at 8 mV/°C. The TMON output is valid after the proper command from the controller over the SDIF bus.

In a multiphase, or multi-rail, application each TMON pin will be tied together and a single signal is routed back to the controller. However, each AOZ52371QI will only report its temperature after the appropriate command is sent over the SDIF bus. This allows for individual phase temperature readings instead of simply the maximum temperature at any given time.

If an over-temperature fault occurs, the IMON pin is pulled high to 3.3 V.

Thermal Protection

If the internal temperature exceeds the over-temperature trip point (+150°C typical), the IMON pin is pulled high to 3.3 V and no other action will be taken. The IMON remains in the fault mode until the junction temperature drops below +135°C (typical); at that point, the IMON resumes normal operation.

Fault Reporting

Over-temperature detection pulls the IMON pin high to 3.3 V, so that the PWM controller quickly recognizes it as out of the normal range.

The fault reporting and respective SPS response are summarized in Table 1.

Table 1. Fault Protection Summary Table

Fault Event	IMON	Response
Over Temperature	3.3 V	IMON fault flag is raised but SPS continues switching until controller provides further action.
PVCC5 UVLO	3.3 V	Switching stops while in UVLO. When PVCC5 voltage is above POR for 210 µs: GH and GL follow PWM TMON is valid IMON-REFIN is valid after GL first goes low.
VCC33 UVLO	IMON - REFIN = 0 V	Switching stops while in UVLO. SPS waits for controller to clear fault flag via SDIF Bus.
VCC33 Brownout	3.3 V	Switching stops. SPS waits for controller to clear fault flag via SDIF Bus.

Layout Guideline

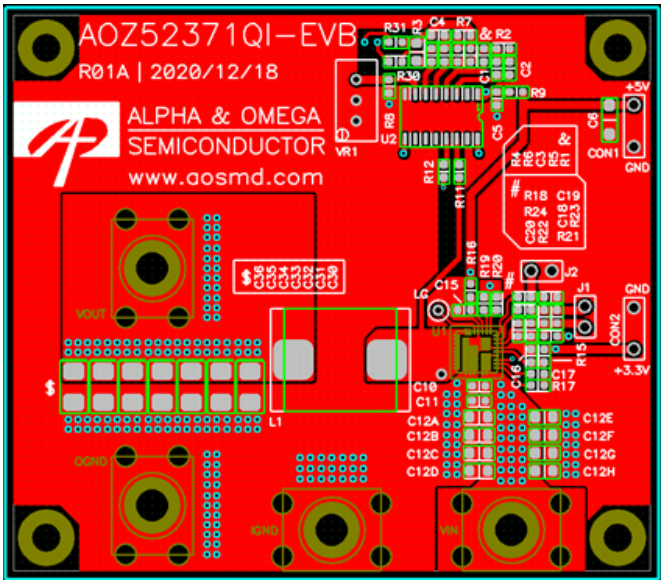


Figure 11. Evaluation Board

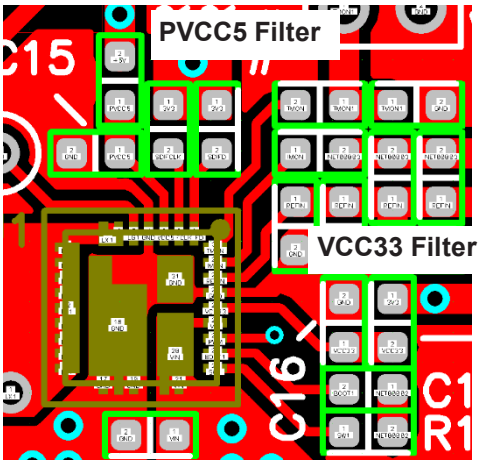


Figure 12. VCC33 and PVCC5 Input Filters

- The VCC33 and PVCC5 input ceramic capacitor should be placed as close as possible to the IC. It is recommended to place two independent R/C filters for each.
- VCC33 capacitor should be placed between VCC33 and the next adjacent SGND to achieve best noise filtering.
- PVCC5 capacitor should be placed between PVCC5 and the nearest PGND power plate to provide maximum instantaneous driver current for low-side MOSFET during switching cycle. It also can connect PGND to inner layers through VIAs.
- The capacitor size could be adopted as either 0603 or 0402. However, please keep the effective capacitance no less than 1 µF in any condition.

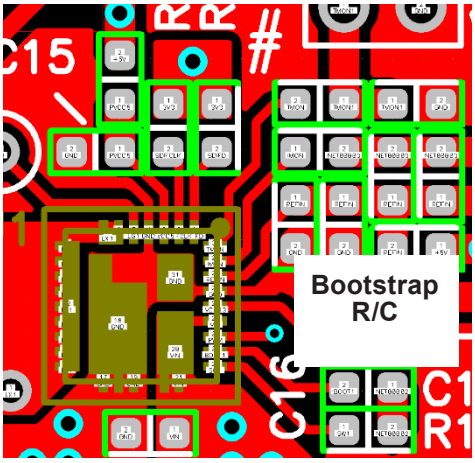


Figure 13. Bootstrap Resistor and Capacitor

- The bootstrap resistor and capacitor need to be placed as close as possible to IC, directly connect between PHASE and BOOT.

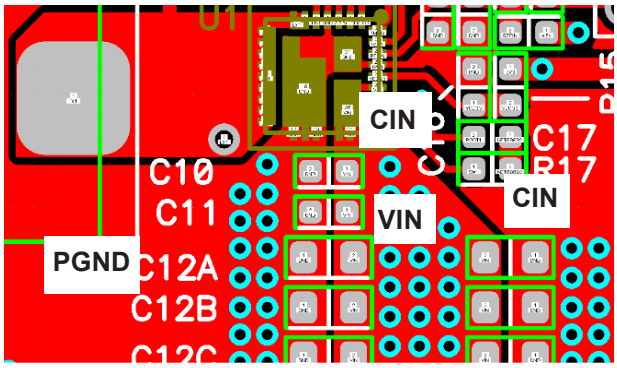


Figure 14. VIN Power Planes and Input Capacitors

- Place VIN and PGND planes as shown in Figure 14.
- Ceramic capacitors should be placed directly between VIN and PGND. Moreover, place these capacitors closer to the SPS for the best VIN power path decoupling.
- At least equivalent 20 µF should be reserved for each phase SPS.
- Smaller capacitance values, placed closer to the SPS VIN/PGND pin(s), results in better high frequency noise absorbing.

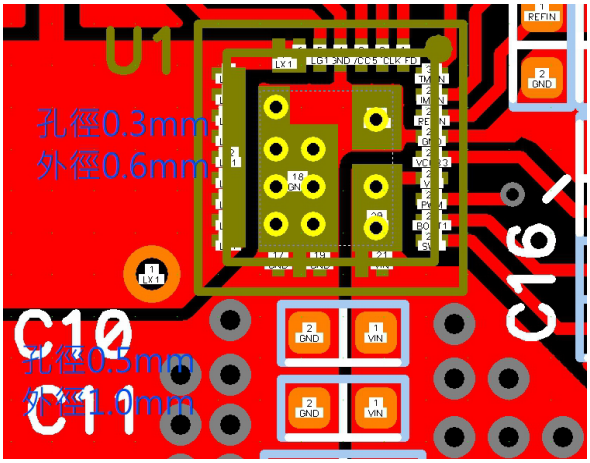


Figure 15. VIAs for Exposed Pads

- To achieve better thermal performance, additional VIAs can be placed under VIN and PGND exposed pads.
- 0.3 mm VIAs for exposed pads are the recommended via sizes. As shown in Figure 15, 7 VIAs and 2 VIAs are recommended for PGND and VIN exposed pads, respectively.

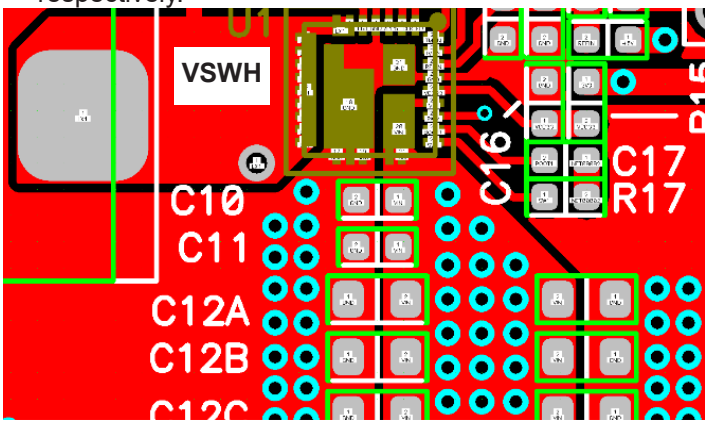


Figure 16. VSWH Plane

- VSWH is a high voltage swing node and behaves as noise antenna.
- Place the inductor next to VSWH pins and make the VSWH plane wide and short to minimize the switching noise propagation.
- If a snubber network is required, place the resistor and capacitor between VSWH and PGND planes, directly. The R/C network can be placed at the bottom.

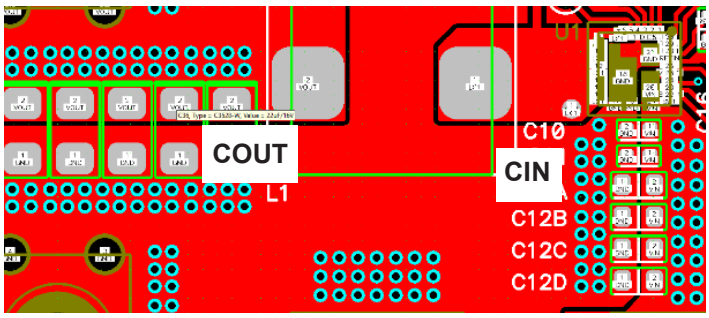


Figure 17. Grounding and VIAs

- It is recommended to make a single connection between SGND and PGND which can be made on the top layer or through VIA to inner layers.
- It is recommended to make the entire first inner layer (below top layer) as grounding plane, at least.
- In order to minimize the parasitic loop inductance and resistance, place more VIAs around the input and output capacitor soldering pads.

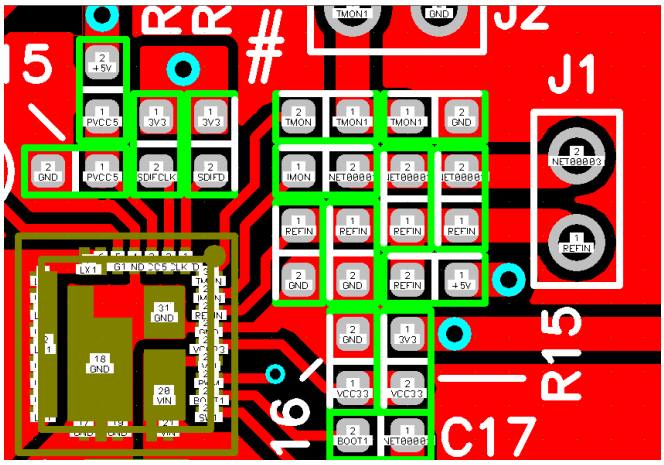
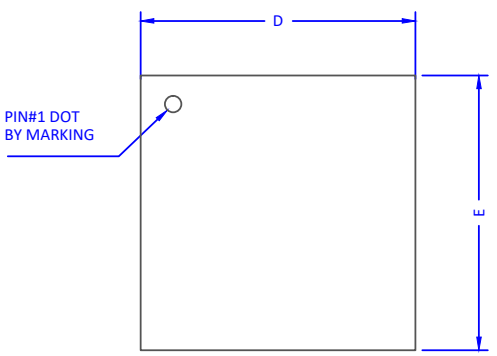


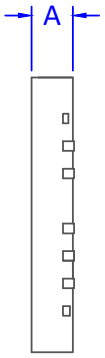
Figure 18. Signal Trace

- PWM, SDIFD and SDIFCLK all are high speed digital signals. Route these traces from pins directly.
- Do not cross these traces with any power nodes on any layers.
- IMON and REFIN are current monitor signal output.
- In order to prevent common mode noise and interference, it is better place IMON and REFIN in-parallel or shield with GND.

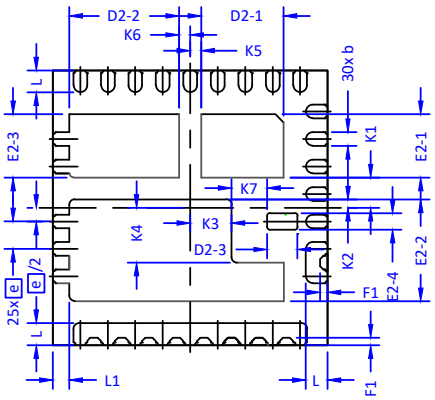
Package Dimensions, QFN5x5-30L



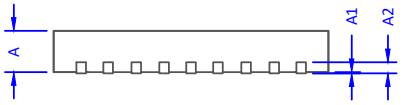
TOP VIEW



SIDE VIEW

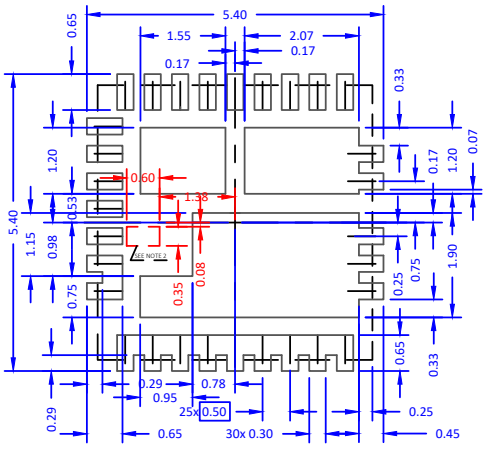


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



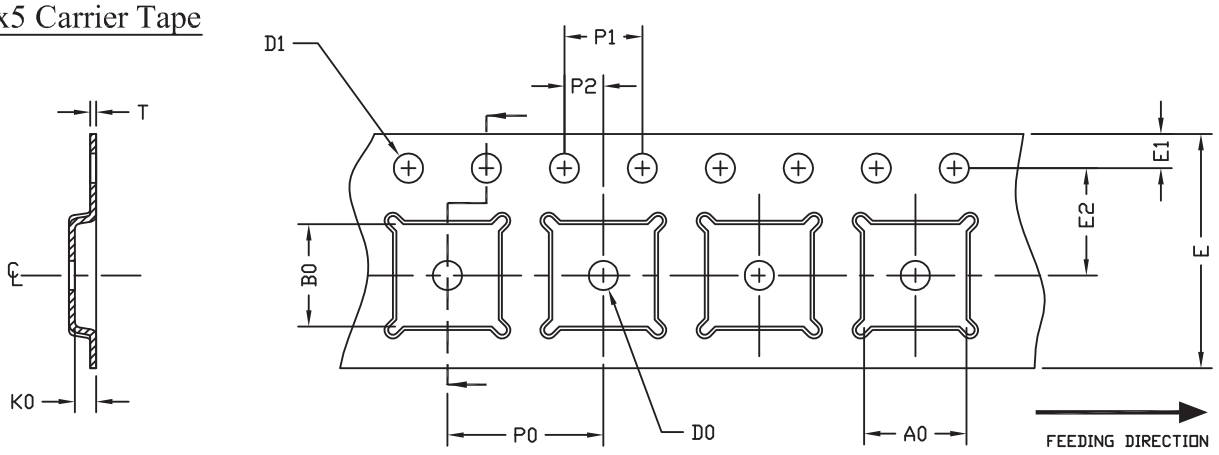
UNIT: mm

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 REF			0.008REF	
b	0.20	0.25	0.30	0.008	0.010	0.012
D	4.90	5.00	5.10	0.193	0.197	0.201
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.95	2.00	2.05	0.077	0.079	0.081
D2-3	0.50	0.55	0.60	0.020	0.022	0.024
e		0.50 BSC			0.020 BSC	
E	4.90	5.00	5.10	0.193	0.197	0.201
E2-1	1.10	1.15	1.20	0.043	0.045	0.047
E2-2	1.80	1.85	1.90	0.071	0.073	0.075
E2-3	1.10	1.15	1.20	0.043	0.045	0.047
E2-4	0.25	0.30	0.35	0.010	0.012	0.014
F1	0.11	0.14	0.17	0.004	0.006	0.007
K1		0.55 ref.			0.022 ref.	
K2		0.15 ref.			0.006 ref.	
K3		0.75 ref.			0.030 ref.	
K4		1.00 ref.			0.039 ref.	
K5		0.20 ref.			0.008 ref.	
K6		0.20 ref.			0.008 ref.	
K7		0.65 ref.			0.026 ref.	
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.25	0.30	0.35	0.010	0.012	0.014

NOTE:
1. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. DOTTED OUTLINE IS GUIDELINE TO BE COMPATIBLE WITH INDUSTRY COMMON LAYOUT BUT NOT RECOMMENDED BY AOS.

Tape and Reel Dimensions, QFN5x5-30L

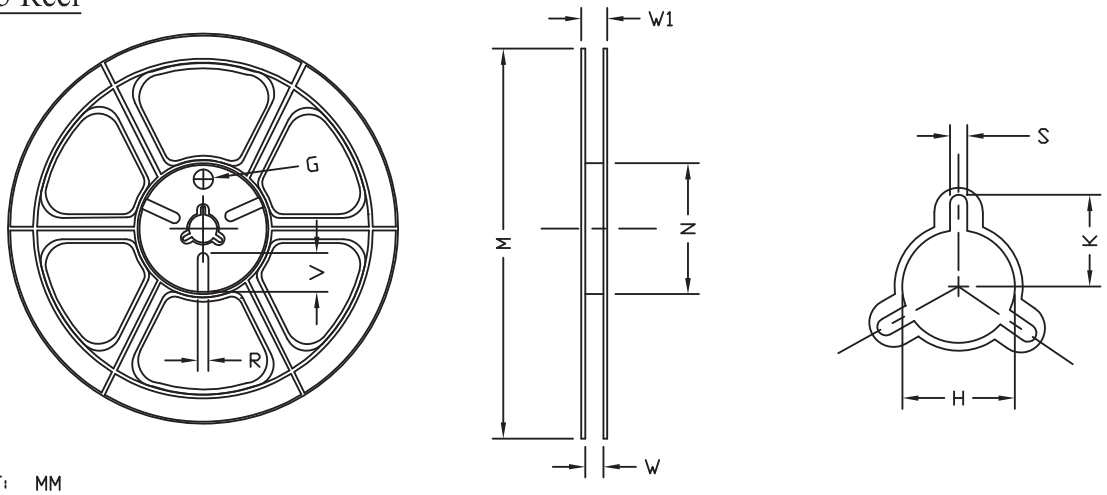
QFN5x5 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 $^{+0.1}_{-0.0}$	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

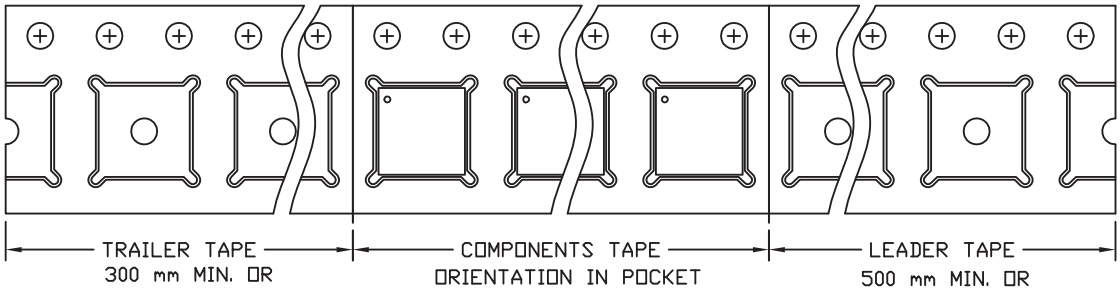
QFN5x5 Reel



UNIT: MM

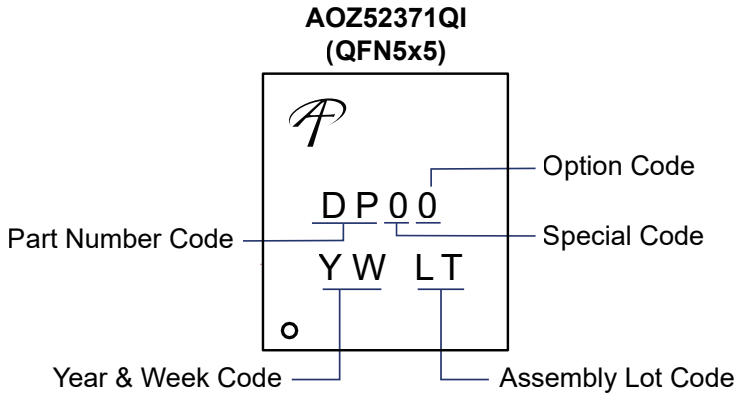
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 $^{+2.0}_{-0.0}$	17.0 $^{+2.6}_{-1.2}$	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

Leader / Trailer & Orientation



Unit Per Reel: 3000pcs

Part Marking



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.