AOZ13984/87DI

Evaluation Board User Guide

General Description

The AOZ13984DI and AOZ13987DI Evaluation Board (EVB) provides a platform to evaluate the AOZ13984DI and the AOZ13987DI ideal diode smart fuse switches. Both ICs feature output Short Circuit Protection (SCP), Ideal Diode True Reverse Current Blocking (IDTRCB) to completely eliminate reverse-current from VOUT to VIN of any magnitude at any frequency (including constant VOUT>VIN blocking).

True power ORing capability: multiple systems in parallel for increased power delivery or smooth transfer to a second power source when the first one turns off.

Features also include: programmable soft start time to control in rush current, Under Voltage Lock Out (UVLO), Over Voltage Protection (OVP) to protect VOUT from excessive VIN and Over Temperature Protection (OTP). FLTB pin (active low) reports OVP and OTP faults.

The ideal diode voltage drop / DC current / pulsed (10ms @ 2% duty cycle) current capabilities for the AOZ13984DI-02 and the AOZ13987DI-02 are 70mV/5.5A/15A and 35mV/8A/20A respectively. The EVB can operate from 3.4V to 22V input voltage. Figures 1 and 2 show pictures of the evaluation board.

Evaluation Board

Figure 1. Top View of AOZ13984/87DI EVB

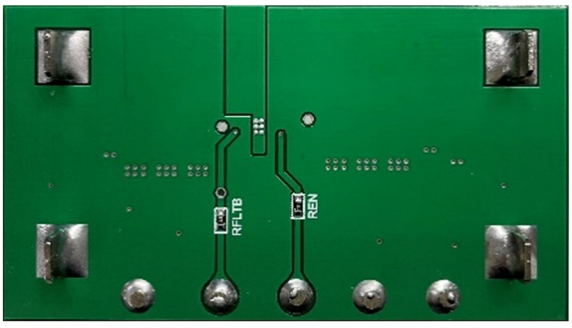


Figure 2. Bottom View of AOZ13984/87DI EVB

Evaluation Board Hardware

The EVB is 2oz, 2 layer board. The board schematic and the PCB layout are included in this document. The EVB has several connectors for quick input/output connections and test points for measurements. The on-board connectors and test points are listed below:

On-board Connectors and Test Points

Connectors	Descriptions
VIN	Input supply connector, connect to 3.4-22V power supply.
VOUT	Output Connector, connect an external load between this connector and the GND connector.
GND	Ground connectors.
VEN	Connector for the enable signal.
+5V	Connector for bias supply for FLTB pull up, connect to 3.3V-5.5V supply.
VFLTB	Test point for FLTB signal.

Quick Power Up Guide [1]

1. Ensure that the circuit is correctly connected to the power supply and load, refer to Figure 3 for proper setup.
2. Turn on the VIN and +5V power supplies.
3. Adjust the +5V power supply to 5V and VIN power supply to 12V. The output voltage should be approximately VIN when VIN>4V.
4. Adjust the load current, do not exceed 3A.

Note:
1. When testing SCP D3 (output Schottky diode) must be installed to avoid excessive negative voltage. The EVB does not come with D3 populated.

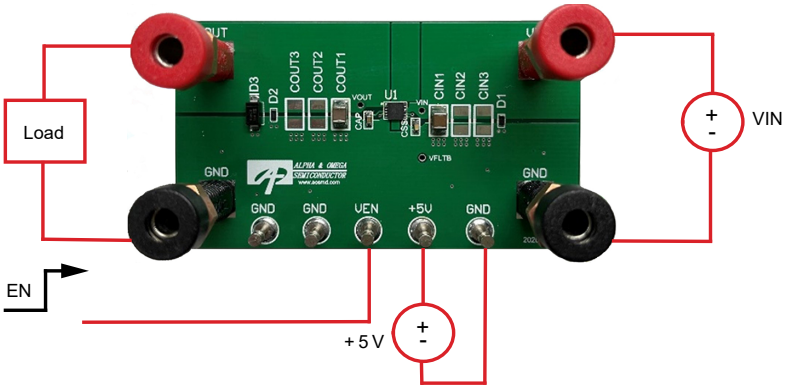
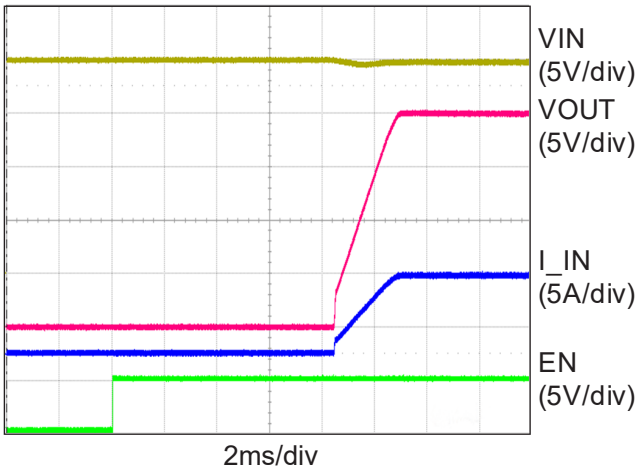


Figure 3. AOZ13984/87DI Evaluation Board Set Up

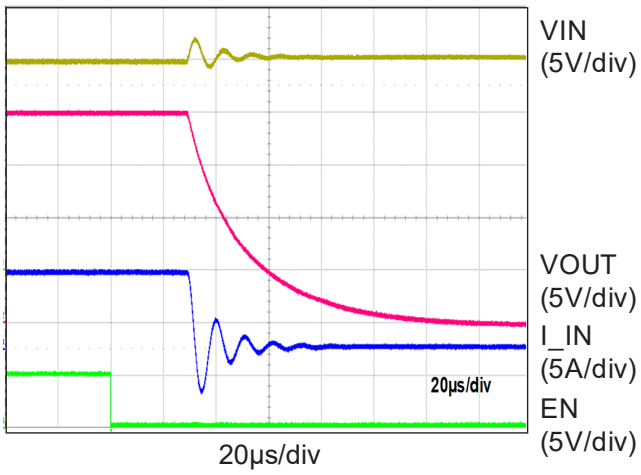
Typical Characteristics

T_A = 25 °C, V_{IN} = 20 V, EN = 5 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{SS} = 5.6 nF, C_{CAP} = 1 nF, unless otherwise specified.

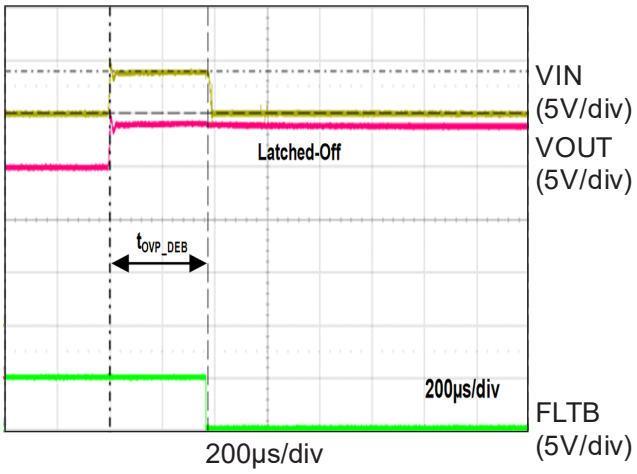
Power Up
(V_{IN} = 20 V)



Power Down
(V_{IN} = 20V)



Over Voltage Protection
(V_{IN} = 20 V)



Setting Soft-start Capacitor, C_{SS}

The AOZ13987DI integrates a SOA management to ensure safe operation during soft-start. During soft-start the output voltage linearly ramps up to the level of the input voltage in a controlled fashion. There are three factors to consider for a successful soft-start.

1. The current demand must not exceed the allowed current anytime during the soft-start. The current demand consists of two parts: (1) the current needed to charge the output capacitance (Cout*Vin/Soft-start-time) and (2) the load current (Vout(t)/Rout).

2. The current demand must not exceed the allowed current when the power switch closes. There is a delay from the beginning of soft-start to the closing of the power switch. The current demand when the power switch closes must not be more than the allowed current at that time.

3. The device must stay within the safe operating area (SOA) during soft-start. The current demand combined with the soft-start time must not violate the SOA. During soft-start the power switch absorbs energy. The linear start-up of a soft-start causes a significant voltage drop across the IC. This voltage drop combined with the current load causes the device to heat up.

The maximum current allowed during soft-start time increases with a decreased voltage drop from VIN to VOUT. During the soft-start time, the output capacitor, the output load and the input voltage should be considered to set the soft-start time so that the SOA management circuit doesn't interrupt the soft-start ramp.

A design tool is available to select C_{SS} based on application conditions for both AOZ13984 and AOZ13987

Once the soft-start time is determined, the corresponding soft-start capacitor can be calculated using the equations below:

$$C_{SS} = \left[\left(t_{ON} \right) x \left(\frac{24}{V_{IN}} \right) + 100 \right] x \; 0.0023$$

where C_{SS} is in nF and t_{ON} is in µs.

EVB Schematic

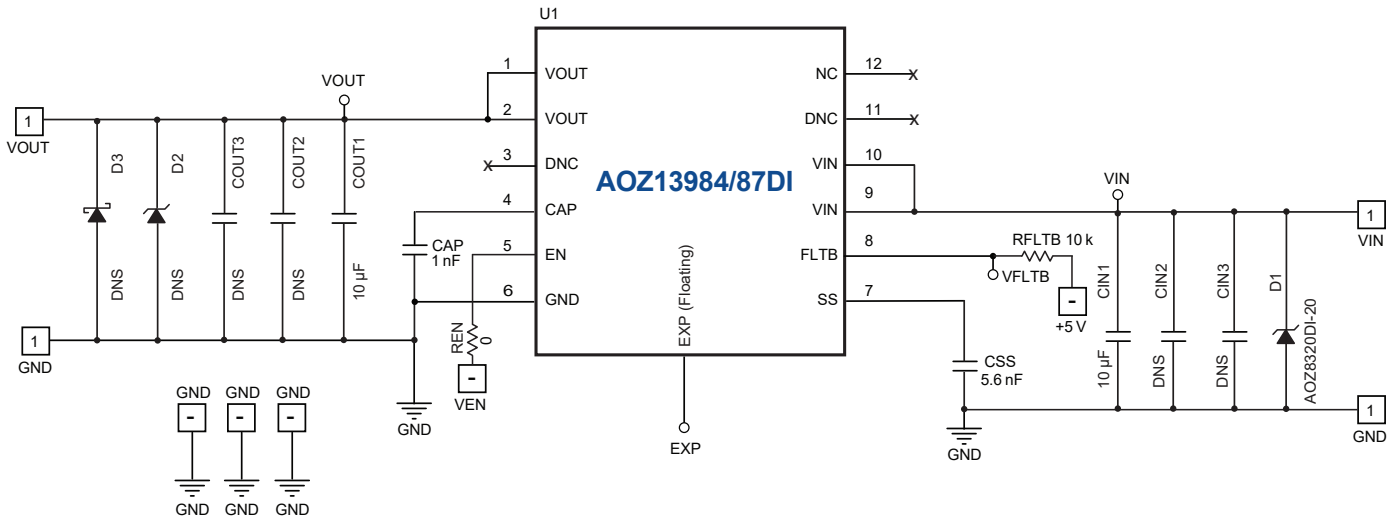


Figure 4. AOZ13984/87DI EVB Schematic

Bill of Materials

Designator	Type	Description	Size	Manufacturer	Qty
U1	Protection Switch	AOZ13984DI-02/AOZ13987DI-02	DFN3x3	AOS	1
CIN1	Capacitor, Ceramic	10 µF, 50 V, X5R	1206		1
CIN2,3	Capacitor, Ceramic	DNS	1206		0
COUT1	Capacitor, Ceramic	10 µF, 50 V, X5R	1206		1
COUT2,3	Capacitor, Ceramic	DNS	1206		0
CSS	Capacitor, Ceramic	5.6 nF, 25 V, X5R	0603		1
CAP	Capacitor, Ceramic	1 nF, 25 V, X5R	0603		1
D1	TVS	AOZ8320DI-20	DFN1.6x0.8	AOS	1
D2	TVS	DNS	DFN1.6x0.8		0
D3	Schottky Diode	DNS - DIODE SCHOTTKY 40 V 3A	SMA		0
RFLTB	Resistor	10 k, 1%, 1/10W	0603		1
REN	Resistor	0, 1%, 1/10W	0603		1

PCB Layout

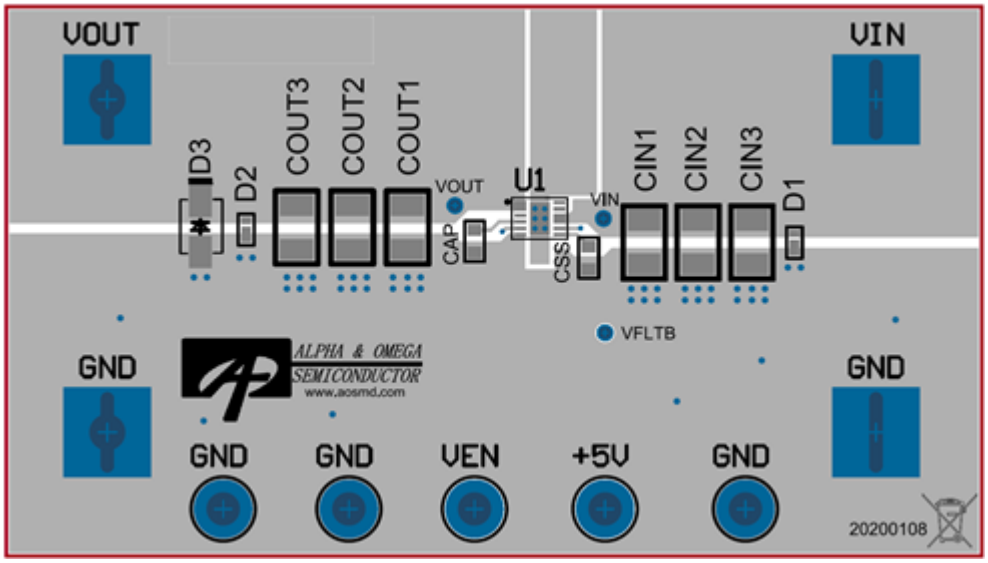


Figure 5. Top Layer

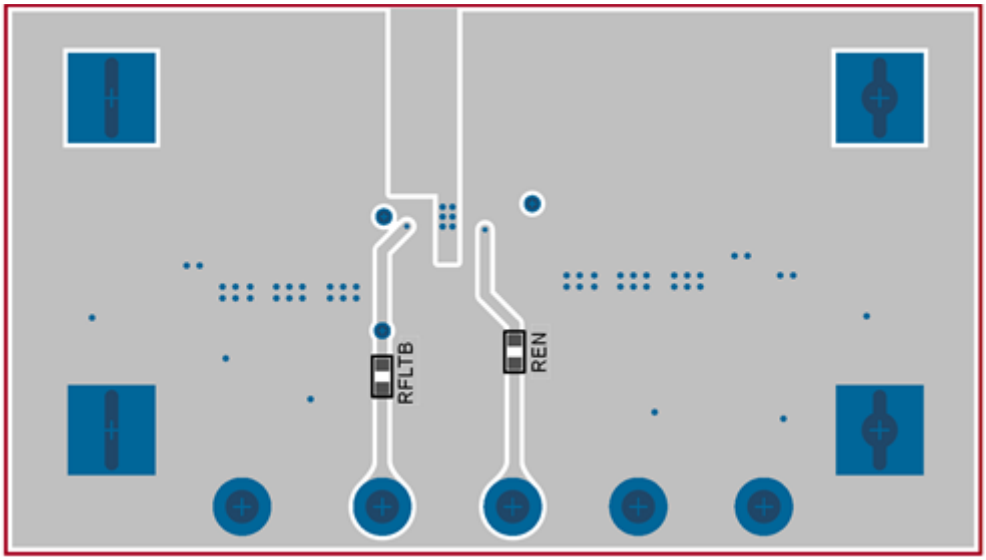


Figure 6. Bottom Layer

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