ALPHA & OMEGA SEMICONDUCTOR

AOZ71137QI

3 Rails 4+2+1 Hybrid Low PQ Intel IMVP 9.1/9.2 Controller

General Description

The AOZ71137QI is a high performance digital & analog hybrid multiphase buck controller designed in compliance with Intel IMVP8, 9, and 9.1/9.2 platform specifications. It provides three output rails (up to 4 + 2 +1) and supports 4 separate SVID domains: Up to 4 phases for core voltage domain (IA), 2 phases for graphics voltage domain (GT) and 1 phase for Auxiliary domain (SA) as well as the PSYS domain's reporting functions, incorporated into a single SVID interface. AOS offers a novel AOS Advanced Transient Modulator (A^2TM). It combines an advanced variable frequency hysteretic peak current mode control with proprietary phase current sensing scheme for fast transient response and low system cost. The control loop enhances light-load efficiency by seamlessly entering DCM mode of operation. Autonomous Phase Management also assures optimized efficiency and power loss during light load with single phase DCM mode.

The AOZ71137QI is equipped with SMBus digital Interface enabling register programming for tuning and configuration to minimize the system components and eliminate the need for manual solder rework on system board. Programmability can be done either by AOS GUI or customized ECS into the controller's built-in RAM or MTP. The controller provides MTP to store register settings once the configuration is finalized and the configuration can be updated more than ten times. In production stage, an external resistor can be used for pin strap to choose 1 out of 6 config settings pre-programmed into the parts to achieve easy BOM management and minimize the number of part number and SKU.

Combined with AOS high performance DrMOS and SPS, the AOZ71137QI provides a complete power solution for Intel IMVP9.2 Meteor Lake UH SKU applications. AOZ71137QI comes in a 6mm x 6mm 52-pin QFN package.

The AOZ71137QI controller features very low power consumption while still enabling digital interface control. This unique "Hybrid Digital" control scheme enables low quiescent power consumption in all power states as defined by the Intel IMVP9.2 platform to enable long system run times in battery life workloads.

The AOZ71137QI provides complete protection and warning functions including UVP, OVP, OCP and OTP. Fault protection behavior can be easily programmed through SMBus. AOZ71137 also offers real time telemetry information via SMBus for VIN, VOUT, temperature, output currents, power states as well as PSYS / VSYS / IAUX pins reporting via SMBus.

Features

- 2.5V to 24V VIN input supply voltage
- Triple output rails: 4/3/2/1 + 2/1 + 1 phase
- Meteor Lake UH Platform
- Support Discrete Inductor and 2 phase Coupled Inductor.
- Autonomous Phase Management including Phase shedding and auto DCM to optimize power loss
- Digital & analog hybrid controller with SMBus programmability and lowest power consumption
- SVID Interface to CPU compliant with IMVP8, 9, 9.1 and the latest 9.2 specifications
  - Support Fast V-Mode (FVM)
- Differential remote sensing to achieve 0.5% regulated VOUT accuracy
- Low quiescent current: 3.7mA at PS0 for 2+1+1 configuration
- Supports multi-sourced industry standard DrMOS or SPS power stages
- User friendly GUI for compensation and configurations with minimal external RC components.
- ECS programmability for configurations with Built-in MTP and RAM with more than 10 times configuration changes
- Pin Strap for easy configuration with 6 configuration setting with same PN to minimize number of SKU
- Proprietary, high performance AOS Advanced Transient Modulator (A^2TM) control scheme:
  - Variable frequency hysteretic peak current mode control gives fast transient response
  - Dynamic phase current balance
  - Excellent load-line control and phase current sensing
  - Seamless CCM to DCM control to maximize efficiency
- System Input Power Monitoring (both PSYS and VSYS)
- 300kHz to 1.8MHz programmable switching frequency
- Acoustic Noise Suppression
- Output Under-Voltage Protection (UVP)
- Output Over-Voltage Protection (OVP)
- Over-Current Protection (OCP)
- Over-Temperature Protection (OTP)
- QFN6x6-52L package

Applications

- Meteor Lake Notebook
- Memory and graphic cards
- Video game console

GREEN Product

Typical Application

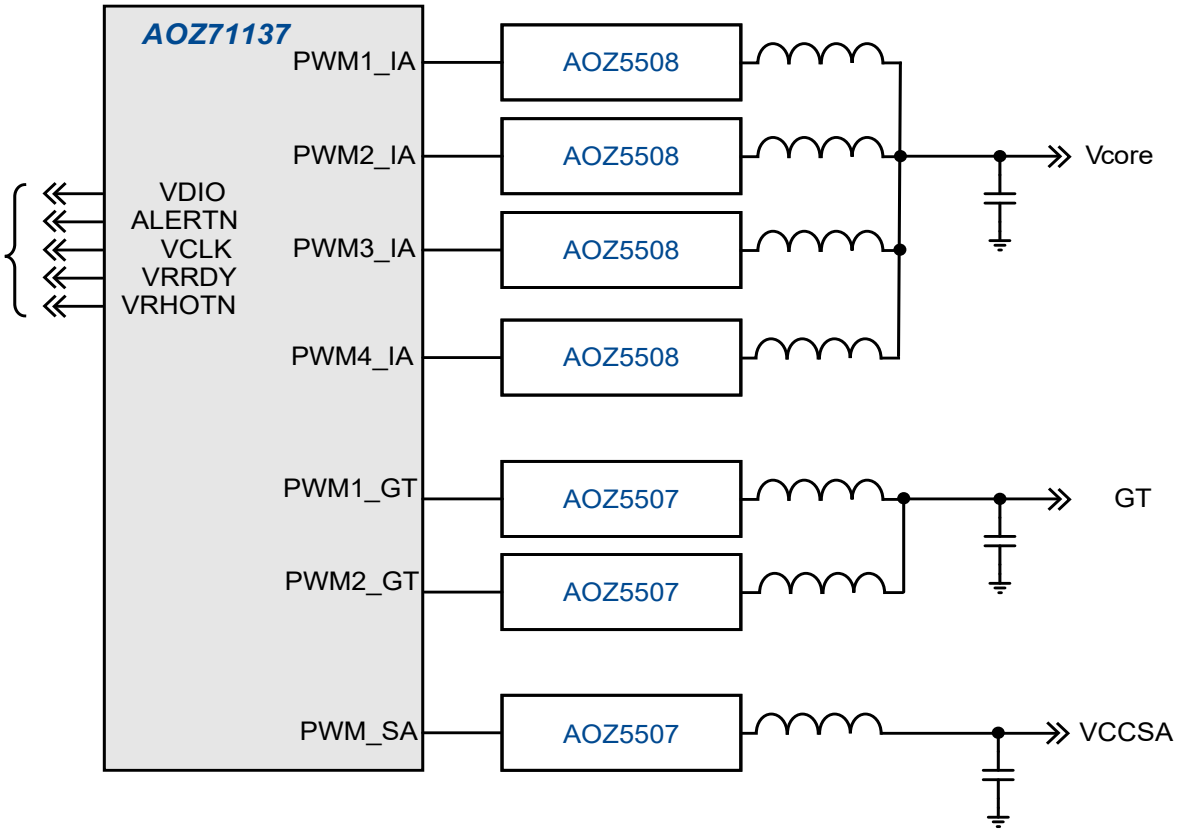


Figure 1. Typical Application

Ordering Information

Part Number[1]	Junction Temperature Range	Package	Environmental
AOZ71137QI-xxx[2]	-40°C to +125°C	QFN6x6-52L	RoHS

Contact local sales office for full product datasheet.

Notes:

1. For each customer, the full PN already created for order is on the last page of this DS. Please refer to last page for more information.
2. "xxx" is the configuration code identifier (also called sub-part number) for the register settings stored in the internal non-volatile memory (NVM). Each "x" can be a value between 0 and 9 and A-Z (except I, J, O, Q). Please work with an AOS Sales/FAE to create this unique number. Each project or board might need to use different sub-PN as the register setting might be different.

AOS products are offered in packages with Pb-free plating and compliant to RoHS standards.
Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

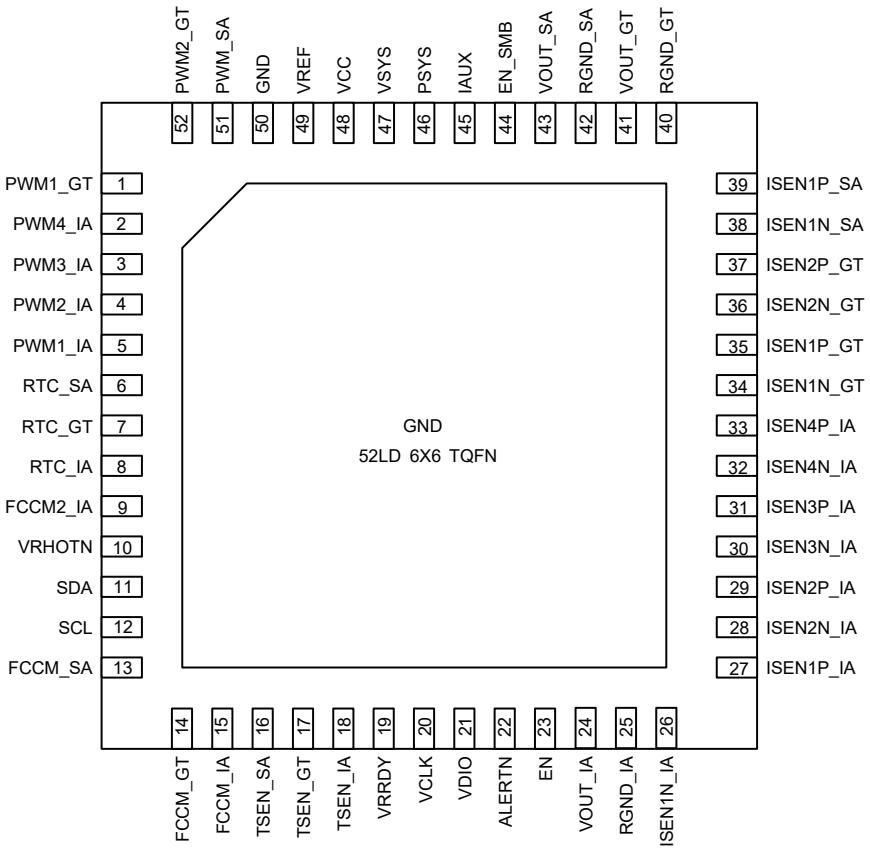


Figure 2. Pin Definition

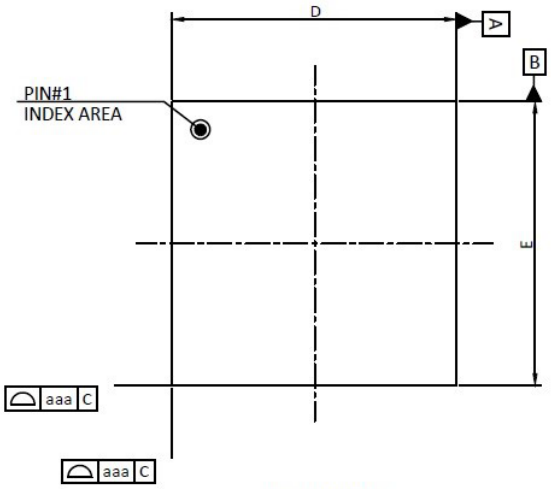
DFN6x6.5-52L
(Top Transparent View)

Pin Description

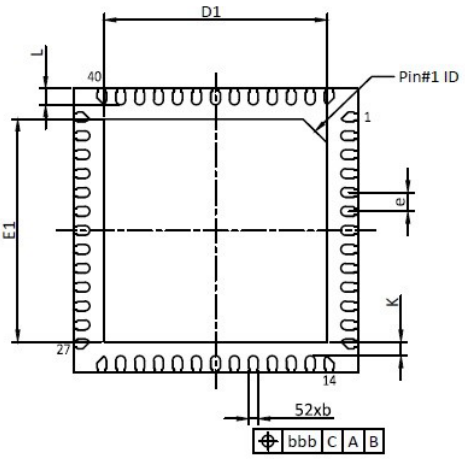
Pin Number	Pin Name	I/O	Pin Function
1	PWM1_GT	O	GT domain PWM signal for Phase 1. Connect to the PWM input of DrMOS.
2	PWM4_IA	O	IA domain PWM signal for Phase 4. Connect to the PWM input of DrMOS.
3	PWM3_IA	O	IA domain PWM signal for Phase 3. Connect to the PWM input of DrMOS.
4	PWM2_IA	O	IA domain PWM signal for Phase 2. Connect to the PWM input of DrMOS.
5	PWM1_IA	O	IA domain PWM signal for Phase 1. Connect to the PWM input of DrMOS.
6	RTC_SA	I	SA domain temperature gain sensing input. Connect a precision 1% resistor to GND and an NTC thermistor to VREF pin for DCR sensing.
7	RTC_GT	I	GT domain temperature gain sensing input. Connect a precision 1% resistor to GND and an NTC thermistor to VREF pin for DCR sensing.
8	RTC_IA	I	IA domain temperature gain sensing input. Connect a precision 1% resistor to GND and an NTC thermistor to VREF pin for DCR sensing.
9	FCCM2_IA	O	Forced Continuous Current Mode for IA domain. Connect to FCCM input of individual DrMOS/ SPS on phases 2-N supplying power for core domain dedicated to low light operation. Continuous mode is active if FCCM is high. DrMOS/SPS is disabled if floating.
10	VRHOTN	O	VR HOT: Active low open drain output to CPU. Notification signal to indicate the system temperature is too high.
11	SDA	I/O	SMBus data line. Open drain I/O. Connect a resistor to VCC.
12	SCL	I/O	SMBus clock line. Open drain input. Connect a resistor to VCC.
13	FCCM_SA	O	Forced Continuous Current Mode for SA domain. Connect to FCCM input of SPS supplying power for SA domain. Continuous mode is active if FCCM is high. Discontinuous mode is active if low. SPS is disabled if floating.
14	FCCM_GT	O	Forced Continuous Current Mode for GT domain. Connect to FCCM input of SPS supplying power for graphics domain. Continuous mode is active if FCCM is high. Discontinuous mode is active if low. SPS is disabled if floating.
15	FCCM_IA	O	Forced Continuous Current Mode for core domain. Connect to FCCM input of phase 1's DrMOS/ SPS supplying power for core domain. Continuous mode is active if FCCM is high. Discontinuous mode is active is low. DrMOS/SPS is disabled if floating.
16	TSEN_SA	I	SA domain temperature sensing input. Connect to TMON from SPS.
17	TSEN_GT	I	GT domain temperature sensing input. Connect to TMON from SPS.
18	TSEN_IA	I	IA domain temperature sensing input. Connect to TMON from SPS.
19	VRRDY	O	VR Ready: Open drain output to CPU. Notification signal to indicate IA, GT and SA output voltages are ready.
20	VCLK	I/O	SVID clock line. Open drain input. Communication line to CPU.
21	VDIO	I/O	SVID data line. Open drain I/O. Communication line to CPU.
22	ALERTN	I/O	VR Alert: Active low open drain output to CPU. Notification signal to indicate all SVID alert conditions.
23	EN	I	Logic input to enable the controller. Active logic high.
24	VOUT_IA	I	Remote CPU IA voltage sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
25	RGND_IA	I	Remote CPU IA ground sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
26	ISEN1N_IA	I	Negative node of IA domain current feedback for droop regulation and output current monitoring for Phase 1. Connect to the VOUT terminal of the inductor for DCR sensing, or connect to Vref in SPS mode.
27	ISEN1P_IA	I	Positive node of IA domain current feedback for droop regulation and output current monitoring for Phase 1. Connect to the center RC network across the inductor for DCR sensing, or connect to IMON of SPS.
28	ISEN2N_IA	I	Negative node of IA domain current feedback for droop regulation and output current monitoring for Phase 2. Connect to the VOUT terminal of the inductor for DCR sensing, or connect to Vref in SPS mode.

Pin Number	Pin Name	I/O	Pin Function
29	ISEN2P_IA	I	Positive node of IA domain current feedback for droop regulation and output current monitoring for Phase 2. Connect to the center RC network across the inductor for DCR sensing, or connect to IMON of SPS.
30	ISEN3N_IA	I	Negative node of IA domain current feedback for droop regulation and output current monitoring for Phase 3. Connect to the VOUT terminal of the inductor for DCR sensing, or connect to Vref in SPS mode.
31	ISEN3P_IA	I	Positive node of IA domain current feedback for droop regulation and output current monitoring for Phase 3. Connect to the center RC network across the inductor for DCR sensing, or connect to IMON of SPS.
32	ISEN4N_IA	I	Negative node of IA domain current feedback for droop regulation and output current monitoring for Phase 4. Connect to the VOUT terminal of the inductor for DCR sensing, or connect to Vref in SPS mode.
33	ISEN4P_IA	I	Positive node of IA domain current feedback for droop regulation and output current monitoring for Phase 4. Connect to the center RC network across the inductor for DCR sensing, or connect to IMON of SPS.
34	ISEN1N_GT	I	Negative node of GT domain current feedback for droop regulation and output current monitoring for Phase 1. Connect to the VOUT terminal of the inductor for DCR sensing, or connect to Vref in SPS mode.
35	ISEN1P_GT	I	Positive node of GT domain current feedback for droop regulation and output current monitoring for Phase 1. Connect to the center RC network across the inductor for DCR sensing, or connect to IMON of SPS.
36	ISEN2N_GT	I	Negative node of GT domain current feedback for droop regulation and output current monitoring for Phase 2. Connect to the VOUT terminal of the inductor for DCR sensing, or connect to Vref in SPS mode.
37	ISEN2P_GT	I	Positive node of GT domain current feedback for droop regulation and output current monitoring for Phase 2. Connect to the center RC network across the inductor for DCR sensing, or connect to IMON from SPS.
38	ISENN_SA	I	Negative node of SA domain current feedback for droop regulation and output current monitoring. Connect to the VOUT terminal of the inductor for DCR sensing, or connect to Vref in SPS.
39	ISENP_SA	I	Positive node of SA domain current feedback for droop regulation and output current monitoring. Connect to the center RC network across the inductor for DCR sensing, or connect to IMON of SPS.
40	RGND_GT	I	Remote CPU GT ground sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
41	VOUT_GT	I	Remote CPU GT voltage sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
42	RGND_SA	I	Remote CPU SA ground sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
43	VOUT_SA	I	Remote CPU SA voltage sensing for control loop feedback and regulation. Connect to CPU prescribed pin.
44	EN_SMB	I	SMBus enable input. Connect to VCC to allow SMBus register read/write. For pin strap block mode and bulk mode, connect MCU GPIO pin or ground through a RADC resistor to choose configuration settings.
45	IAUX	I	Current monitor input from VCCIN_AUX rail. Input analog signal will be converted to digital signal and communicated to the CPU through SVID Bus via the PSYS domain.
46	PSYS	I	System power monitor input from Battery Charger. Input analog signal will be converted to digital signal and communicate with CPU through SVID Bus via the PSYS domain.
47	VSYS	I	System power monitor input voltage level from battery output. Input analog signal will be converted to digital signal and communicate with CPU through SVID Bus via the PSYS domain.
48	VCC	I	Power supply for the controller. Connect a 1µF MLCC capacitor to GND.
49	VREF	O	2.56V reference voltage output in DCR sensing mode. Connect NTC thermistors from TSEN_IA/GT/SA to this pin. VREF changes to 1.2V as IMON reference for SPS mode
50	GND		Ground pin. Must be connected directly to EP.
51	PWM_SA	O	SA domain PWM signal for Phase 1. Connect to the PWM input of DrMOS.
52	PWM2_GT	O	GT domain PWM signal for Phase 2. Connect to the PWM input of DrMOS.

Package Dimensions, QFN6x6-52L

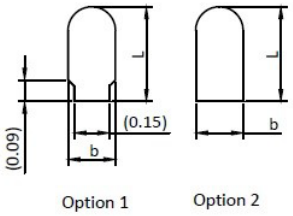


TOP VIEW



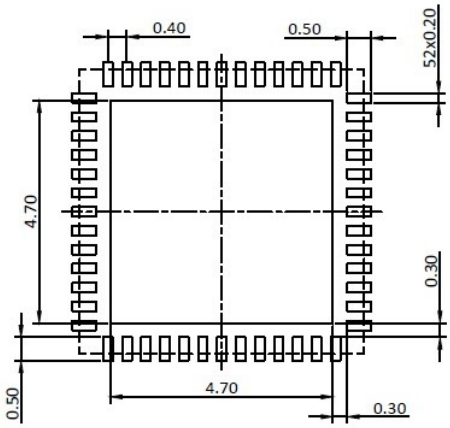
BOTTOM VIEW

SIDE VIEW



Lead Option

RECOMMENDED LAND PATTERN



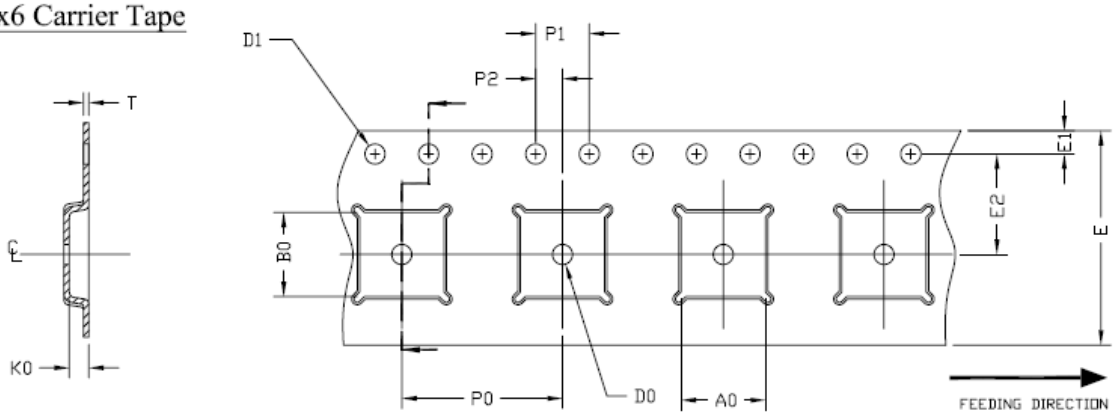
SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.15	0.20	0.25	0.006	0.008	0.010
b	0.15	0.20	0.25	0.006	0.008	0.010
D	5.90	6.00	6.10	0.232	0.236	0.240
D1	4.55	4.70	4.80	0.179	0.185	0.189
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.55	4.70	4.80	0.179	0.185	0.189
e	0.40 BSC			0.016 BSC		
K	0.20	0.30	0.40	0.008	0.012	0.016
L	0.25	0.35	0.45	0.010	0.014	0.018
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.08			0.003		

UNIT: mm

NOTE:
1. CONTROLLING DIMENSION IS MILLIMETER.
2. CO-PLANARITY APPLIES TO THE EXPOSED PAD AND THE LEADS.

Tape and Reel Dimensions, QFN6x6-52L

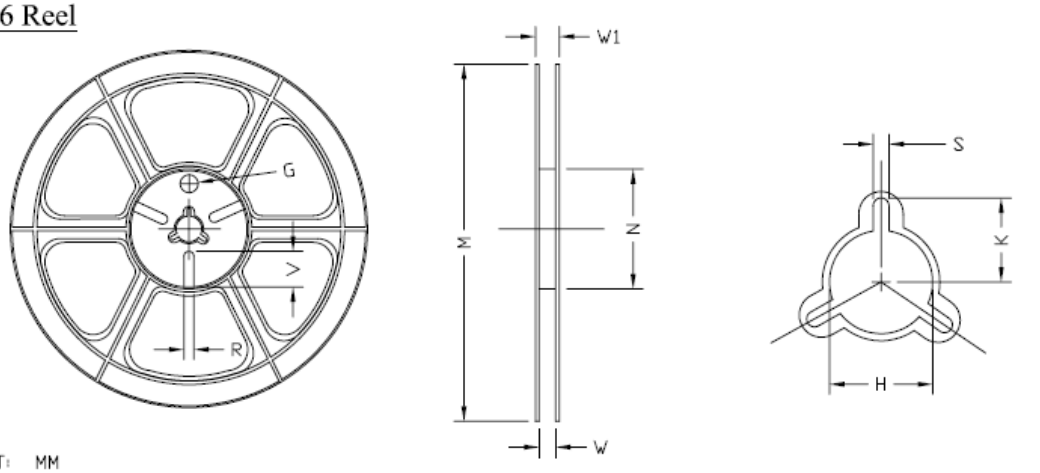
QFN6x6 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN6x6 (16 mm)	6.30 ±0.20	6.30 ±0.20	1.10 ±0.20	1.50 MIN.	1.50 $^{+0.1}_{-0.0}$	16.0 ±0.3	1.75 ±0.10	7.5 ±0.1	12.00 ±0.20	4.00 ±0.20	2.00 ±0.10	0.30 ±0.05

QFN6x6 Reel

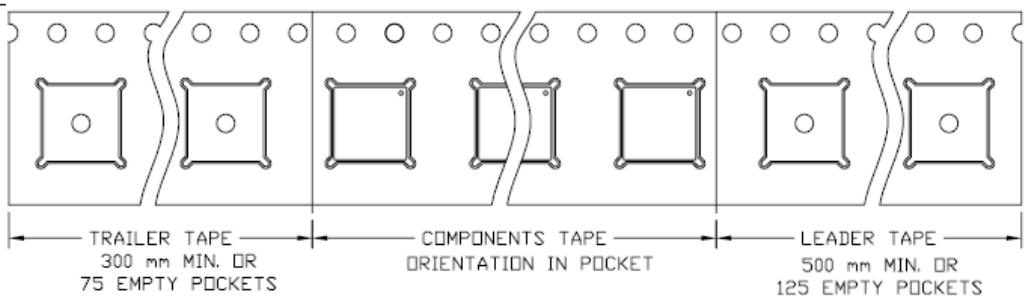


UNIT: MM

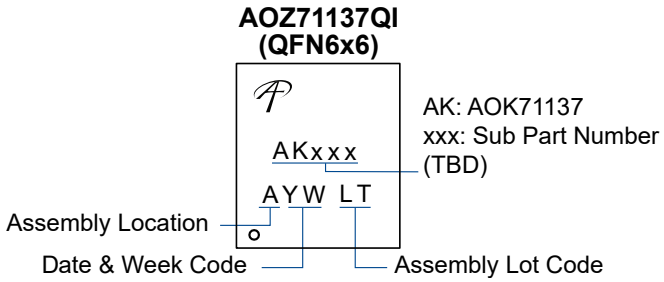
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
16 mm	ø330	ø330 MAX.	ø100 MIN.	16.4 $^{+2.0}_{-0.0}$	22.4 MAX.	ø13.0 $^{+0.5}_{-0.2}$	10.1 MIN.	1.5 MIN.	---	---	---

QFN6x6 Tape

Leader / Trailer & Orientation



Part Marking



Sub PN Marking	SKU	Project Descriptions	Full PN	Full Marking in Label
000	Blank Configuration	Blank Parts	AOZ71137QI-000	AOZ71137QI-000

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.