

# AOZ73004CQI

NVIDIA OpenVReg Compliant Controller Multiphase Controller with PWMVID Interface

### **General Description**

The AOZ73004CQI is a high performance multiphase buck controller designed in compliance with NVIDIA OpenVReg specifications. It provides one output rail and supports PWMVID interface.

AOS offers a novel AOS Advanced Transient Modulator (A<sup>2</sup>TM). It combines an advanced variable frequency hysteretic peak current mode control with proprietary phase current sensing scheme for fast transient response and low system cost. The control loop enhances light-load efficiency by seamlessly entering DCM mode of operation. Autonomous Phase Management also assures the optimized efficiency and power loss during light load with single phase DCM mode.

The AOZ73004CQI provides complete protection including UVP, OVP, thermal warning, cycle-by-cycle current limit. AOZ73004CQI also offers real time telemetry information via IMON pin for output currents.

The AOZ73004CQI features an external reference input and PWMVID dynamic output voltage control, in which the output voltage is regulated and tracks the external input reference voltage. The PWMVID duty cycle determines the variable output voltage at REFIN, Vmin is the zero percent duty cycle voltage value. Vmax is the one hundred percent duty cycle voltage value.

AOZ73004CQI can be paired and supports multi-sourced industry standard DrMOS. AOZ73004CQI is offered in compact 4mm x 4mm 32-pin QFN package.

### **Features**

- Compliant with NVIDIA OVR-4-22 specifications
- Supports up to 4 phase
- 2.7V to 20V VIN input supply voltage
- 300 kHz to 1 MHz programmable switching frequency
- High performance operational error amplifier
- Differential remote sensing to achieve 1% regulated VOUT accuracy
- Supports multi-sourced industry standard DrMOS
- Proprietary, high performance AOS Advanced Transient Modulator (A<sup>2</sup>TM) control scheme:
  - Variable frequency hysteretic peak current mode control gives fast transient response
  - Dynamic phase-to-phase current balancing
  - Excellent phase current sensing
  - Seamless CCM to DCM control to maximize efficiency
- Supports DCR or R<sub>ON LG</sub> sensing current balance
- Automatic Phase Shedding (APS) with user settable thresholds
- Power Saving Interface (PSI)
- Supports Diode Emulation Mode (DEM)
- PWMVID interface
- Output Under-Voltage Protection (UVP)
- Output Over-Voltage Protection (OVP)
- Cycle-by-Cycle current limit
- Thermal Warning (THWRN)

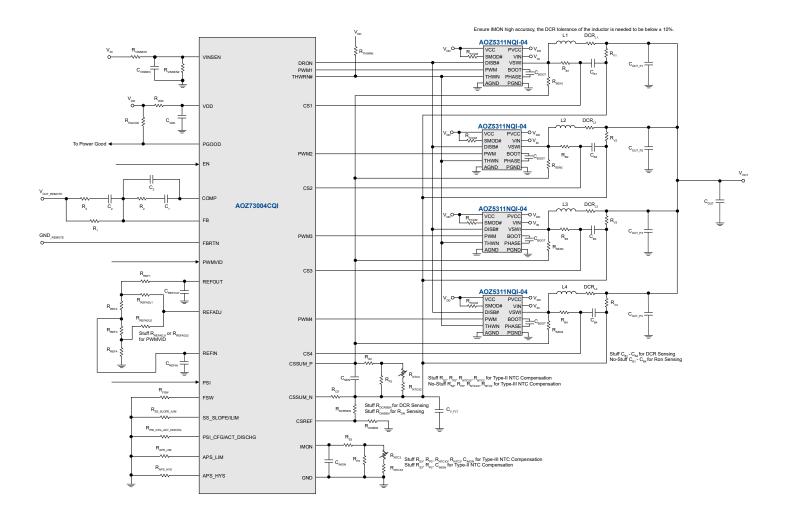
### **Applications**

- GPU and CPU power
- Graphic cards
- Desktop and notebook applications





# **Typical Application**





# **Ordering Information**

Part Number Ambient Temperature Range		Package	Environmental	
AOZ73004CQI	-40°C to +125°C	QFN4x4-32L	Green	

### Contact local sales office for full product datasheet.



AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit https://aosmd.com/sites/default/files/media/AOSGreenPolicy.pdf for additional information.

# **Pin Configuration**

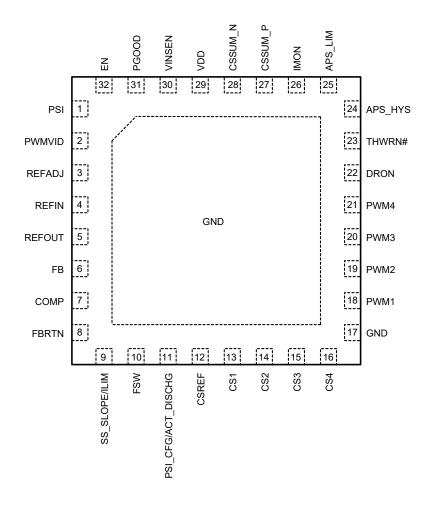


Figure 1. QFN4x4-32L

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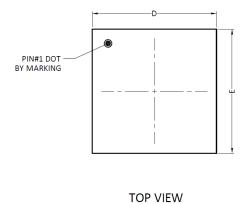


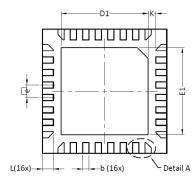
# **Pin Description**

Pin Number	Pin Name	Pin Function					
1 PSI		Power Saving Interface control pin. This pin can be set low, high or left floating. If this pin needs to be pulled up, the maximum resistance should be below $10k\Omega$ . If this pin needs to be pulled down, the maximum resistance should be below $5.1k\Omega$ .					
2	PWMVID	PWMVID input. If this pin needs to be pulled up, the maximum resistance should be below $10k\Omega$ . If this pin needs to be pulled down, the maximum resistance should be below $5.1k$					
3	REFADJ	PWMVID buffer output. Refer to PWMVID dynamic voltage control.					
4	REFIN	Reference voltage input for output voltage regulation.					
5	REFOUT	PWMVID reference output, which is regulated to 2V. A minimum 0.22µF decoupling capacitor is required from this pin to ground.					
6	FB	Error amplifier inverting input.					
7	COMP	Output of the error amplifier.					
8	FBRTN	Remote OUTPUT ground sensing for control loop feedback and regulation.					
9	SS_SLOPE/ILIM	Soft-start and current limit setting pin. Connect a resistor to ground to program soft-start slope and current limit level.					
10	FSW	Switching frequency setting pin. Connect a resistor to ground to select the switching frequency.					
11	PSI_CFG/ ACT_DISCHG	This pin is a combined strap to enable active discharge and configure for flexible assignment of active phases to power zones in APS mode. The lowest zone configured by the PSI_CFG portion of this strap is the zone used when the PSI pin is pulled low.					
12	CSREF	Current sense reference.					
13	CS1	Positive node of current balance sense circuit for phase 1.					
14	CS2	Positive node of current balance sense circuit for phase 2.					
15	CS3	Positive node of current balance sense circuit for phase 3.					
16	CS4	Positive node of current balance sense circuit for phase 4.					
17	GND	Ground pin.					
18	PWM1	PWM signal for Phase 1. Connect to the PWM input of DrMOS.					
19	PWM2	PWM signal for Phase 2. Connect to the PWM input of DrMOS.					
20	PWM3	PWM signal for Phase 3. Connect to the PWM input of DrMOS.					
21 PWM4		PWM signal for Phase 4. Connect to the PWM input of DrMOS.					
22	DRON	Gate driver enable for external drivers.					
23	THWRN#	Thermal fault indication from power stage.					
24	APS_HYS	A dedicated strap sets the automatic phase shedding (APS) hysteresis. Connect a resistor to ground to program the hysteresis value. The value of APS_LIM minus the hysteresis value is the leaving phase threshold when current falling down.					
25	APS_LIM	A dedicated strap sets the automatic phase shedding (APS) threshold limit. Connect a resistor to ground to program the threshold of entering different phase when current rising up.					
26	IMON	The IMON pin outputs a current proportional to the sum of the measured inductor current. Ensure IMON high accuracy, the DCR tolerance of the inductor is needed to below ±10%.					
27	CSSUM_P	Current Sensing positive terminal.					
28	CSSUM_N	Current Sensing negative terminal.					
29	VDD	Power for the internal control circuits. A $4.7\mu\text{F}\sim10\mu\text{F}$ decoupling capacitor is required from this pin to ground.					
30	VINSEN	Input voltage sense for feed forward.					
31	PGOOD	Power good signal output. PGOOD is an open-drain output used to indicate the status of the output voltage. PGOOD is pulled low during soft-start and shut down.					
32	EN	Enable input. The AOZ73004CQI is enabled when EN is pulled high. The device shuts down when EN is pulled low. Assert EN to high for power-up after VIN and VDD are well supplied.					

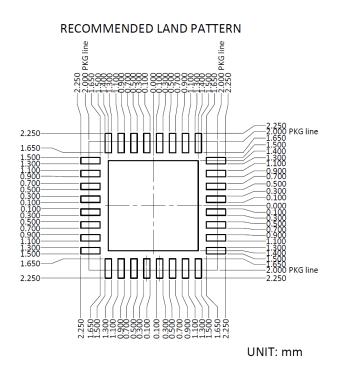


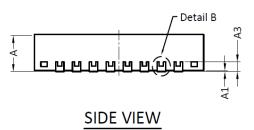
# Package Dimensions,QFN4x4-32L





BOTTOM VIEW





SYMBOLS	DIM.	IN MILLM	ETERS	DIM. IN INCHS				
STIVIBULS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
Α	0.800	-	1.000	0.031	-	0.039		
A1	0.000	0.020	0.050	0.000 0.001		0.002		
A3		0.203 REF		0.008 REF.				
b	0.150	0.200	0.250	0.006	0.008	0.010		
D	3.900	4.000	4.100	0.154	0.157	0.161		
D1	2.700	2.800	2.900	0.106	0.110	0.114		
E	3.900	4.000	4.100	0.154	0.157	0.161		
E1	2.700	2.800	2.900	0.106	0.110	0.114		
e		0.400 BSC			0.016 BSC			
L	0.250	0.350	0.450	0.010	0.014	0.018		
K	0.250 REF.			0.010 REF.				

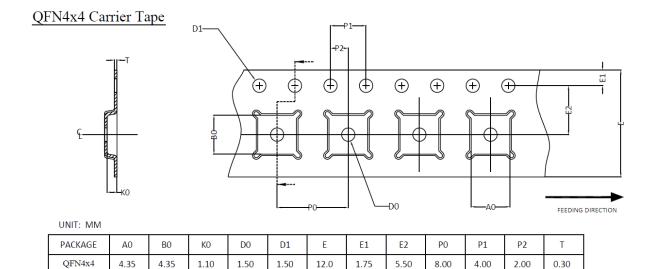
### NOTE:

1. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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# Tape and Reel Dimensions, QFN4x4-32L



±0.3

+0.1

MIN.

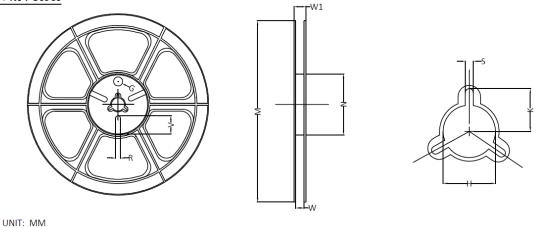


 $\pm 0.10$ 

±0.10

 $\pm 0.10$ 

(12 mm)



±0.10

±0.05

±0.10

±0.10

±0.05

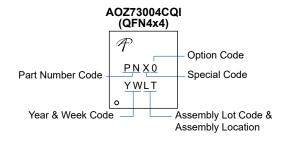
±0.05

TAPE SIZE	REEL SIZE	М	N	W	W1	Н	K	S	G	R	V
12 mm	Ø330	Ø330.0 ±2.0	Ø79.0 ±1.0	12.4 +2.0 -0.0	17.0 +2.6 -1.2	Ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5			

#### QFN4x4 Tape Leader / Trailer $\oplus$ ⊕ $\oplus$ & Orientation Normal Unit Per Reel: 3000pcs COMPONENTS TAPE TRAILER TAPE LEADER TAPE 300 mm MIN. OR ORIENTATION IN POCKET 500 mm MIN. OR **60 EMPTY POCKETS** 70 EMPTY POCKETS



### **Part Marking**



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