



**ALPHA & OMEGA**  
SEMICONDUCTOR

# ***AOS Semiconductor Product Reliability Report***

**AOZ15333DI** rev A

**Plastic Encapsulated Device**

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The AOS product reliability report summarizes the qualification results for AOZ15333DI in DFN3x3-12L package. Accelerated environmental tests are performed on a specific sample size, samples are electrically tested before and after each stress time point. Review of final electrical test results confirm that AOZ15333DI pass the AOS quality and reliability requirements. The released products will be categorized by its process family and routinely monitored for continuous improvement of product quality.

## I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Sample Size / Lots	Number of Failures	Reference Standard
HTOL	T <sub>J</sub> = 150°C, V <sub>IN</sub> = Vin_max	168 / 500 / 1000 hours	231 pcs (3 lots)	0	JESD22-A108
Preconditioning (Note A)	T <sub>A</sub> = 85°C, RH = 85% + 3 cycle reflow @ 260°C (MSL 1)	168hours	924 pcs (3 lots)	0	JESD22-A113
HAST	T <sub>A</sub> = 130°C, RH = 85%, P = 33.3psia, V <sub>IN</sub> = Vin_max	96 hours	231 pcs (3 lots)	0	JESD22-A110
Autoclave	T <sub>A</sub> = 121°C, RH = 100%, P = 29.7psia	96 hours	231 pcs (3 lots)	0	JESD22-A102
Temperature Cycle	T <sub>A</sub> = -65°C to 150°C, air to air	250 / 500 cycles	231 pcs (3 lots)	0	JESD22-A104
High Temperature Storage	T <sub>A</sub> = 150°C	168/500/ 1000 hours	231 pcs (3 lots)	0	JESD22-A103

**Note:** The reliability data presents total of available generic data up to the published date.

Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

## II. Reliability Evaluation

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the product technology. Failure Rate Determination is based on JEDEC Standard JESD 85.

**FIT rate (failures per billion device hours): 14.10**

**MTTF = 70.9 million hours =8098 years**

**Condition:** V<sub>o</sub> = 5.5V, T<sub>o</sub> = 55°C, V<sub>s</sub> = 5.5V and T<sub>s</sub> = 125°C

**Sample Size:871**

The failure rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \chi^2[CL, (2f+2)] / 2 \times [1 / (SS \times t \times AF)]; \text{ [equation 1]} \quad \text{where} \quad \begin{array}{l} CL = \% \text{ of confidence level} \\ f = \text{number of failure} \\ SS = \text{sample size} \\ t = \text{stress time} \end{array}$$

Looking up the  $\chi^2/2$  table for zero failure (burn-in) with 60% confidence, the value of  $\chi^2[CL, (2f+2)] / 2$  is 0.92.

The Acceleration Factor (AF) is calculated from the following formula (both temperature and voltage acceleration factors are used in the final acceleration factor calculation) :

$$AF = AF_T \times AF_V = \exp[(E_a/k) \times (1/T_o - 1/T_s)] \times \exp[\beta (V_s - V_o)] \text{ where} \quad \begin{array}{l} E_a = \text{activation energy} \\ k = \text{Boltzmann constant} \\ T_o = \text{operating } T_J \\ T_s = \text{stress } T_J \\ V_s = \text{stress voltage} \\ V_o = \text{operating voltage} \\ \beta = \text{voltage acceleration coefficient} \end{array}$$

Assuming typical operating environment,  $V_o = 5.5V$ ,  $T_o = 55^\circ C$ ,  $E_a = 0.7eV$ ,  $V_s = 5.5V$ ,  $T_s = 150^\circ C$ ,  $\beta = 0.5$  (silicon defect)

$$AF = \exp \left[ \left( \frac{0.7}{8.617E - 5} \right) \cdot \left( \frac{1}{273 + 55} - \frac{1}{273 + 125} \right) \right]$$

Substituting the values in equation 1, we have  $\lambda =$

$$0.92 \cdot \frac{1}{\text{sample Size} \cdot \text{Stress Duration} \cdot AF} \text{ hr}^{-1}$$

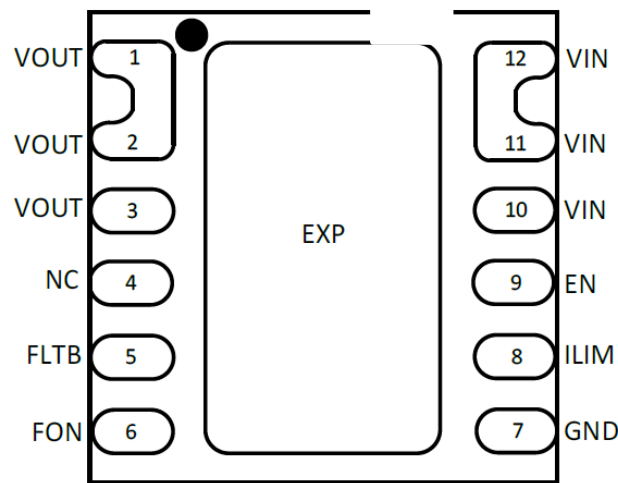
$\lambda = 14.10 \cdot 10^{-9} \text{ hr}^{-1}$  or 14.10 FIT;  $MTTF = (1/\lambda) = 70.9$  million hrs = 8,098 years

The calculation shows failure rate is 14.10 FIT, MTTF is 70.9 million hours under typical operating conditions.

### III. ESD and Latch Up Test Results

Test	Test Conditions	Total Sample Size	Number of Failures	Reference Standard
Electrostatic Discharge Human Body Model	$T_A = 25^\circ C$ , +/-2kV	10	0	JESD-A114
Electrostatic Discharge Charged Device Model	$T_A = 25^\circ C$ , +/-1kV	10	0	JESD-C101
Latch Up	$T_A = 25^\circ C$ , +/-100mA, 1.5x OV	10	0	JESD78
Latch Up	$T_A = 125^\circ C$ , +/-100mA, 1.5x OV	10	0	JESD78

**Note:** ATE results are used to determine PASS/FAIL. Parametric shift<10%.



DFN3x3-12L

Top Transparent View