



ALPHA & OMEGA
SEMICONDUCTOR

***AOS Semiconductor
Product Reliability Report***

AOZ97774QE

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

**475 Oakmead Parkway
Sunnyvale, CA 94085
United States**

**Tel: (408)830-9742
www.aosmd.com**

The AOS product reliability report summarizes the qualification results for AOZ97774QE in QFN5x5-40L package. Accelerated environmental tests are performed on a specific sample size, samples are electrically tested before and after each stress time point. Review of final electrical test results confirm that AOZ97774QE pass the AOS quality and reliability requirements. The released products will be categorized by its process family and routinely monitored for continuous improvement of product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Sample Size / Lots	Number of Failures	Reference Standard
HTOL	$T_J = 150^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, $V_{PINX} = 14\text{V}$	168 / 500 / 1000 hours	231 pcs (3 lots)	0	JESD22-A108
Preconditioning (Note A)	$T_A = 85^{\circ}\text{C}$, RH = 85% + 3 cycle reflow @ 260°C (MSL 1)	168hours	924 pcs (3 lots)	0	JESD22-A113
HAST	$T_A = 130^{\circ}\text{C}$, RH = 85%, P = 33.3psia, $V_{CC} = 3.6\text{V}$, $V_{PINX} = 14\text{V}$	96 hours	231 pcs (3 lots)	0	JESD22-A110
Autoclave	$T_A = 121^{\circ}\text{C}$, RH = 100%, P = 29.7psia	96 hours	231 pcs (3 lots)	0	JESD22-A102
Temperature Cycle	$T_A = -65^{\circ}\text{C}$ to 150°C , air to air	500 / 1000 cycles	231 pcs (3 lots)	0	JESD22-A104
HTSL	$T_A = 150^{\circ}\text{C}$	1000 hours	231 pcs (3 lots)	0	JESD22-A103
Solderability (SnAgCu = 96.5/3/0.5%)	Steam Aging = $93^{\circ}\text{C} \pm 3^{\circ}\text{C}$ $T_{SOLDER} = 245^{\circ}\text{C} \pm 5^{\circ}\text{C}$	1 hour 5 sec	45 pcs (3 lots)	0	M2003 J-STD-002

Note: The reliability data presents total of available generic data up to the published date.
 Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the product technology. Failure Rate Determination is based on JEDEC Standard JESD 85.

FIT rate (failures per billion device hours): 12.36
MTTF = 80.9 million hrs

Condition: $V_o = 3.3V$, $T_o = 55^\circ C$, $V_s = 3.6V$ and $T_s = 150^\circ C$
Sample Size: 240

The failure rate (λ) is calculated as follows:

$$\lambda = \chi^2[CL, (2f+2)] / 2 \times [1 / (SS \times t \times AF)]; \text{ [equation 1]} \quad \text{where}$$

- CL = % of confidence level
- f = number of failure
- SS = sample size
- t = stress time

Looking up the $\chi^2/2$ table for zero failure (burn-in) with 60% confidence, the value of $\chi^2[CL, (2f+2)] / 2$ is 0.92.

The Acceleration Factor (AF) is calculated from the following formula (both temperature and voltage acceleration factors are used in the final acceleration factor calculation):

$$AF = AF_T \times AF_V = \exp[(E_a/k) \times (1/T_o - 1/T_s)] \times \exp[\beta (V_s - V_o)] \text{ where}$$

- E_a = activation energy
- k = Boltzmann constant
- T_o = operating T_J
- T_s = stress T_J
- V_s = stress voltage
- V_o = operating voltage
- β = voltage acceleration coefficient

Assuming typical operating environment, $V_o = 3.3V$, $T_o = 55^\circ C$, $E_a = 0.7eV$, $V_s = 3.6V$, $T_s = 150^\circ C$, $\beta = 0.5$ (silicon defect)

$$AF(IC) = \exp \left[\left(\frac{0.7}{8.617E - 5} \right) \cdot \left(\frac{1}{273 + 55} - \frac{1}{273 + 150} \right) \right] \cdot \exp[0.5 \cdot (3.6V - 3.3V)]$$

Substituting the values in equation 1, we have

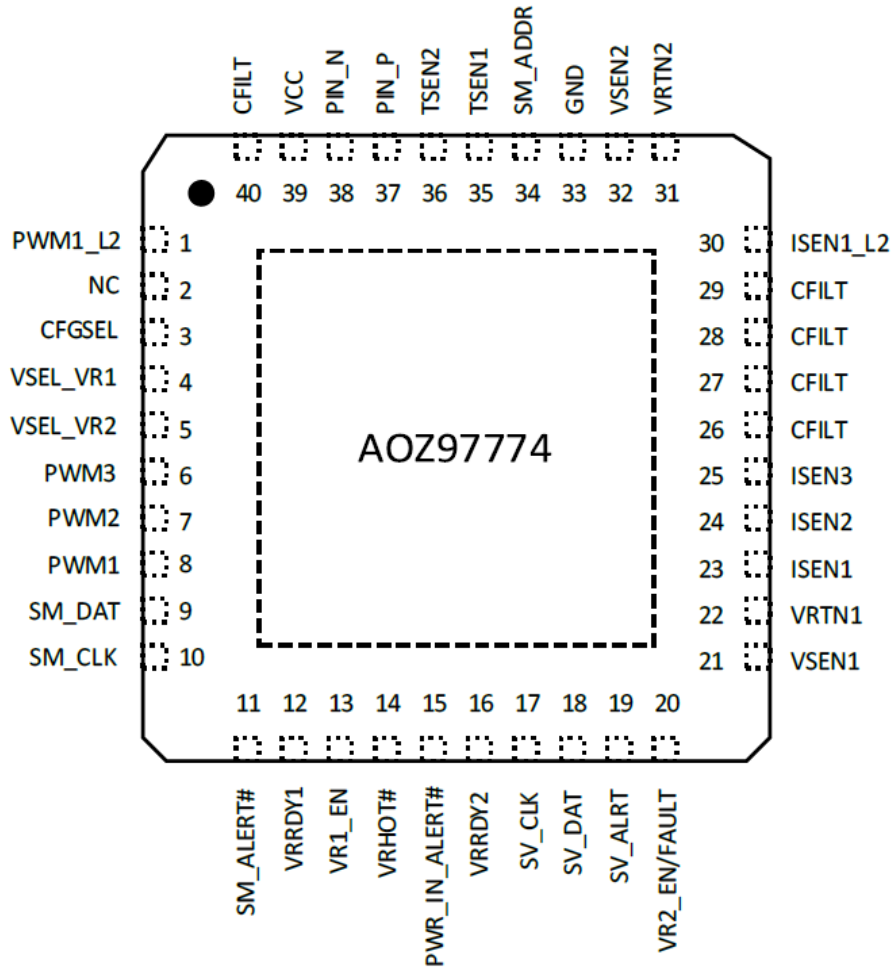
$$0.92 \cdot \frac{1}{\text{sample Size} \cdot \text{Stress Duration} \cdot AF(IC)} \text{ hr}^{-1}$$

$\lambda = 12.36 \cdot 10^{-9} \text{ hr}^{-1}$ or 12.36 FIT; MTTF = $(1/\lambda) = 80.9$ million hrs

III. ESD and Latch Up Test Results

Test	Test Conditions	Total Sample Size	Number of Failures	Reference Standard
Electrostatic Discharge Human Body Model	T _A = 25°C, +/-2kV	10	0	JESD-A114
Electrostatic Discharge Charged Device Model	T _A = 25°C, +/-1kV	10	0	JESD-C101
Latch Up	T _A = 25°C, +/-100mA, 1.5x OV	10	0	JESD78
Latch Up	T _A = 125°C, +/-100mA, 1.5x OV	10	0	JESD78

Note: ATE results are used to determine PASS/FAIL. Parametric shift<10%.



**Figure 3. QFN5x5_40L
(Top View)**